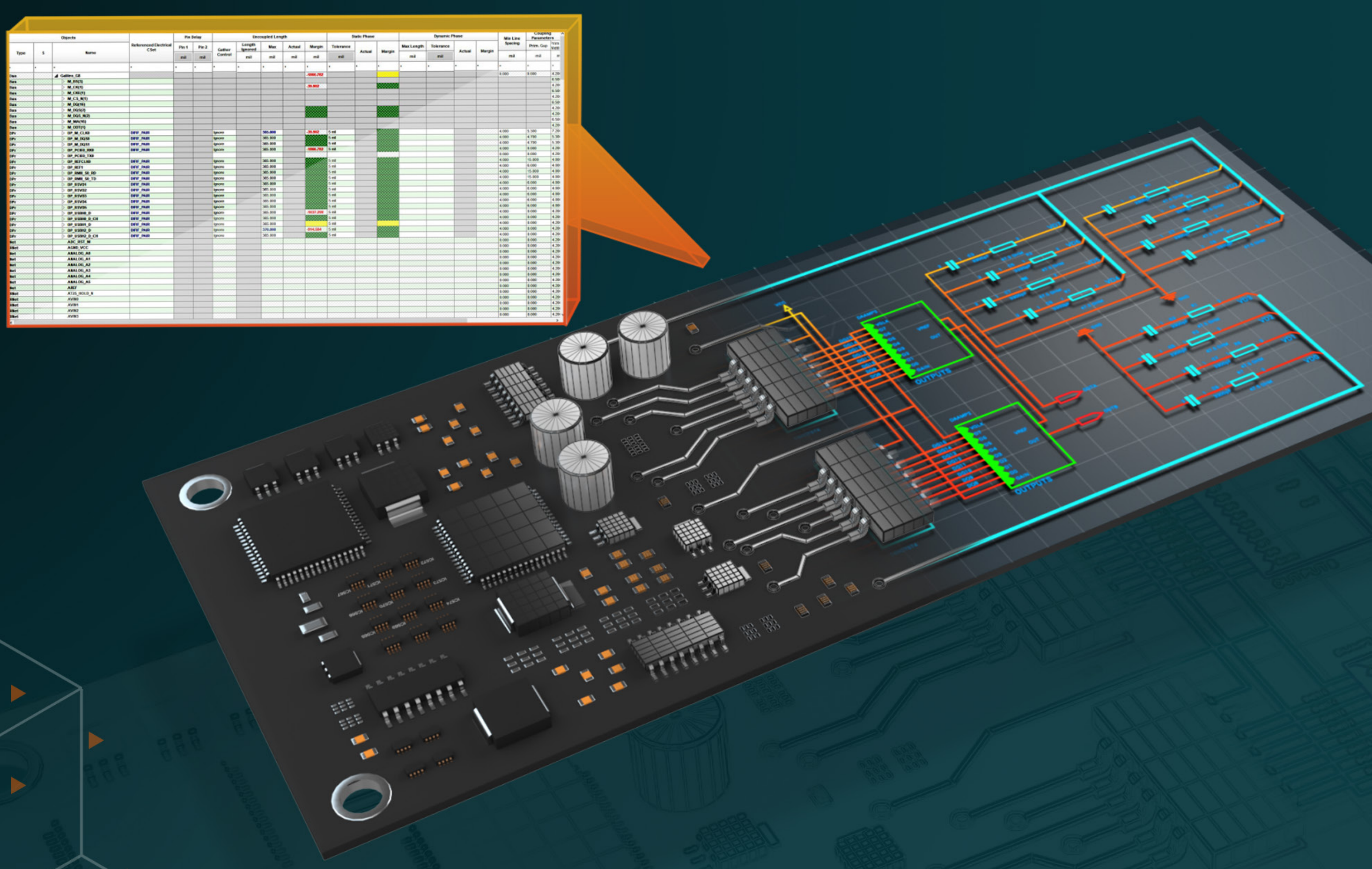
DESIGN **GUIDE**

cadence

OrCAD X Constraint Management Guide

Part 1 of 5



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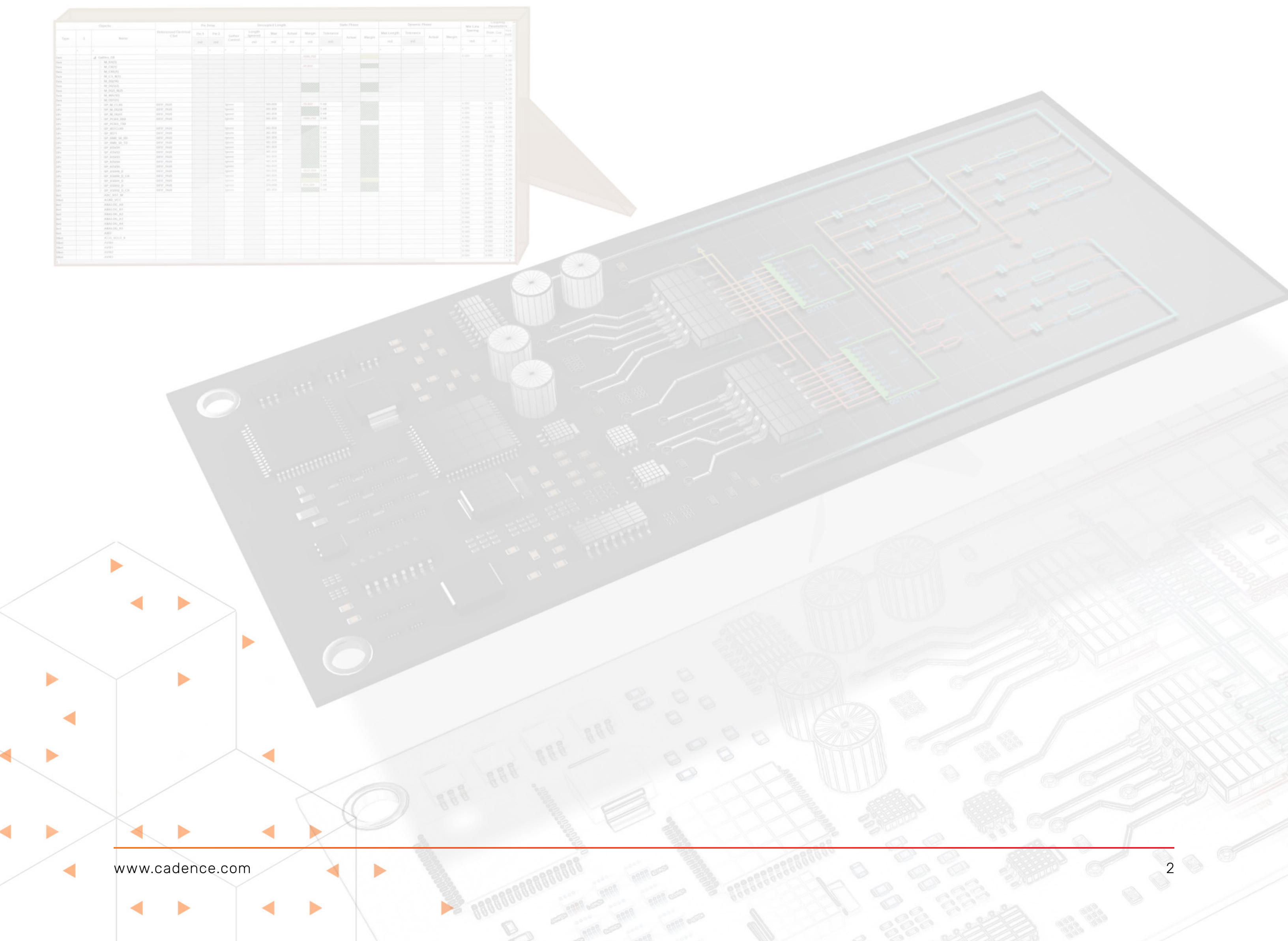


Part 1 – Introduction to Constraint Management

Imagine a world where electronic devices are unreliable, prone to failure, and exhibit inconsistent performance. This was once the reality in the early days of printed circuit board (PCB) design. Enter the hero of our story: constraint management.

Picture a team of engineers working tirelessly on a groundbreaking new smartphone. As they design the PCB, they face a myriad of challenges: signals degrading over long traces, components overheating, and electromagnetic interference causing mysterious glitches. Without a system to manage these issues, their project is at risk of failure.

Constraint management emerges as the solution, offering a set of guidelines and automated tools to ensure design integrity. It's like having a vigilant guardian watching over every aspect of the PCB design, from signal integrity to thermal management.

With constraint management, engineering teams can confidently tackle complex designs. They can prevent signal degradation in high-speed circuits, minimize electromagnetic interference, and ensure proper power distribution. Manufacturing becomes smoother, with fewer errors and increased yield.

The benefits are clear: reduced design errors, improved performance, enhanced reliability, and streamlined manufacturing. Whether it's a cutting-edge smartphone, a reliable automotive system, or a critical aerospace component, constraint management plays a crucial role in bringing these innovations to life.

In the ever-evolving world of electronics, where devices are becoming smaller, faster, and more complex, constraint management in PCB design software isn't just a nice-to-have—it's an absolute necessity for creating the reliable, high-performance devices we depend on every day.

What is Constraint Management?

Constraint management is a system for defining and enforcing design rules such as electrical, physical, spacing, manufacturing, and more in PCB layout.

It includes a set of guidelines ensuring the design meets specific performance, manufacturability, and reliability criteria.

Constraint management tools help automate the process of checking and enforcing these rules during the design phase.

Problems Solved by Constraint Management

Robust constraint management practices help mitigate design issues earlier within the PCB development cycle and address the following common design challenges:

- **Signal Integrity:** Ensures signals are transmitted without degradation, which is crucial for high-speed circuits.
- **Electromagnetic Interference:** Minimizes the interference caused by electromagnetic noise, ensuring the PCB operates reliably in various environments.
- **Manufacturing Constraints:** Ensures that the PCB design complies with the manufacturing processes, reducing the risk of errors and increasing yield.
- **Power Distribution:** Manages power distribution across the PCB to prevent voltage drops and ensure stable operation of components.
- **Thermal Management:** Ensures proper heat dissipation to prevent overheating, which can damage components and affect performance.

Benefits of Proper Constraint Management

Effective constraint management leads to designing functional and reliable PCBs. Here are some benefits of a properly constrained design:

- **Reduces Design Errors:** Using automated rule checks that help identify and correct errors early in the design process.
- **Improves Performance:** Adhering to constraints ensures that the PCB will perform as intended under various conditions.
- **Enhances Reliability:** Proper constraint management leads to designs that are less likely to fail in the field.
- **Streamlines Manufacturing:** Ensures the design is compatible with manufacturing processes, reducing delays and costs.

Applications of Constraint Management

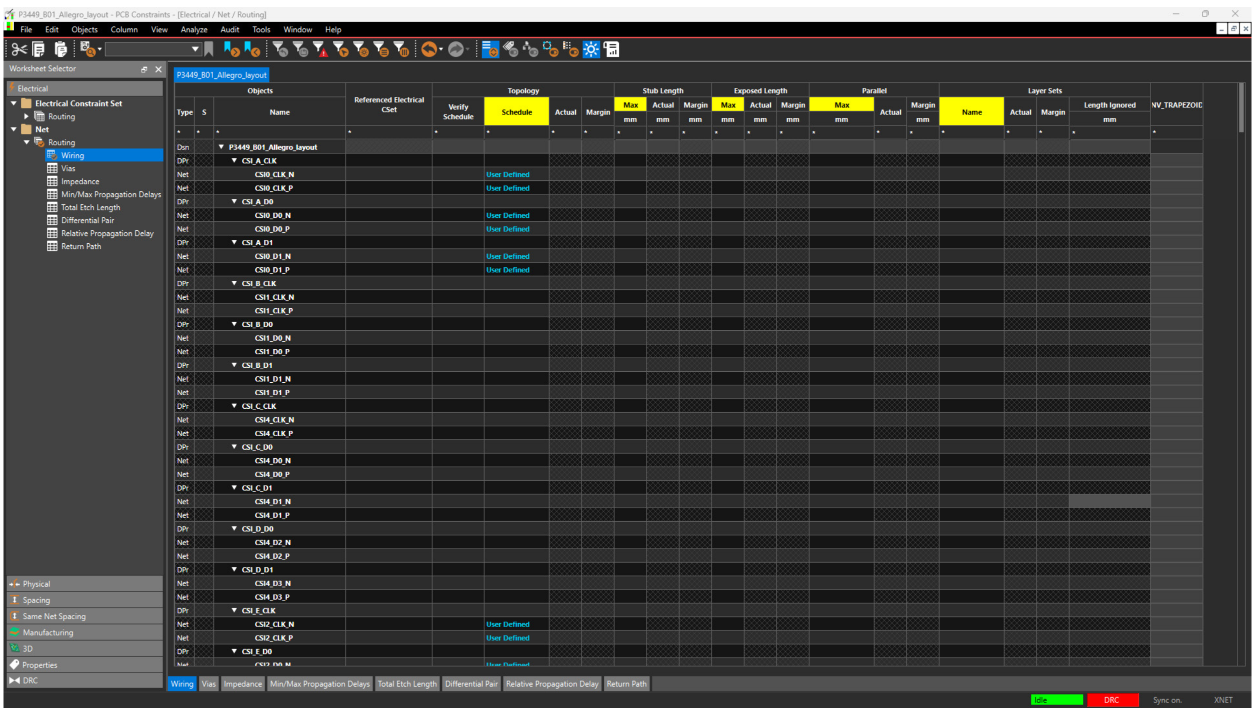
Used in various PCB designs, especially those with complex requirements or high-speed applications. Below are some applications where constraint management is commonly applied:

- **High-Speed PCBs:** Where signal integrity and timing are critical.
- **Complex Multilayer Boards:** Where managing multiple constraints is essential for performance and manufacturability.
- **Consumer Electronics:** Ensures reliable operation in compact and thermally challenging environments.
- **Automotive and Aerospace:** Where reliability and adherence to stringent standards are crucial.

Now that we understand the impact and importance of constraint management in PCBs, let's discuss the types of constraints and how the Cadence® OrCAD® X Platform organizes constraints in a way that is easy and flexible.

Finding the Constraint Manager (CM)

In OrCAD X Presto PCB Editor, select **Tools - Constraint Manager** to open the constraint manager (CM). You will see the window shown in the image below.



The constraint manager has a lot of rows and columns that are essentially spreadsheet files placed into various folders called 'worksheets'. Don't worry about the detailed structure for now, as we will understand sheets, rows, cells and so on throughout the guide.

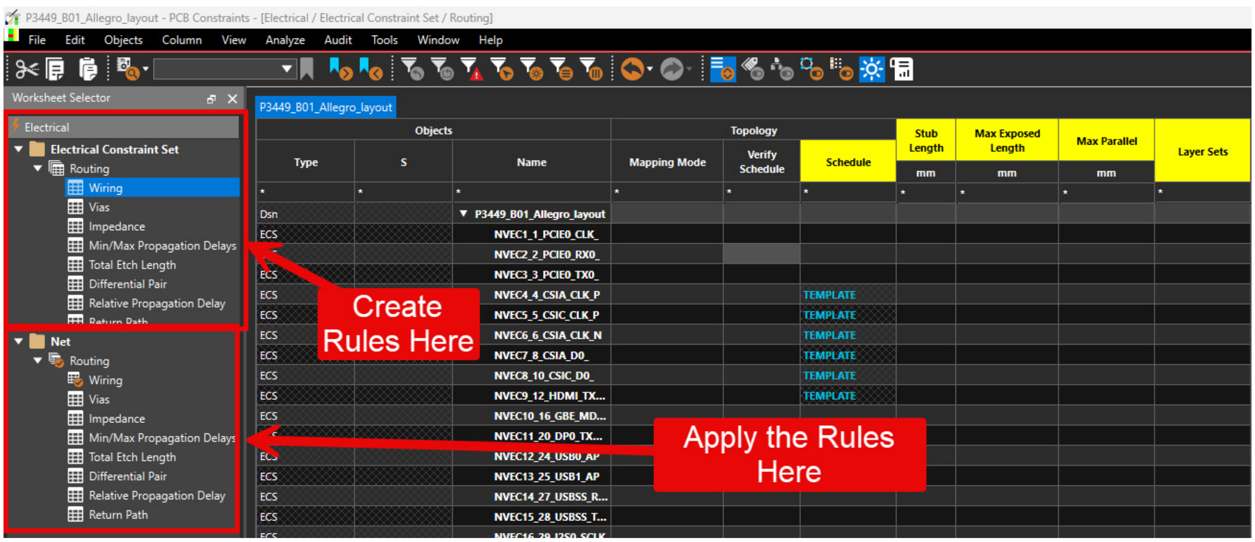
Understanding How the Constraint Manager Works

The Constraint Manager can be confusing at first glance. How do you know which constraints to set up?

The Constraint Manager uses the following method to apply constraints: First, you set up rules (we'll use 'rules' and 'constraints' interchangeably throughout this guide) in one part of the tool, then you apply those rules selectively to different nets, groups, and classes of nets.

For example, let's say we want to create Electrical rules that can be applied to any net, group of nets, or net class.

In the CM, you would first set your rules in the Electrical Constraint Set (ECS) section of the tool (see below).



At first glance, this method may seem redundant or unnecessary. Why not simply identify the objects you want to apply rules to first, then define your rules for those objects?

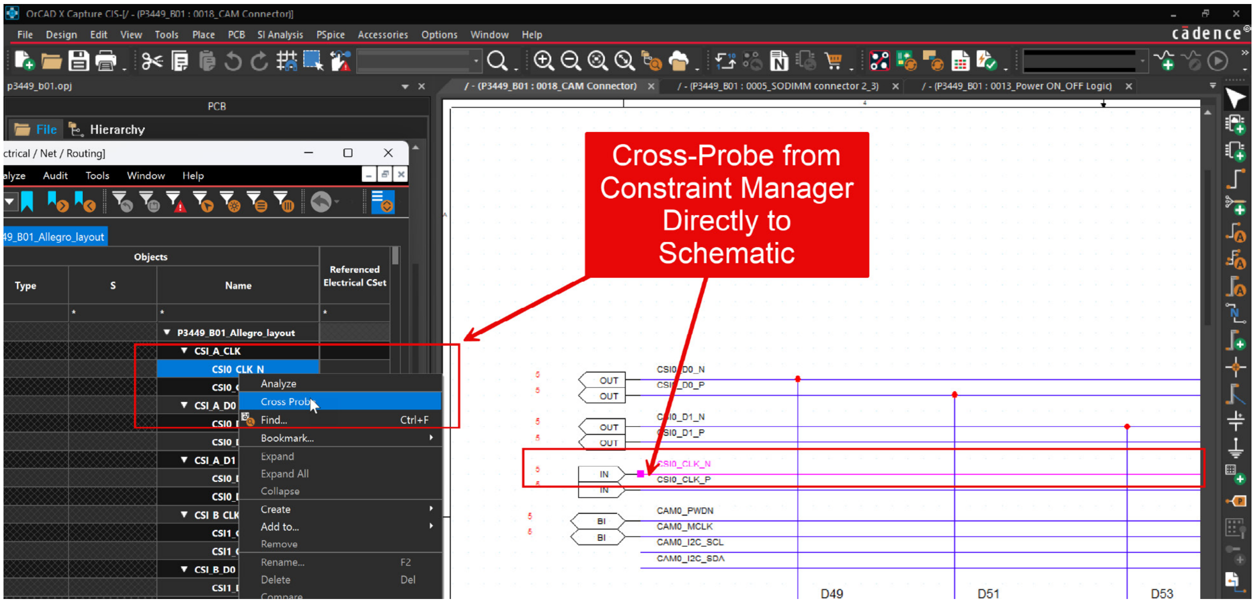
The issue with that approach is that you'd need to manually track all your rules for every object in a list and worry about prioritizing them correctly. Moreover, if you overlook an object or relationship, you could face significant problems later. By using this modular and categorical approach to constraint management—keeping rules separate from what they're applied to—, you gain flexibility, reduce the mental burden of tracking specific rules for specific objects, and can create blanket rule sets and categories.

As you'll see later, you can still apply specific rules when necessary. This approach to constraint management is incredibly robust, efficient, and flexible. If you need to change a rule for entire groups of nets, you can do so simply by modifying the rule itself or swapping out a rule created in the Constraint Set section.

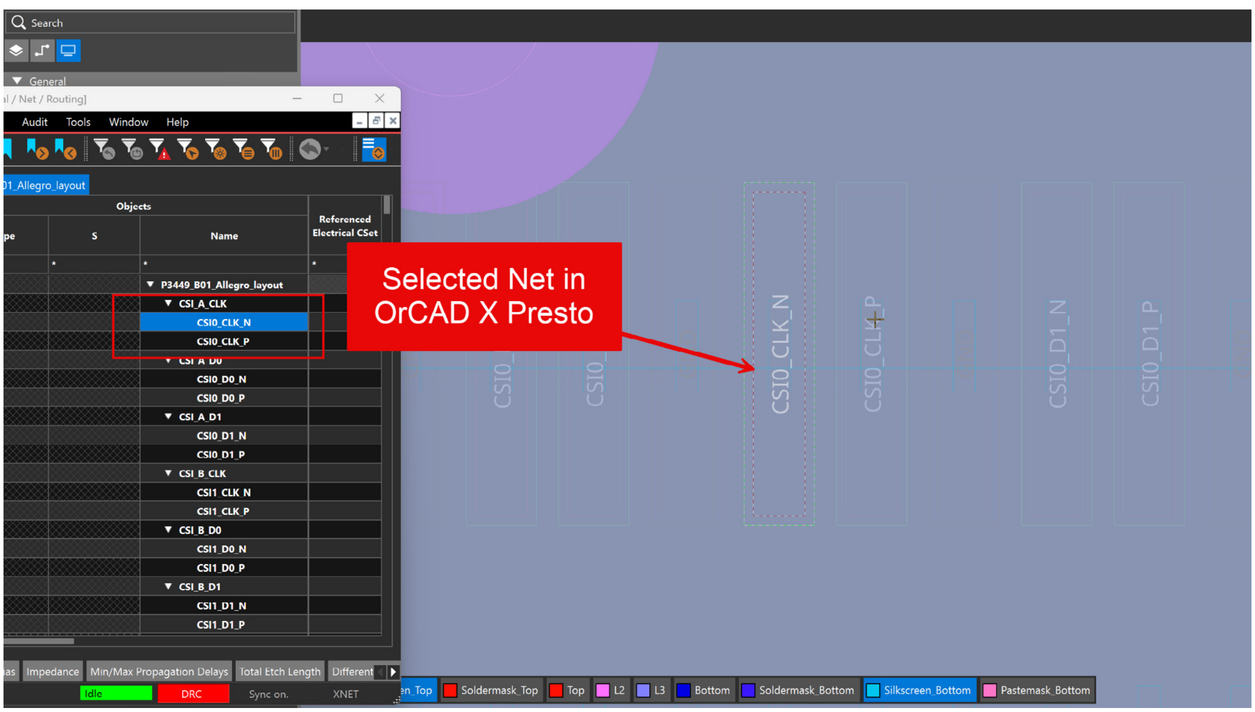
Even if nets change through PCB and design updates, you can maintain the same rules and apply them to the new nets, or incorporate the new nets (along with their changes) into existing rules. The flexibility and power of this approach make it the current gold standard for rules and constraints management.

Another powerful feature of the CM is the ability to locate your nets on your schematic or PCB directly from the constraint manager.

With the CM open in Presto and the schematic open in Capture, you can right-click a net and choose Select. Presto and Capture will then highlight the net in pink for you, as shown below.



The net and connected pins get highlighted in Presto as well.



Types of Constraints

In PCB design, constraints are crucial for ensuring the final product's functionality, reliability, and manufacturability. The main types of constraints are electrical, physical, spacing, manufacturing, and high-speed design constraints. Each domain addresses specific aspects of PCB design and often interrelates with others. Let's explore these domains and their importance:

Electrical Constraints

Electrical constraints focus on maintaining signal integrity, controlling impedance, and managing power distribution. These constraints are vital for ensuring proper circuit functionality and preventing issues like signal degradation or electromagnetic interference. Some key areas managed by electrical constraints include:

- Wiring topology (e.g., for DDR3 or T-branch configurations)
- Impedance control
- Signal timing and propagation delays
- EMI management
- Power integrity

Physical Constraints

Physical constraints deal with the tangible aspects of PCB design, including component placement, board dimensions, and layer stack-up. These constraints ensure that the PCB can be physically manufactured and assembled while meeting performance requirements. Examples of physical constraints include:

- Board outline and dimensions
- Component placement rules
- Layer stack-up definition
- Differential pair geometry
- Via types and usage

Spacing Constraints

Spacing constraints define the minimum distances between various elements on the PCB, such as traces, components, and board edges. These constraints are crucial for preventing short circuits, reducing electromagnetic interference, and ensuring manufacturability. Key spacing constraints may include:

- Trace-to-trace clearance
- Component-to-component clearance
- Trace-to-board edge clearance
- Pad-to-pad spacing

Manufacturing Constraints

Manufacturing constraints ensure that the PCB design can be produced using available manufacturing technologies. These constraints help prevent issues during fabrication and assembly, reducing costs and improving yield. Some manufacturing constraints include:

- Minimum trace width and spacing
- Drill sizes and tolerances
- Solder mask and silkscreen clearances
- Copper pour rules

High-Speed Design Constraints

High-speed design constraints are specific rules for managing signal timing, crosstalk, and other issues in high-frequency circuits. These constraints are critical for maintaining signal integrity in modern, high-speed designs. Examples include:

- Controlled impedance routing
- Length matching for differential pairs
- Via stitching for return paths
- Signal rise time management

Understanding these constraint domains provides a foundation for effectively using the constraint manager. In the next section, we'll explore how to organize nets using net classes, net groups, and constraint regions, which are essential for applying these constraints efficiently in your PCB designs.

Understanding Net Classes, Net Groups, and Regions in PCB Design

In PCB design, net classes, net groups, and regions are powerful tools for organizing and managing design rules. Let's explore each concept and their applications.

1. Net Classes

Definition: A net class is a group of nets that share similar electrical constraints within a specific domain (Physical, Spacing, or Electrical).

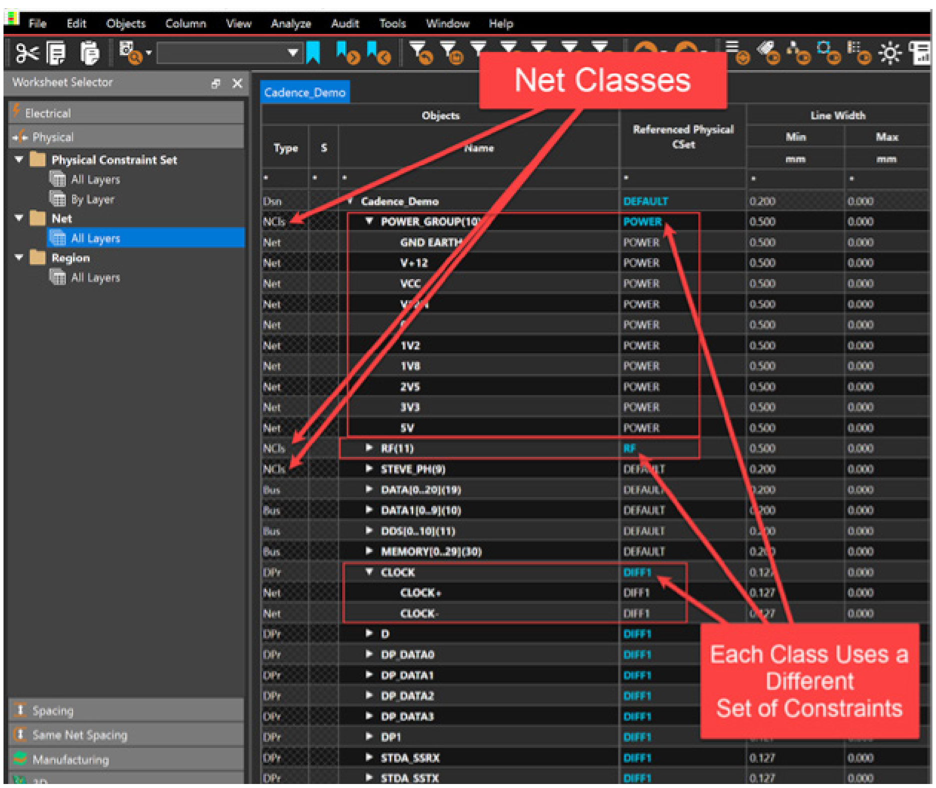


Diagram showing different net classes (e.g., Power, Signal, Ground) with their specific rules applied

Application: Use net classes when you need to apply specific rules to a group of nets within a particular domain.

Benefits:

- Simplifies rule application for similar nets
- Allows for domain-specific constraints

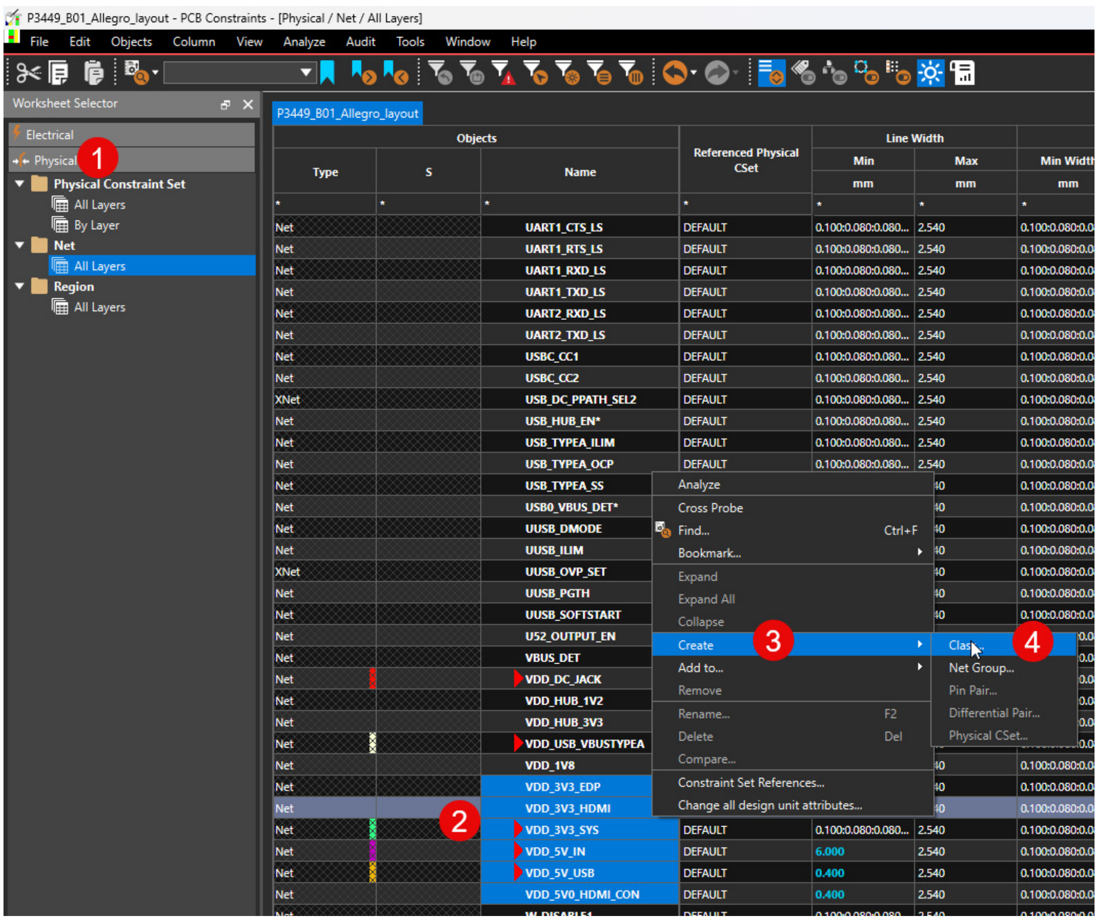
EXAMPLE - CREATING A NET CLASS

Here's the real benefit of using net classes. Let's say you know you need 2 Amperes going through any of the power traces in a design (VDD_5V_USB, VDD_3V3_EDP, and so on) at any given time.

We know that a 10 mil (0.254 mm) trace with 1 oz copper can withstand a 1 amp current at a 10°C temperature rise, so we decide on 10 mils for each of our power traces or a range of about 4 - 100 mils (0.1 - 2.540 mm). We have the option to set a rule to each trace width, but instead, we can set a rule to a class instead, then put those traces into that class, and have the 10 mil (0.254 mm) width rule applied to all of them at once. This is the power of Net classes.

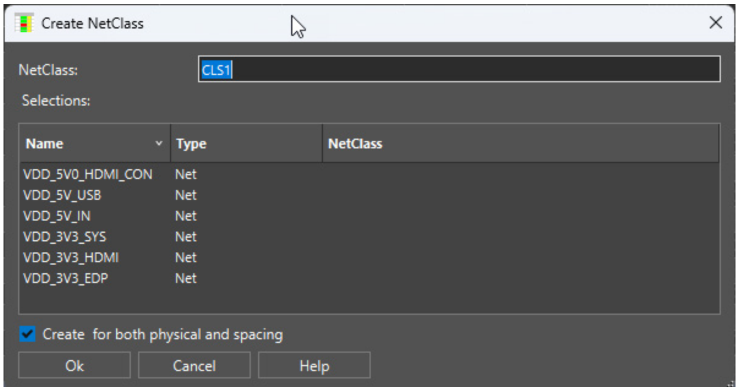
To demonstrate this, let's Group all power nets into a "Power" net class in the CM.

In OrCAD X Presto PCB Editor, open the CM using by clicking **Tools - Constraint Management**. The CM will appear as shown below.

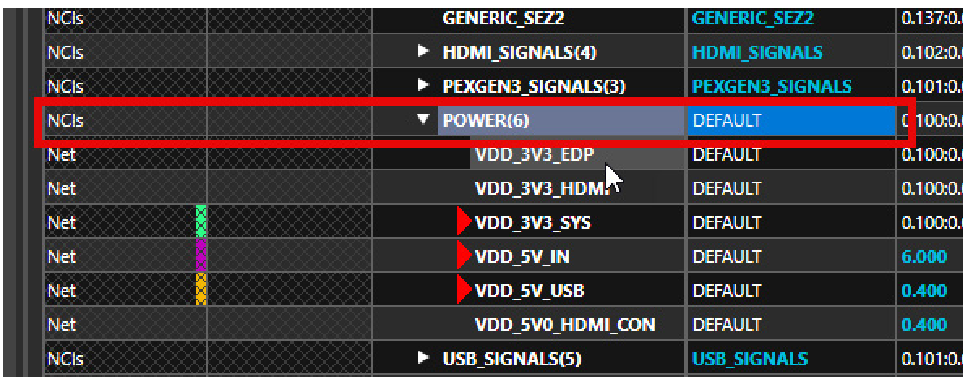


1. Go to the Physical Constraints Group (where we will set physical class definition for physical properties we want in our traces)
2. Under the Nets section, select All Layers from the dropdown item.
3. The spreadsheet will open up.
4. Select the cell that says VDD_3V3_EDP.
5. Hold the Shift Key.
6. Select the VDD_5VD_HDMI_CON cell. All the selected cells will be highlighted among them in blue.
7. On any of the selected blue cells, right-click to generate a pop up window.

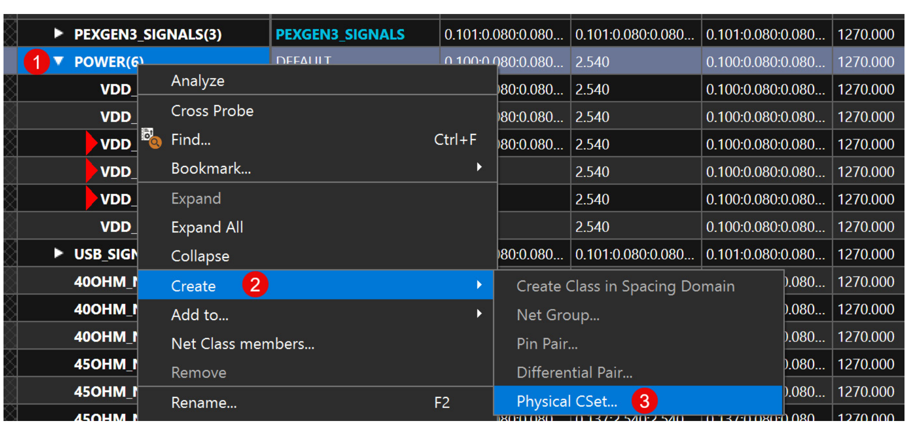
8. Choose **Create - Class**. The Create NetClass popup window will appear as shown below.



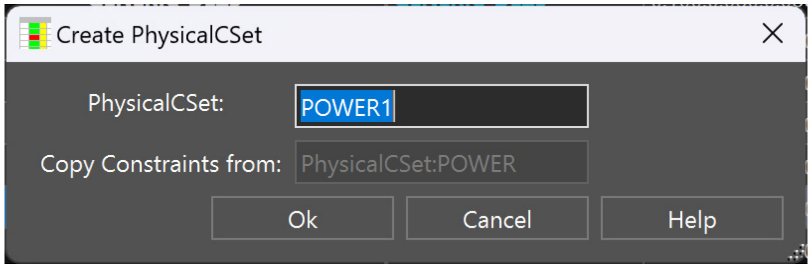
9. We want to come up with a name for the class of power traces, so let's rename the NetClass field from CLS1 to Power. Note how the names of the nets are shown in the list.
10. At the bottom of the window, keep the checkbox selected for *Create for both physical and spacing* because we'll want to add the right spacing for these nets as well, and click Ok.
11. Back in the CM Physical Nets Worksheet shown below, you can see the POWER category as a NetClass.



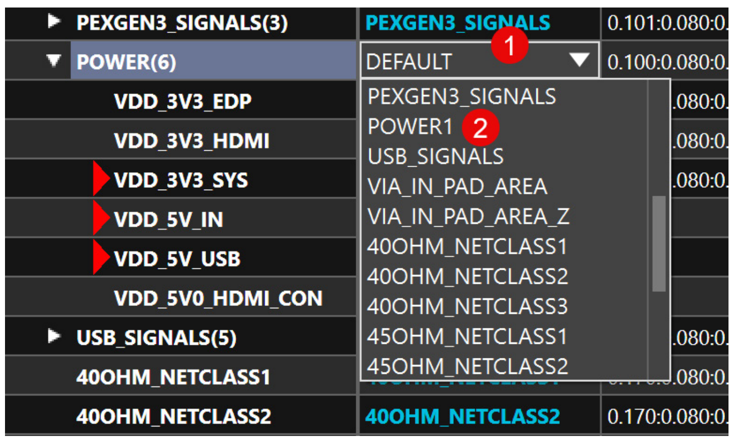
12. That's not the end of it though. We need to assign a trace width rule to that entire class, because right now it only has the default rules applied to it (shown in image above).
13. To apply the rule to the entire class of power traces, let's create a Power rule (called a Constraint Set).
14. Right-click the POWER(6) cell above (the net class you just created), then in the menu, choose **Create - Physical CSet.**



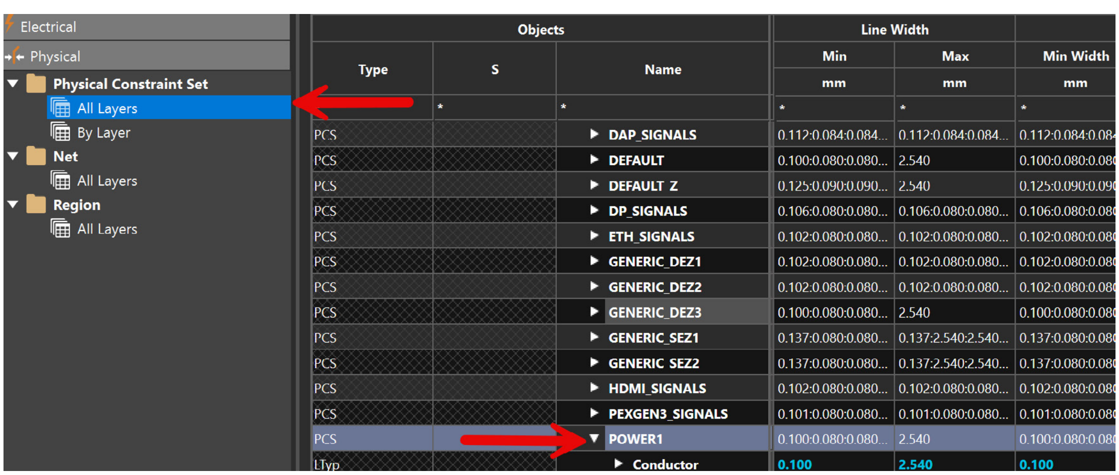
15. The Create PhysicalCSet window appears (seen below).



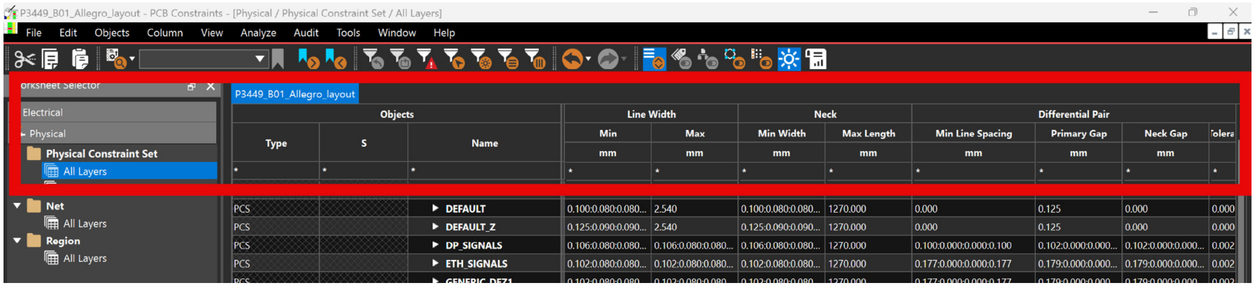
16. In the PhysicalCSet field, name it POWER1, then click OK. The window closes.
17. Next, we assign this POWER1 rule to this entire class by clicking the dropdown list to the right of the POWER(6) cell (click DEFAULT shown below), then select POWER1.

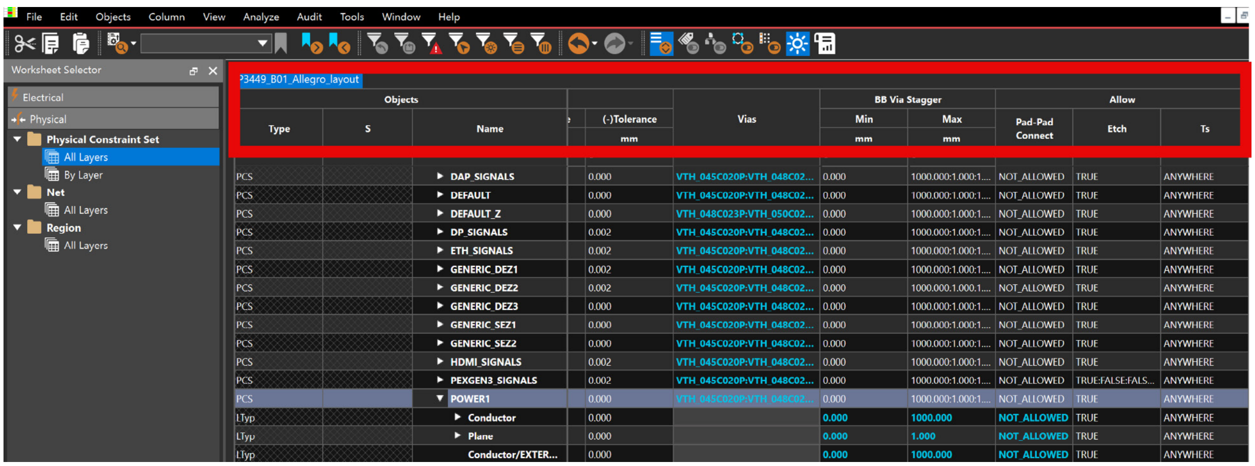


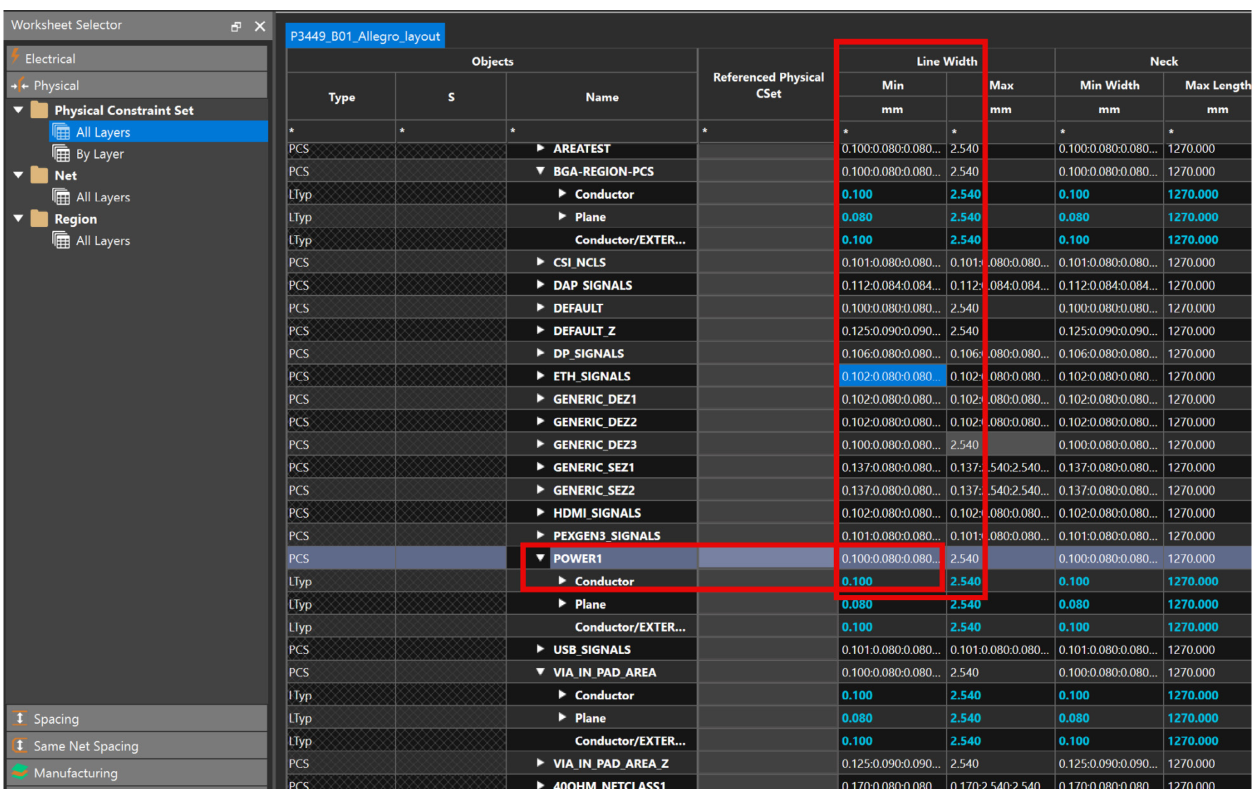
18. Now, at any time, we can go to the POWER1 Physical Constraint Set in CM and set any values we want to all those traces within the Power net class we created earlier.
19. To do the constraint update (see below), while still in the Physical worksheet in CM, choose **Physical Constraint Set folder - All Layers**. That will make the worksheet visible on the right.
20. Scroll down that worksheet to find POWER1. Expand it by clicking the triangle.



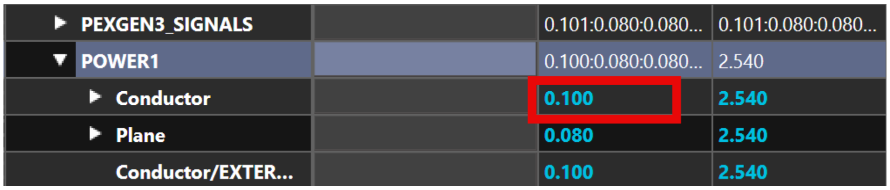
21. You will see all the options going right across the columns shown below, like Line Width, Neck, Differential Pair, Vias (BB Via Stagger), and Allow.





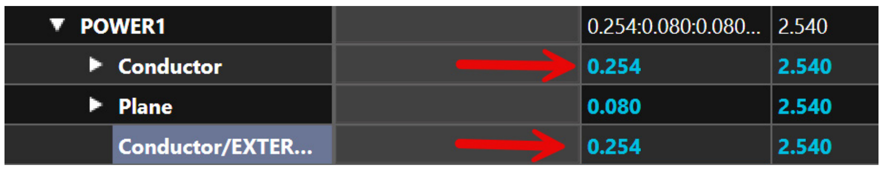


22. Look at the cell named **Conductor** in the image above, then to its right, click on the field value in the column named Min (found under the Lined Width column).



▶ PEXGEN3_SIGNALS		0.101:0.080:0.080...	0.101:0.080:0.080...
▼ POWER1		0.100:0.080:0.080...	2.540
▶ Conductor		0.100	2.540
▶ Plane		0.080	2.540
Conductor/EXTER...		0.100	2.540

23. Now highlight the value there and change it to whatever your minimum trace width needs to be for any power trace (10 mils, or 0.254 mm in this example).



▼ POWER1		0.254:0.080:0.080...	2.540
▶ Conductor		0.254	2.540
▶ Plane		0.080	2.540
Conductor/EXTER...		0.254	2.540

24. Notice the units are listed under the **Min** column header at the top.

Now, the Physical Constraint Set (POWER1) that you applied to your Net Class (POWER) can be changed at any time to set all traces in the power class to the desired width.

Impacts:

- Power Consumption - Easy to specify minimum trace width to ensure proper current carrying capacity, regardless of the net, as long as it's in the right class or a ground/power net.
- Signal integrity - Easy to specify impedance on any traces within the same class, regardless of protocol.
- Efficiency - No need to individually set trace widths. Apply one rule to many nets and objects all at once by capitalizing on classes for physical properties.

However, while net classes are very powerful, we may not always want to set the same physical or electrical properties to all nets in a protocol for instance.

That's why we also need to be able to set properties and rules by groups of nets that may not have the same physical or electrical properties. In the next section, we will address the addition of net groups.

2. Net Groups

Definition: A net group is a collection of nets that are common (usually in functionality and operation) across all domains.

Application: Use Net Groups when you need to apply general rules across multiple property domains, i.e., even if traces have different physical and electrical properties and constraints.

In most cases in PCB design, we have nets and traces that can't carry the same widths or impedances, but they're nonetheless part of the same protocol or device.

In other words, devices can carry nets that require different physical and electrical properties.

When this happens, we still want to remain organized, so we introduce nets that belong to a specific group, regardless of their physical or electrical properties.

In this section, we will:

- Create a Net Group
- Distinguish between Net Classes, Net Groups, and their benefits
- Understand why both Net Groups and Net Classes are important

We will first create the net group and then a general spacing rule, and then we will apply that general spacing rule to that net group, even though some of the nets are part of their own classes and have their own physical and electrical properties.

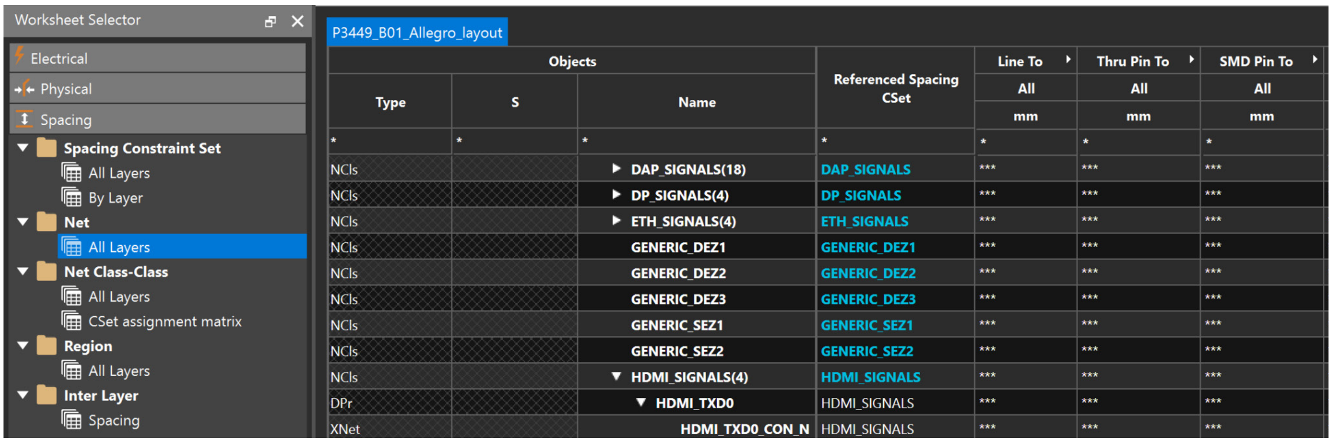
Benefits of Net Groups:

- Provides a higher-level organization of nets
- Allows for consistent rule application across domains

EXAMPLE - CREATE A NET GROUP

Let's say we want to group all nets related to a specific interface (e.g., USB) because we want to apply common rules, like routing topology and spacing among all of them. This is where we create the Net Group.

1. With OrCAD X Presto PCB Editor open, select **Tools - Constraint Manager** from the toolbar menu. The CM will appear.
2. Go to the **Spacing - Net - All Layers** worksheet (shown below).



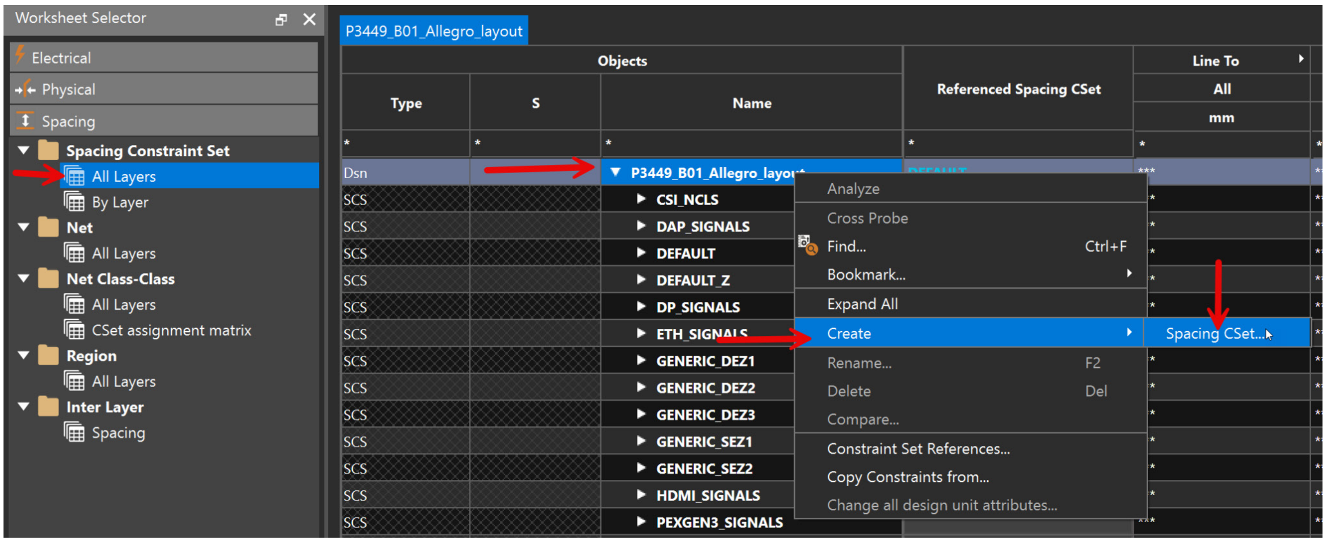
3. Scroll down the spreadsheet and select the 'USB_SIGNAL(S)' cell. This is a defined group for all USB signals, a perfect example of a group. But let's go a step further, because the signals have the same Spacing Constraint Set already.

Let's make a group called USB_All, which includes some USB C nets.

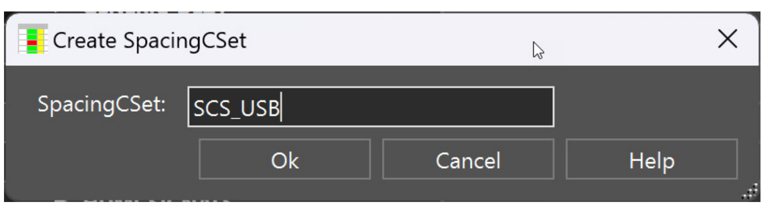
4. Scroll down to USBC_CC1, select it, then select the rest shown in the image below, down to USB_TYPA_SS (see below).
5. With those nets selected, they have different impedance profiles if put in their own classes, but can still be part of the USB_ALL group.
6. So right-click any of the highlighted blue cells.
7. Choose **Create… - Net Group…**
8. A new window named Create NetGroup appears. It has the list of nets being considered for this new net group we're about to create.
9. In the NetGroup field, type UBS_ALL.
10. Click Ok. The window will disappear.

Now, you can make any kind of rule (e.g., a spacing rule) to apply to that group of nets. Let's create and apply that spacing rule. Let's say we want all USB nets, whether power or signal, to have a certain voltage withstanding by keeping them far enough away from other objects that might get to that high a voltage (10 mils/0.127 mm of clearance is sufficient for 500 V withstanding on the PCB surface according to IPC-2221B, Table 6-1). So, let's set a rule for 10 mils (0.254 mm) minimum spacing in the design.

11. With the CM still open, go to the **Spacing Constraint Set - All Layers** section.
12. Right-click the cell in the Dsn row named **P3449_B01_Allegro_layout.**



13. From the dropdown menu, select **Create - Spacing CSet...**.
14. The Create SpacingCSet window appears.



15. In the SpacingCSet field, name it SCS_USB, then click Ok.

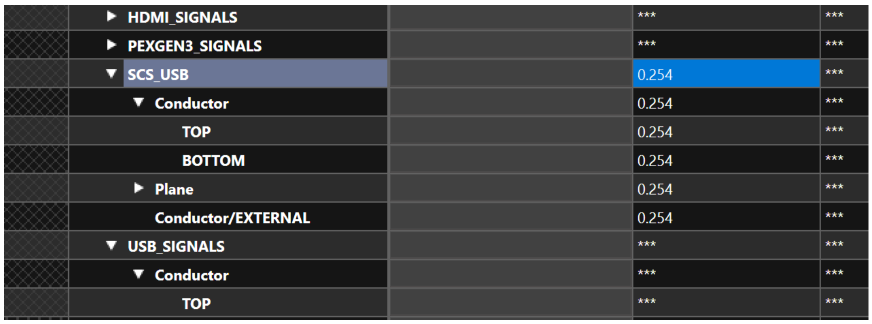
Tip: SCS means SpacingCSet, so we can distinguish that constraint set from others such as physical CSets (PCS) and electrical Csets (ECS).

16. You will see your spacing constraint rule set below.

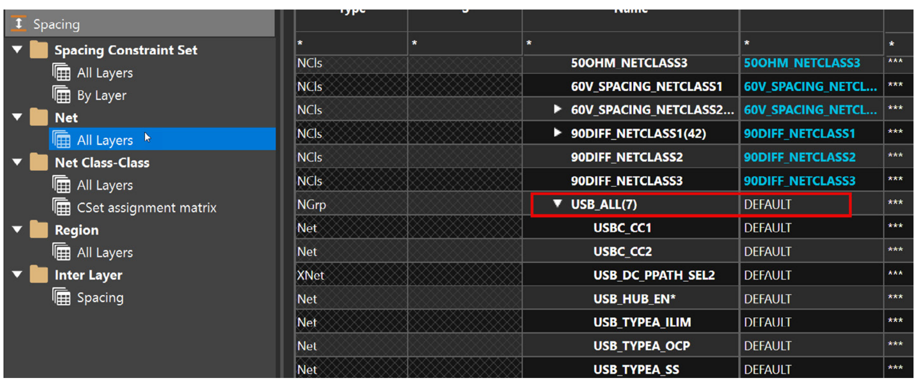
All the columns in this spreadsheet have some kind of spacing rule for one object to another object. For instance, the column that says "Line To" - then "All" below means this column sets the space from the edge of a 'line' (this is a trace in OrCAD X Presto PCB Editor) to all other objects.

That means whether it's a via, another trace edge, or a mounting hole, we want that gap to be a certain distance from the edge of the trace to the edge of the next object.

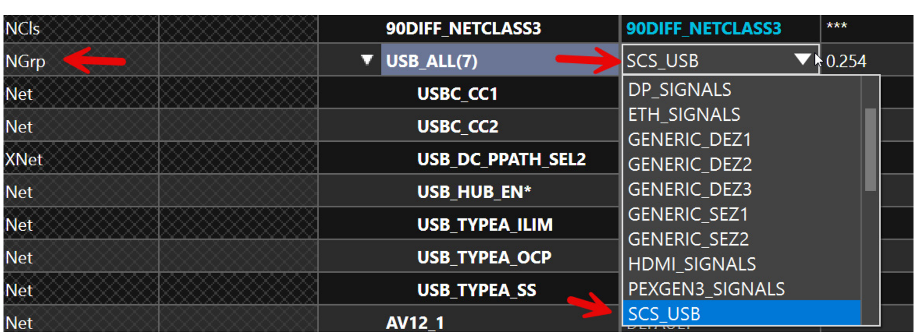
17. Let's set this rule to 10 mils (0.254 mm) by clicking on the *** field, then typing 10 (or 0.254), then hitting Enter on your keyboard or Tab to populate that field.



18. Notice that the values in that field show up in all the rows below SCS_USB. This means that there are conductor layers (basically copper layers) named TOP layer and BOTTOM layer. For all the traces and conductors on those layers, the spacing rule for any 'lines' (traces) on those layers is 0.254 mm from edge to other objects. Now, this set of rules (Spacing Constraint Set) can be applied to any object or group of objects we want.
19. Let's go back to the Net Group we created in the Spacing - Net - All Layers spreadsheet, then scroll down to 'USB_ALL'.



20. Now the moment of truth. Instead of the DEFAULT rules being applied to the USB_ALL net group, we will apply the SCS_USB (Spacing Constraint Set, USB).
21. Click the field that says DEFAULT, then you will see all the spacing constraint sets drop down and become available. Also notice how the Net Group we created is labeled as **NGrp**.



22. Choose the SCS_USB Spacing Constraint Set, and then it will be applied to the entire group.

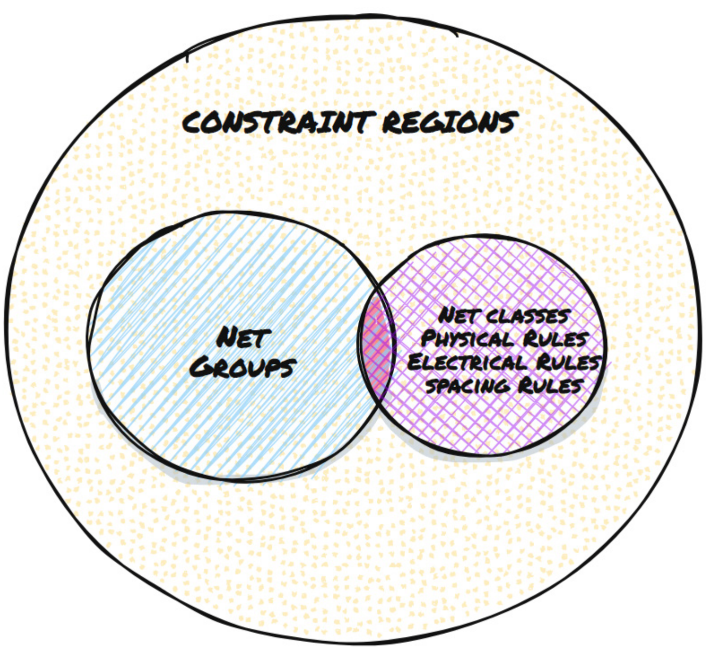
▼ USB_ALL(7)	SCS_USB	0.254
USBC_CC1	SCS_USB	0.254
USBC_CC2	SCS_USB	0.254
USB_DC_PPATH_SEL2	SCS_USB	0.254
USB_HUB_EN*	SCS_USB	0.254
USB_TYPEA_ILIM	SCS_USB	0.254
USB_TYPEA_OCP	SCS_USB	0.254
USB_TYPEA_SS	SCS_USB	0.254

The constraint mapping is already saved immediately in the Constraint Manager, so there is no need to save the constraints. At this point, however, you should save your design. Here is the impact on what we just did - applying spacing constraints (10 mil or 0.254 mm spacing to the power nets).

Impacts:

- Even though we may have traces with different physical properties, like the ones in the USB_ALL group (for example, USBC_CC1 and 2 need a 50 Ohm single ended impedance, while other traces do not), we can group them together for any reason, to apply rules on the entire group despite physical and electrical property differences.
- The creation of Net Groups bypasses the limitations of only being able to apply physical and electrical properties to some nets at a time and being forced to work within only those rules.
- The Net Group now allows us to overcome the limitation of not being able to assign a rule to an entire set of nets regardless of the class they belong to. This is the benefit of Net Groups - more opportunities and ways to organize your constraints to handle most any design.

The image below explains graphically how this looks.

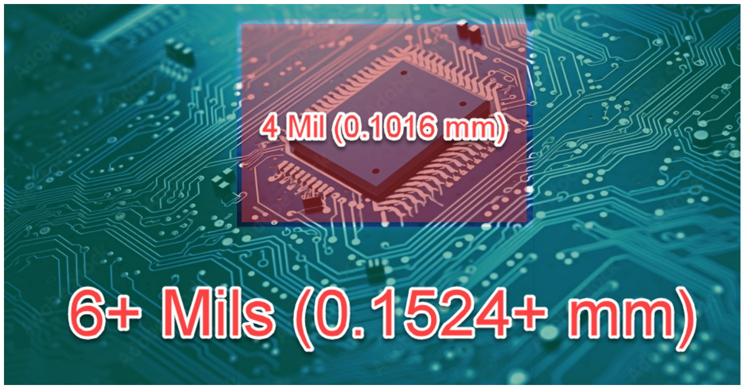


Venn diagram showing how a net group spans across different domains (Physical, Spacing, Electrical)

So the understanding of the Venn diagram is that Net Groups can include Net Classes, Physical, Electrical and Spacing rules and constraints. Net Groups can also apply constraints to various groups. Finally, all rules, groups and classes are found within a constraint region. What is a region? In the next section we will explain constraint regions for PCB design.

3. Regions

While we can set rules for any of our nets whether by class or group, oftentimes we need yet another set of rules for specific areas of a PCB. For example, look at the traces on the PCB below.



Top view of a PCB layout with different regions highlighted and their specific rules listed

Definition: Regions are specific areas on the PCB where unique design rules are applied.

Application: Use regions when you need to apply different rules to specific areas of the board, regardless of net group, net class, or general rules on the PCB.

Let's say the traces found in the green area must not be any thinner than 6 mils (0.1524 mm) to save on costs and because we don't have a particularly dense board. However, the ball grid array (BGA) chip on the PCB (in the red region of the image above) has such fine pitch pins that 6 mil traces are simply too thick to route the pins.

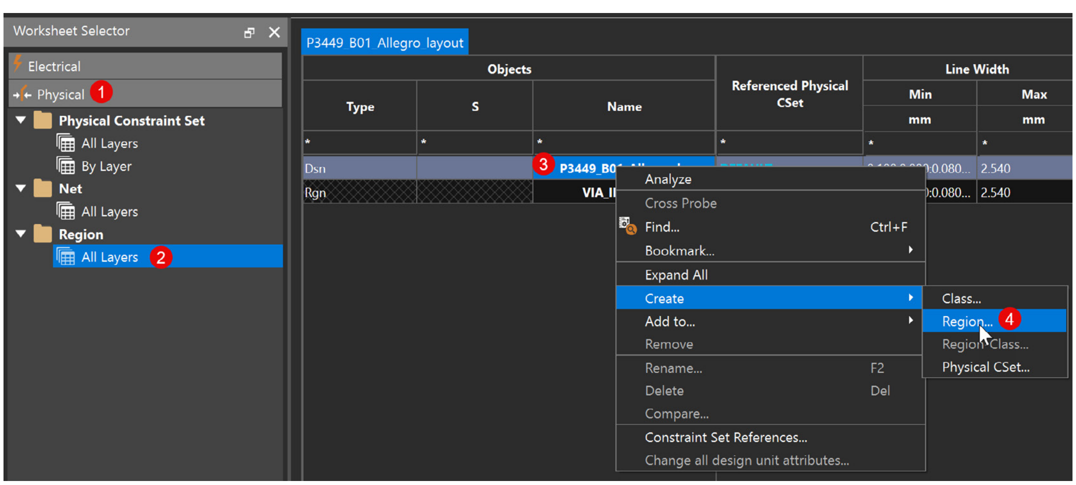
So what is the solution? Make the traces thinner in that BGA chip area. In addition, we must set this rule for all layers of the PCB found underneath this BGA device.

Those layers would be the top, middle, and bottom conductor (copper) layers of the PCB. Also, we need to allow for tighter spacing in that region as well to avoid violating general spacing and trace width rules for the entire design. Let's look at the benefits of constraint regions.

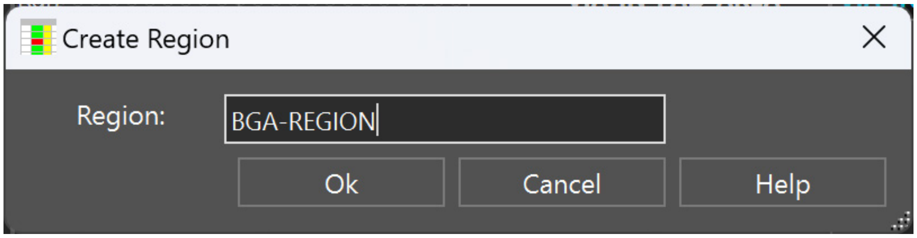
Example: Define a high-density region containing a BGA device with tighter spacing and trace width rules compared to the rest of the board.

REGION PHYSICAL CONSTRAINT SET

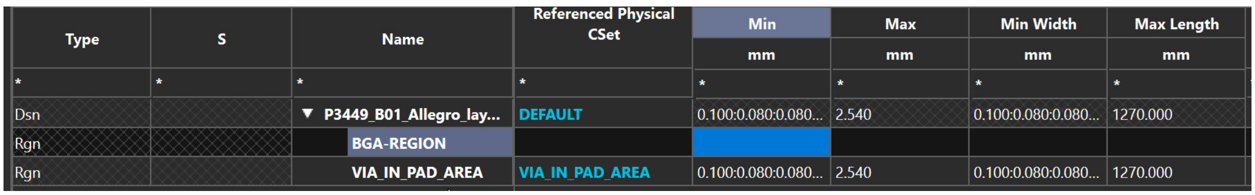
23. Open the CM in OrCAD X Presto PCB Editor by going to **Tools - Constraint Manager.**
24. Shown in the image below, go to the Physical Worksheet/section on the left, then select **Region - All Layers.**



25. Right-click on the Dsn row's cell name, then in the pop-up menu, choose **Create - Region**. You will get the Create Region window below.



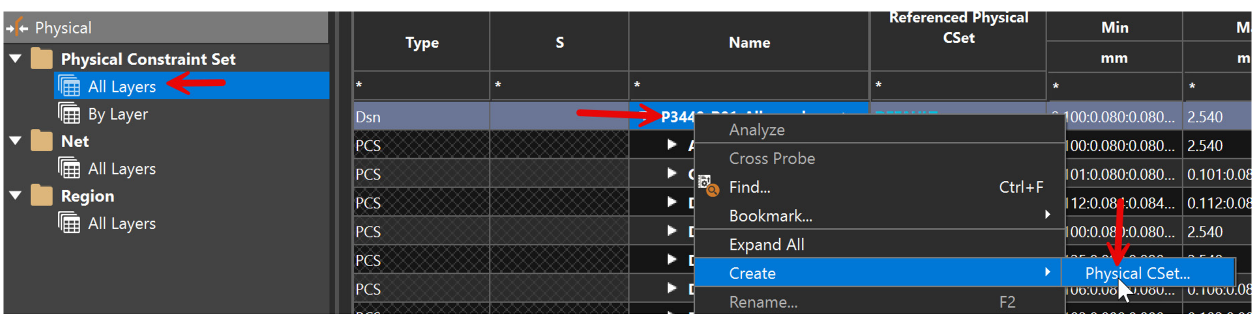
26. Name the Region field BGA-REGION. Click Ok.
27. The window will disappear and show the added region below within the CM.



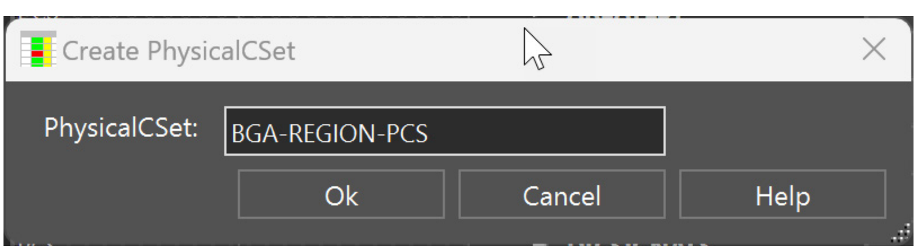
28. Now, we have the option to manually fill in our desired values in the BGA-REGION row of cells for each column. However, this is suboptimal. We want to manage multiple regions with one change if we want, so instead, like before, we will create a Constraint Set that can be applied to any object. That way, no matter how many objects we apply the constraint set to, we only have to change the constraints once to affect all nets, spacing, and in this case, regions.

Note: Constraint Regions can only be created in the Physical and Spacing Constraint Set domains, not in the Electrical domain within Constraint Manager.

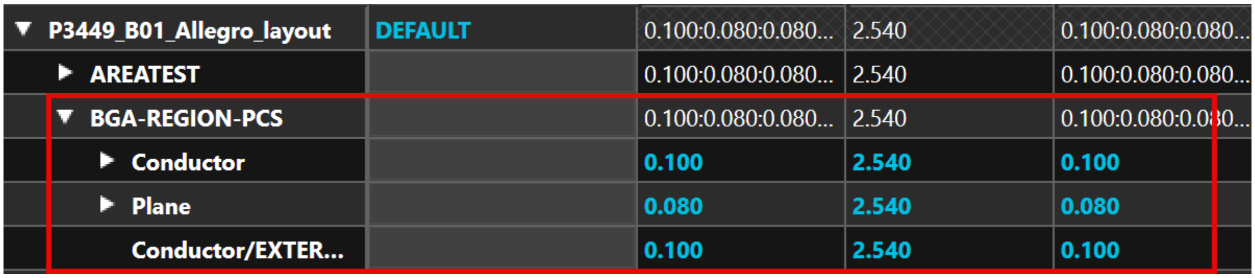
29. Let's set the physical constraint set. While still in the Physical section in CM, choose All Layers - The Dsn named cell in the top row of the spreadsheet, right-click it, then choose Create - Physical CSet....



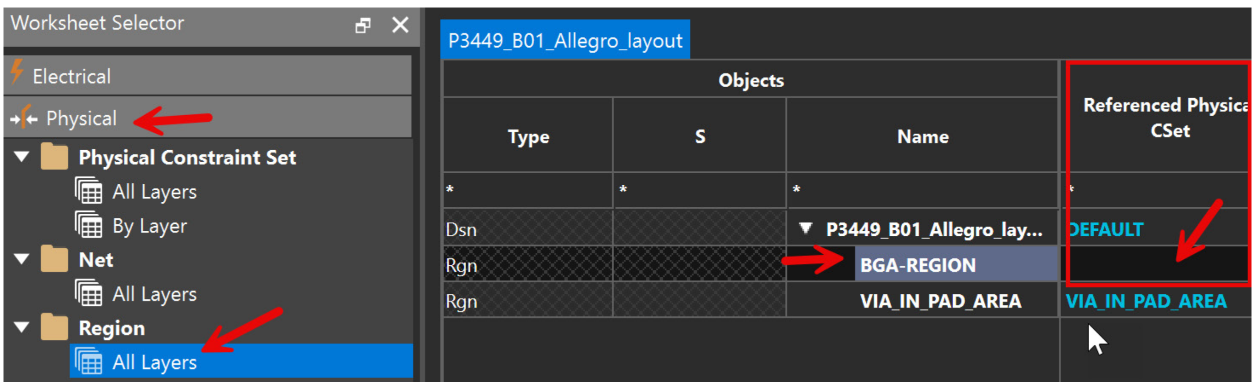
30. The Physical Constraint Set window will open.



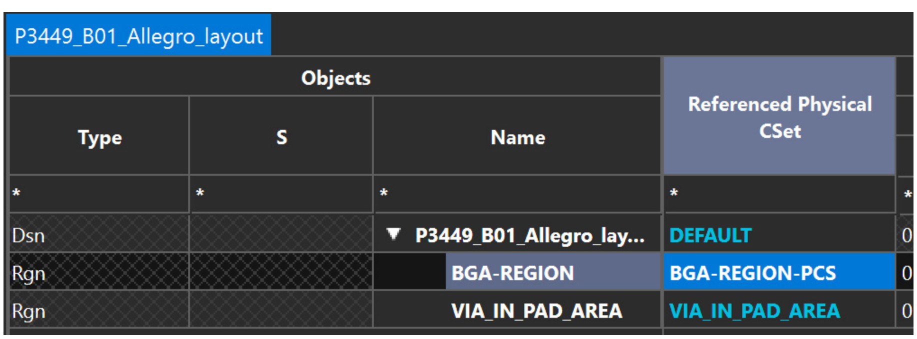
31. Give it a name in the PhysicalCSet field (e.g. BGA-REGION-PCS, for Physical Constraint Set to distinguish it from the spacing rules we will create for the BGA Region).
32. Click Ok. The window will disappear. The Physical CSet you created will appear (see below).



33. The final step is to apply this BGA-REGION-PCS Constraint set to our newly created Physical Region (BGA-REGION).
34. Go back to the **Physical - Region - All Layers Worksheet** (see below).



35. In the image above, notice the **Referenced Physical CSet** column to the right of the 'BGA-REGION' field. Click that cell and select the Physical CSet we just created, BGA-REGION-PCS.



36. Now we have our physical rules applied to the Physical region!

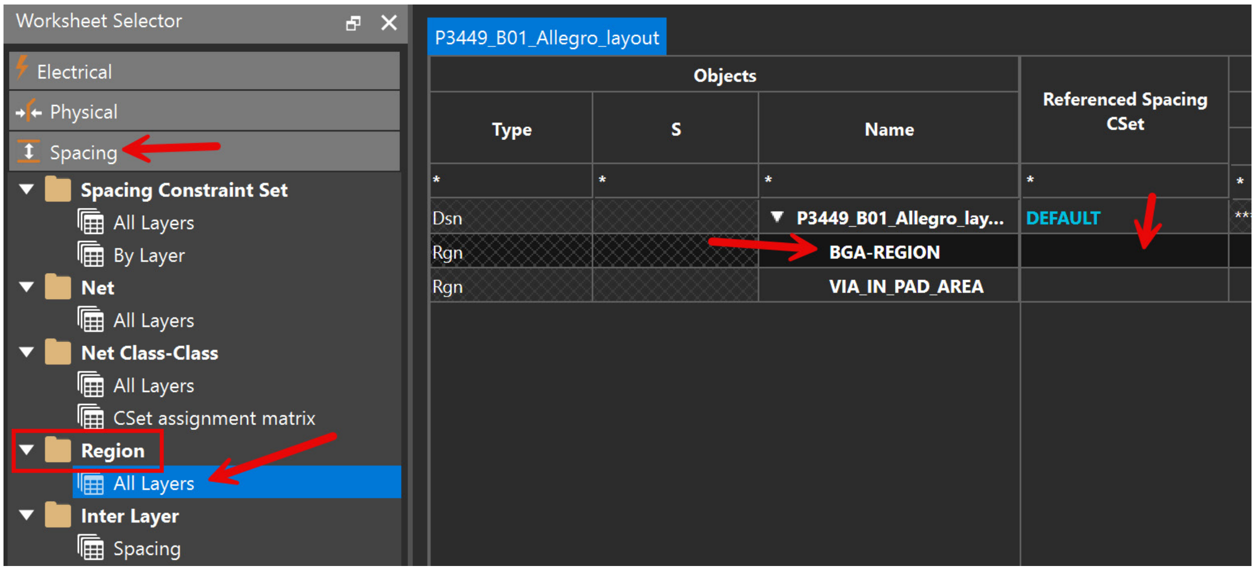
Notice that the widths of the Conductor row are already 0.100 mm, which is lower than our 4 mil minimum requirement for conductor trace width in this region.

That is a satisfactory value, so let's set the spacing rules for the BGA region by again, first creating the region (but in the Spacing domain). Then we'll create a Constraint set specifically for that region and finally apply it.

REGION SPACING CONSTRAINT SET

In this section, we set the spacing constraints specific to a region of the PCB (namely, a BGA device) across all layers of the PCB.

1. Go to the CM section, **Spacing - Region - All Layers**, to pull up the worksheet shown below.

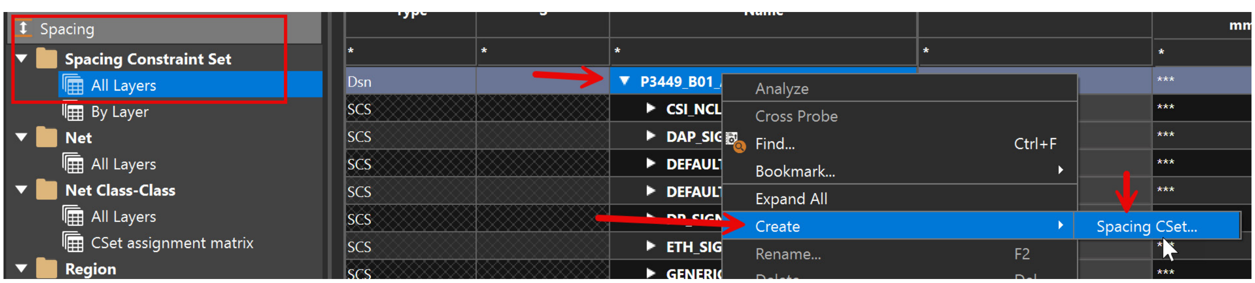


2. Notice we already have a BGA-REGION cell populated on the worksheet. In the cell next to it, under the column named Referenced Spacing CSet, click the cell.

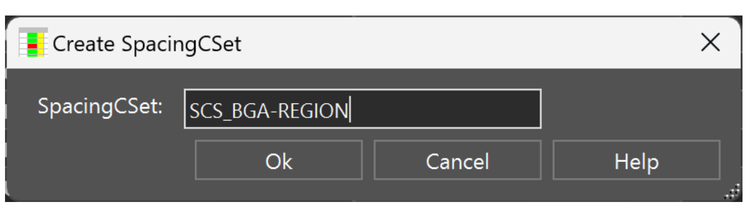
You get a dropdown showing the list of possible spacing constraint sets, so there is no surprise that our BGA-REGION-PCS doesn't appear since that's a physical CSet, not a spacing CSet.

3. Let's create the Spacing CSet, then come back later to apply it to this BGA-REGION.

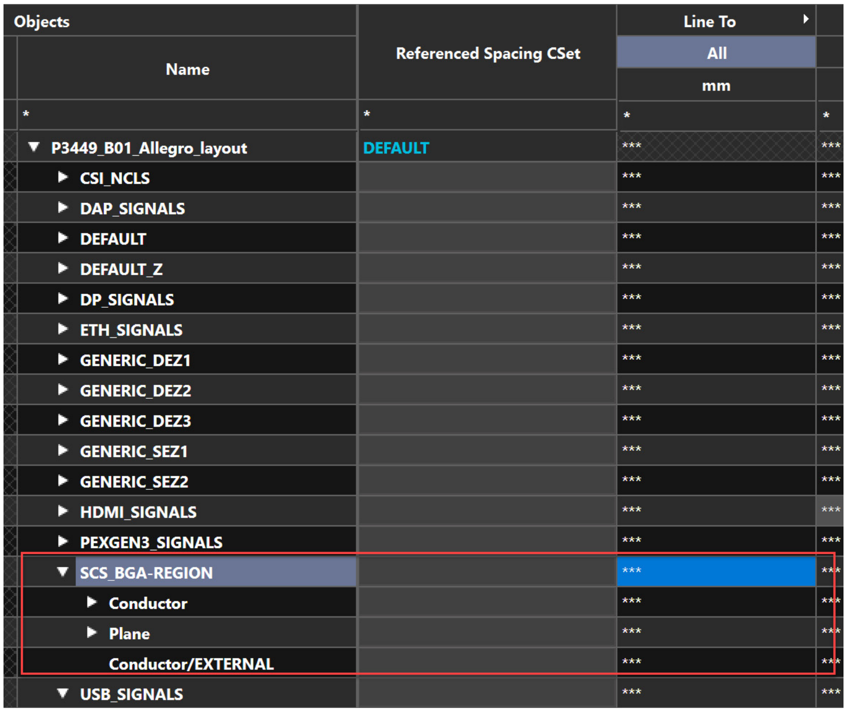
To make the spacing CSet while still in the Spacing domain in CM, click under **Spacing Constraint Set - All Layers**, as shown below.



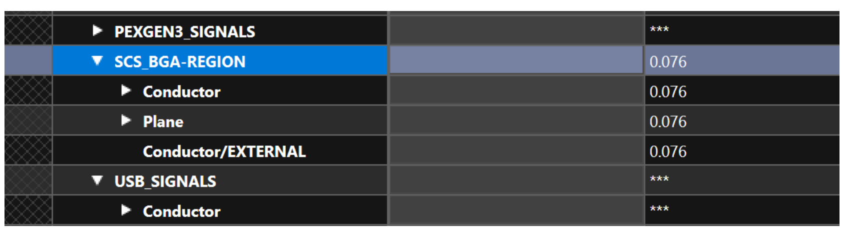
4. Right-click the first cell named **P3449_801** (in the Dsn row), then choose **Create—Spacing CSet.**



5. In the new window, type SCS_BGA-REGION (Stands for Spacing Constraint Set BGA Region). Click Ok.
6. The spacing constraint set (SCset) has been created and is visible on the worksheet.

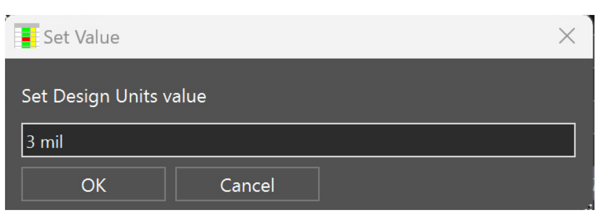


7. Let's set the value in the column **Line To - All (mm/mil)** to 3 mils by typing "3 mil" into the blue highlighted field (to account for neck mode for differential pairs and random scenarios we may run into while routing underneath the BGA). The value will change from *** to the correct value, and units (ours changed from mils to 0.076 mm) are shown below.



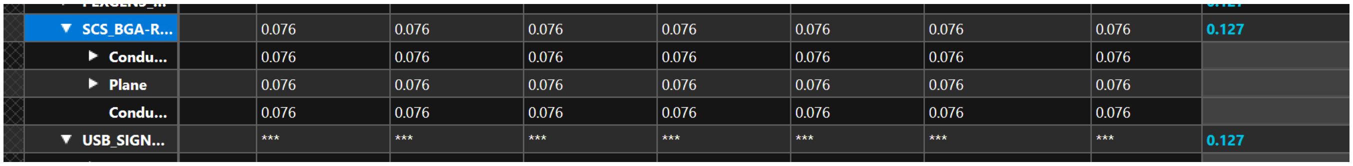
Tip: When you enter a value, you don't have to convert to mm or mils beforehand. Just type "3 mil" into the field, and the software will convert it to the appropriate units automatically.

8. We should also update all the column values to be at least 3 mils in spacing. However, that would be tedious. Luckily we can assign the same value to all columns and rows. Do that by right clicking the SCS_BGA-REGION cell, then choosing - Change all design unit attributes…. A **Set Value** window will appear.



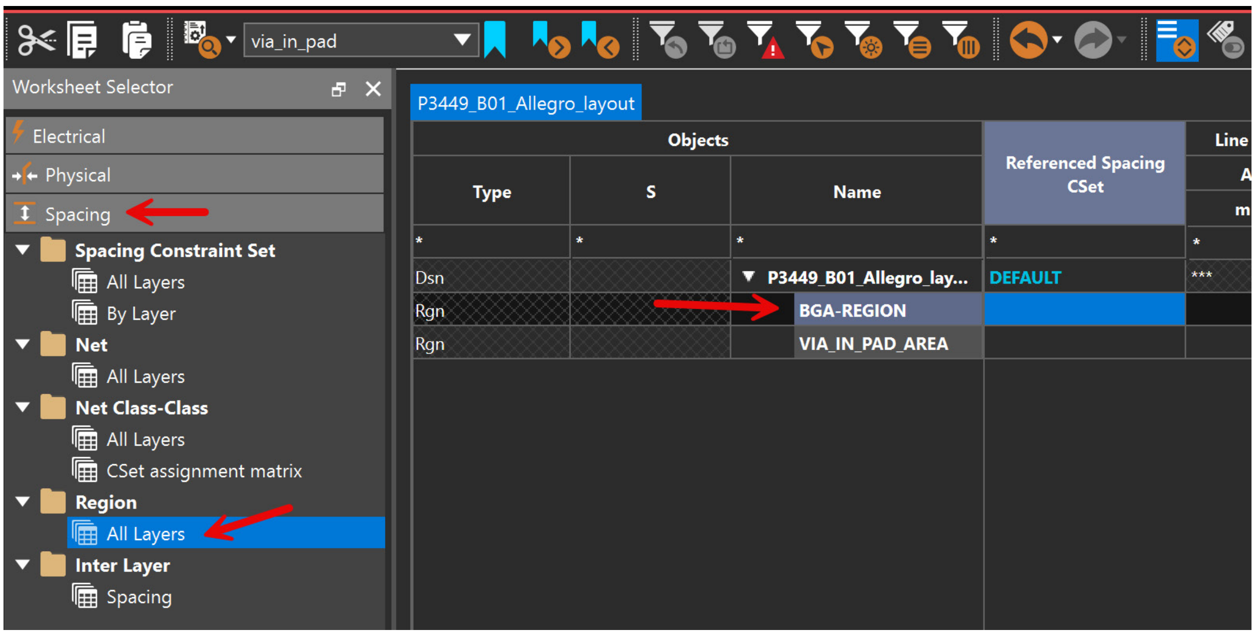
9. Enter '3 mil' (without the quotation marks). Click Ok.

10. If you scroll to the right, you will see all the fields populated, and the **Min BB Via Gap** value is already set (see image below).



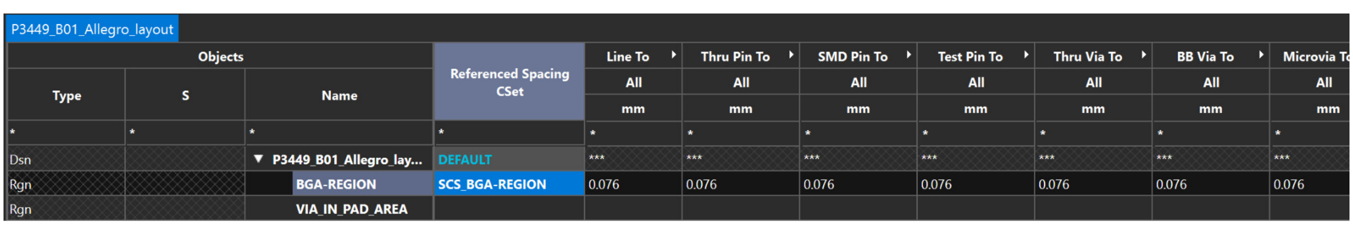
Now that the spacing constraint set has been created for any object in the BGA Region/area, we are ready to apply it to said region.

11. In CM, return to the left section **Spacing - Region - All Layers** to open the worksheet shown below.



12. Let's assign our new spacing constraint set to this BGA-REGION by clicking the cell in the column named **Referenced Spacing CSet** and choosing **SCS_BGA-REGION.**

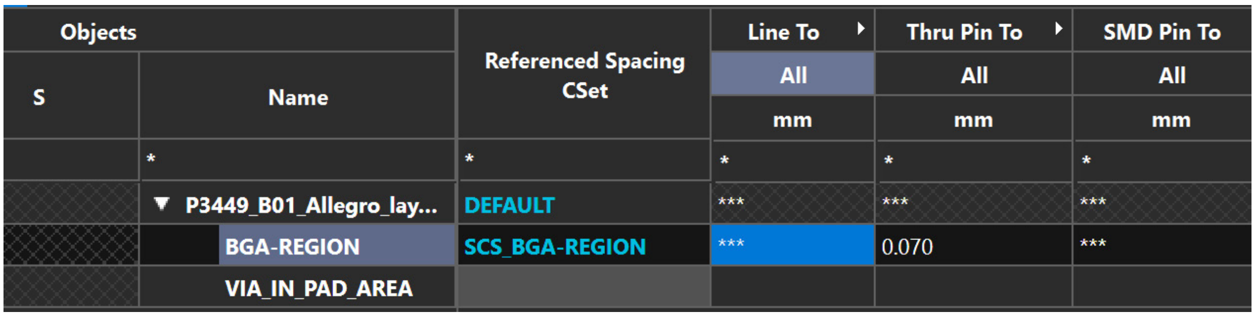
13. Notice that all the cells (values under every column) get populated with the spacing rule we set just earlier (3 mils = 0.076 mm).



MANUAL CONSTRAINT ENTRY VS. CONSTRAINT SETS

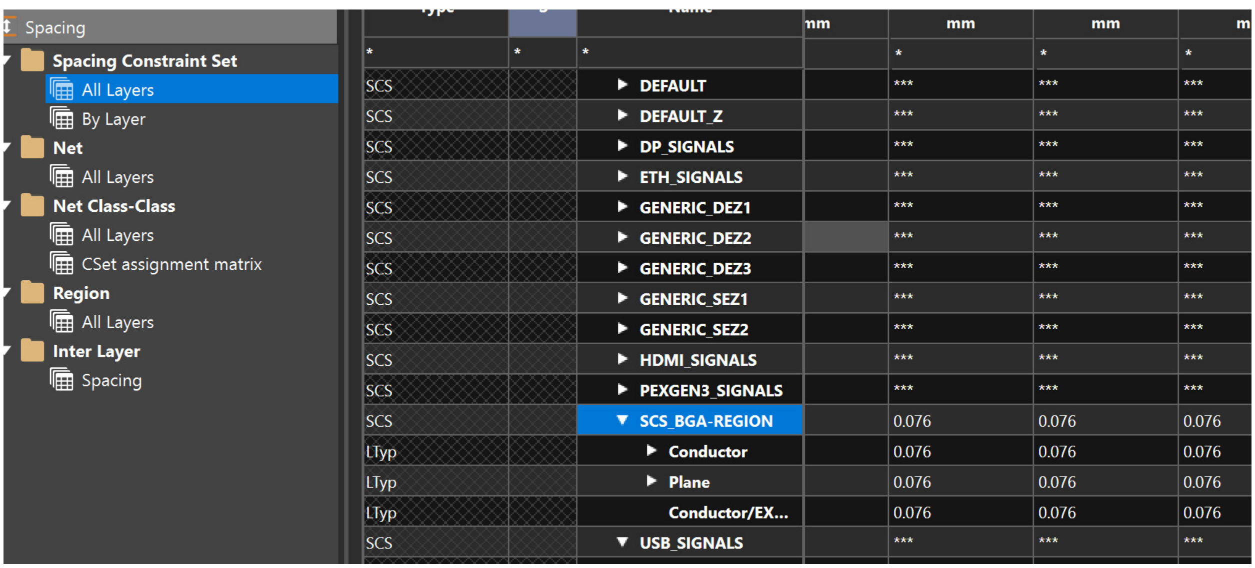
Sometimes you need a constraint value applied to one specific object (trace width, SMD pin spacing, etc.). In this part of the example, we will apply a constraint value manually and then examine the benefit of doing that versus using blanket constraint sets.

14. Enter 0.070 in one of the column cell values (e.g., under the column **Thru Pin To - All**). Notice how all the other cells go to ***'s. This is fine. There is no need to modify them either because they just indicate that not all the values within the constraint set are the same.



15. Now that I manually entered a new value (0.070 mm) for my **Thru Pin To - All** spacing cell, any time I use the BGA-REGION constraint region on an area of the PCB, it will apply that rule to that area of the PCB.

16. However, let's click on the original spacing constraint set for this BGA. Go back to **Spacing - Spacing Constraint Set - All Layers,** then the worksheet opens.

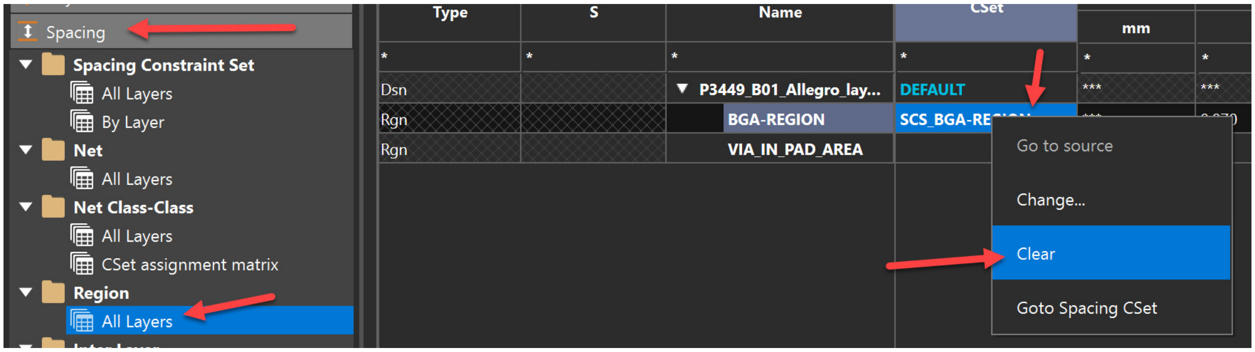


17. Notice that all the rows and columns still have the same value (0.076) and our higher level constraint set, SCS_BGA-REGION has **not** adopted the new spacing value I put in one of the cells in the BGA-REGION worksheet cells. Why is that?

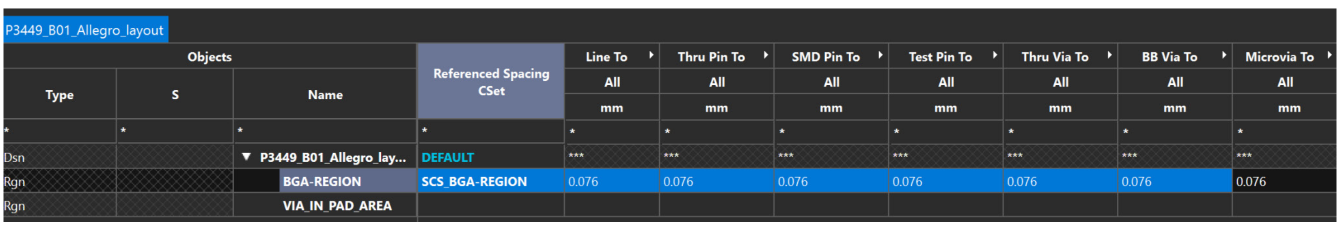
18. Higher-level constraint sets, such as SCS_BGA-REGION, do not adopt manual lower-level entries. This behavior allows you to apply these constraint sets to any number of objects or groups first, then later, lets you set more specific constraints that are unique to certain objects. That is, we can swap in and swap out constraint sets at any time to any object or region for convenience.

19. We won't go deeper into that, so for now, let's reapply the SCS_BGA-REGION constraint set to our spacing region.

20. Return to **Spacing - Region - All Layers** spreadsheet.



21. Right-click the cell that says SCS_BGA-REGION, where we've applied this spacing constraint set, then choose **Clear** (notice that the values changed to ***'s and 0.070's).
22. Now, left-click that blank cell and choose **SCS_BGA-REGION** again. Notice that the 0.070 value does not change.
23. Select all the cells in that row, then hit Delete on your keyboard until all your custom values are deleted. The spacing constraint set values will update to the original 0.076 found in the **SCS_BGA-REGION** rules (see below).



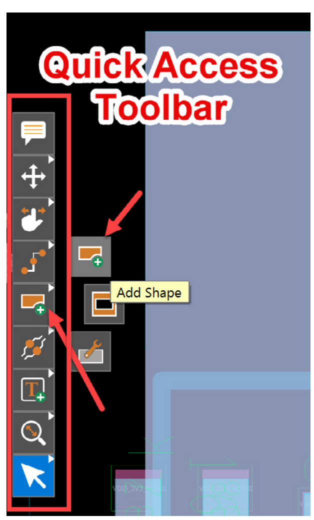
P3449_B01_Allegro_layout

Objects			Referenced Spacing CSet	Line To	Thru Pin To	SMD Pin To	Test Pin To	Thru Via To	BB Via To	Microvia To
Type	S	Name		All	All	All	All	All	All	All
				mm	mm	mm	mm	mm	mm	mm
*	*	*	*	*	*	*	*	*	*	*
Dsn		▼ P3449_B01_Allegro_lay...	DEFAULT	***	***	***	***	***	***	***
Rgn		BGA-REGION	SCS_BGA-REGION	0.076	0.076	0.076	0.076	0.076	0.076	0.076
Rgn		VIA_IN_PAD_AREA								

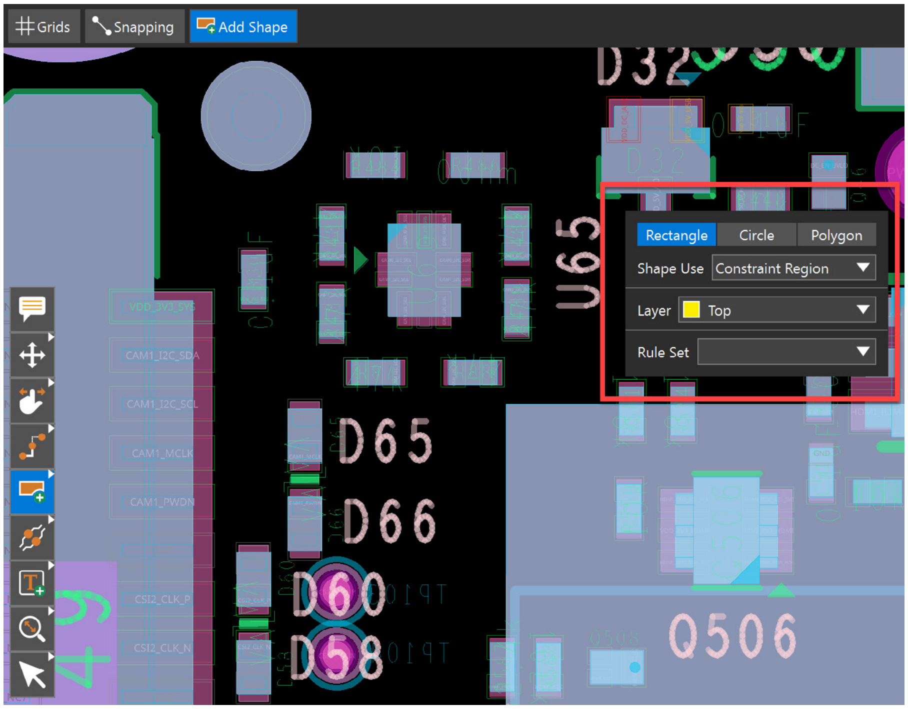
APPLYING THE CONSTRAINT REGION

Now that we have set the physical and spacing regions and created and applied physical and spacing rule sets just for those regions, we are ready to apply all those region-specific rules to an area of the PCB.

1. Take note of the **BGA-REGION** name. Close the CM.
2. Even though the CM automatically applies the rules, save the design (Ctrl + S) first.
3. In OrCAD X Presto PCB Editor, right-click the Add Shape icon found on the quick access toolbar, then select **Add Shape**.

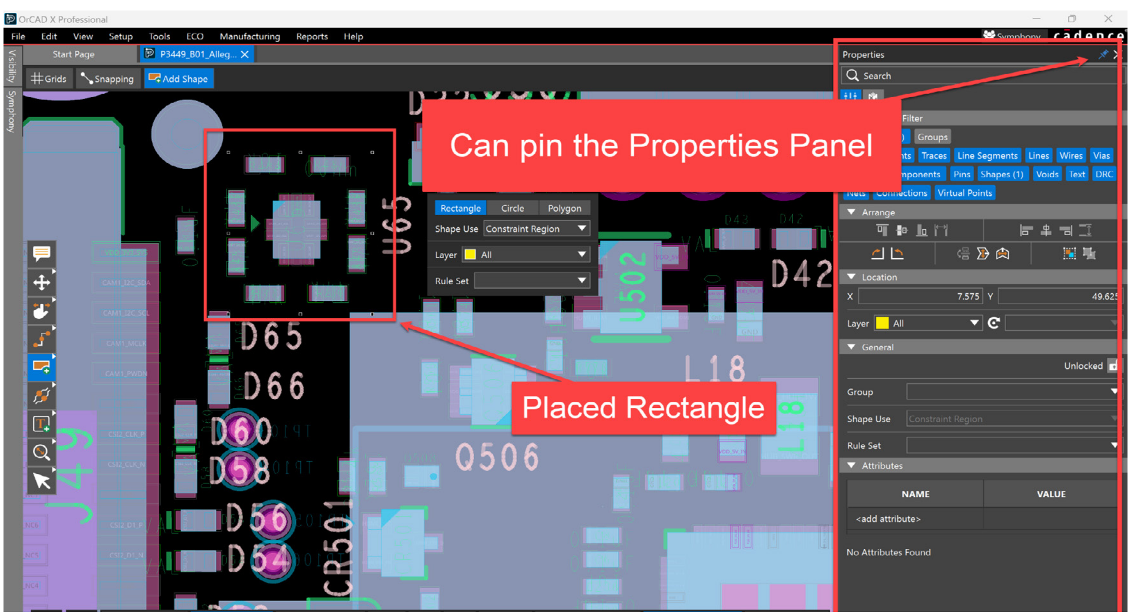


4. A window will appear so you can define the shape you want, the type of object the shape should be and the layers it applies to.



We're going to make a rectangular shape that is of type Constraint Region, then we'll apply its BGA-REGION rules to all layers of the PCB as long as they fit within that shape. And we will place that rectangle shape on top of a chip.

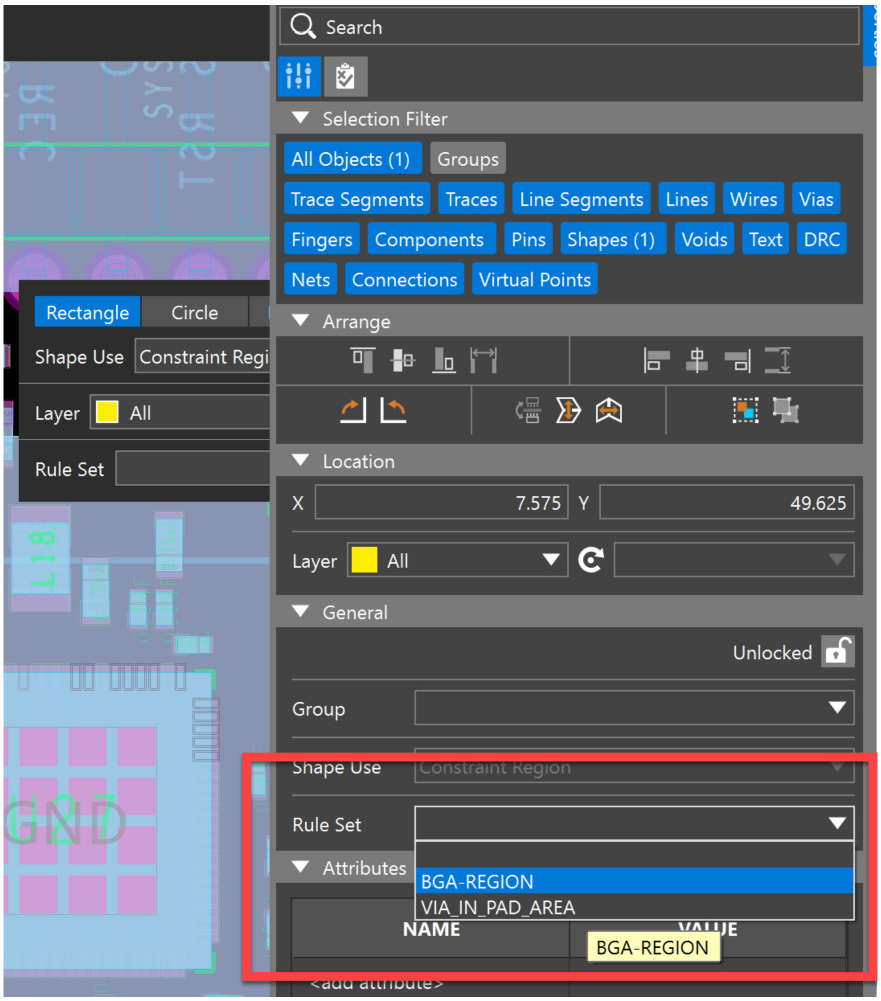
5. In the pop up window, select **Rectangle** for the shape.
6. In the **Shape Use** field, choose **Constraint Region.**
7. In the **Layer** field, choose **All** (this constraint region will apply to all layers of the PCB).
8. Now click hold and drag a rectangle or square shape across the U65 device just to test out the rule.



9. Open the **Properties** panel found on the right of the OrCAD X Presto PCB Editor window.
10. To keep that panel active, click the **Pin** icon in the upper right corner.

For all objects on the PCB canvas, you can select that object then examine its properties in the Properties panel. In the case of our Rectangle, we need to add a Rule Set to it. We do that in the Properties Panel.

11. In the Properties panel, navigate to the **Rule Set** field, then click the dropdown and select **BGA-REGION** (the region we created earlier for physical and spacing rules).



12. Press the Escape key (ESC) when finished. The rectangle constraint is placed, and you can modify the rest of the PCB as needed.

In this exercise, we created constraint regions with their own spacing and physical rules that apply only to that region type. We saw how such rules can be applied to any area of the PCB, allowing more relaxed or, oftentimes, stricter constraints than on the rest of the PCB.

In the next section, we will summarize the differences among net groups, net classes, and regions.

KEY DIFFERENCES AND IMPLICATIONS AMONG NET CLASSES, GROUPS, AND CONSTRAINT REGIONS

As stated, for complex PCBs, we need classes, groups, and regions to create a robust set of rules that will make our design reliable or right the first time. The scope, application, and flexibility vary for each of these constraint types. Below are the distinctions, pros, and cons of each of them:

1. Scope:
   a. Net Classes: Domain-specific
   b. Net Groups: Cross-domain
   c. Regions: Area-specific on the PCB
2. Rule Application:
   a. Net Classes: Can have class-to-class rules (e.g., spacing between different classes)
   b. Net Groups: Cannot have class-to-class rules
   c. Regions: Can have rules that override global or class-based rules within the defined area
3. Flexibility:
   a. Net Classes: Most flexible for domain-specific rules
   b. Net Groups: Best for general organization and basic rule application
   c. Regions: Most powerful for managing complex board areas with unique requirements

For more details on which constraints you can set, see the CM hierarchy chart below.

Electrical	Physical	Spacing (net-to-net/same-net)
--------------------------	Design	Design
Net Class	Net Class	Net Class
Bus	Bus	Bus
Differential Pair	Differential Pair	Differential Pair
Match/Relative Group	--------------------------------	--------------------------------
Xnet	Xnet	Xnet
Net	Net	Net
Pin Pair	Pin Pair	Pin Pair
--------------------------	--------------------------	Net Class-Class*
--------------------------	Region	Region
--------------------------	Region-Class	Region-Class
--------------------------	--------------------------	Region-Class-Class*

* Not available in the Same Net Spacing Domain

Constraint Management Hierarchy Chart

Benefits:

As we have seen, there are major benefits to having constraint regions in your designs. The top two benefits are:

- Allowing for area-specific rule application
- Helping manage complex designs with varying and often unique requirements

Summary

In this part of the guide, you learned the following:

- What constraint management is
- The problems that constraint management solves in PCB design
- Benefits of properly constraining your design software and PCB
- Understanding the constraint manager and how it applies constraints
- The different types of constraints
- Net Classes and their use
- Net Groups and their use
- Constraint Regions and their use

Conclusion to Part 1

In this first part of the OrCAD X Constraint Management Guide, we've explored the foundational aspects of constraint management in PCB design. We delved into creating and applying constraint regions, which allow for precise control over specific areas of a PCB, ensuring both reliability and efficiency in complex designs. The key takeaways include understanding the types of constraints, their applications, and the benefits of using constraint regions to manage intricate design requirements. As we move forward, the next sections will provide quick, practical guides on implementing common beginner-level constraints, equipping you with the knowledge to optimize your design processes.