FlowCAD

FloWare Modules – Enhancing Productivity

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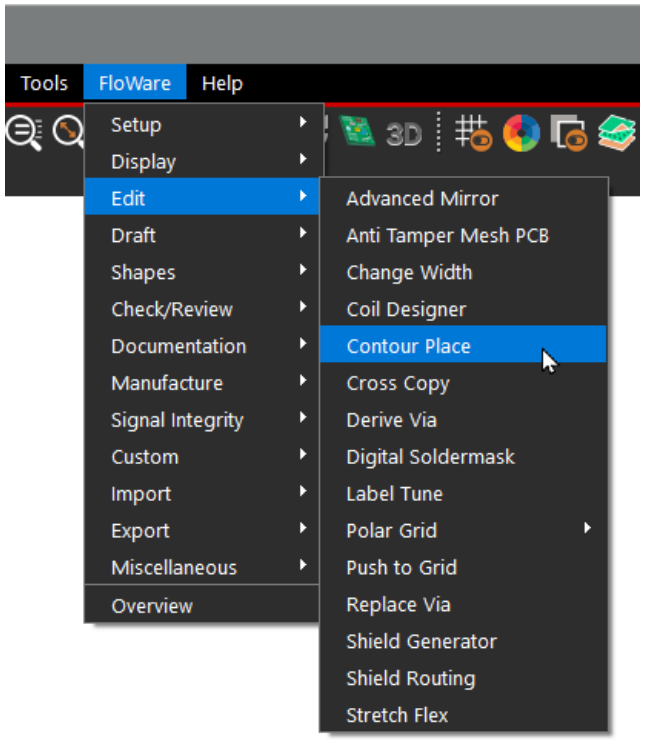
October 2024

FloWare Features

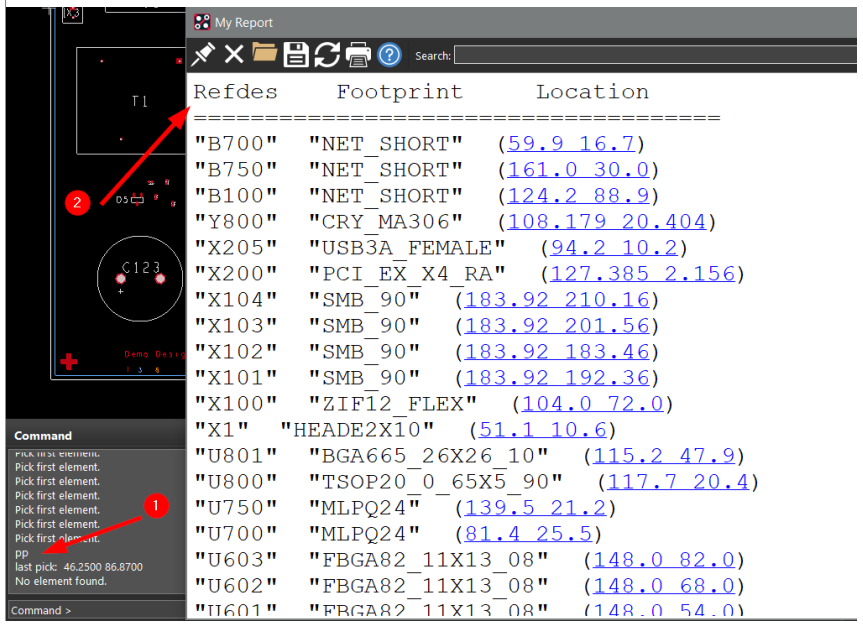
- General purpose utilities
  - Functions not in standard tool yet
  - Not written for one specific customer
  - Everybody should benefit
- Easy installation
  - Also casual users must be able to install FloWare
  - No variables
  - Menus will be created automatically
  - Integrates perfectly into existing customizations
- Documentation
  - Full documentation is provided for every module



FloWare Under the Hood: Skill Interface

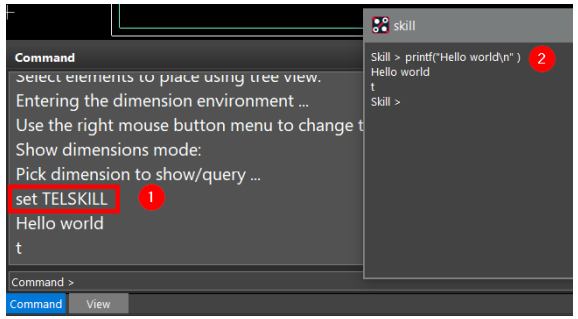
- The PCB Editor Skill in Cadence Allegro is a powerful scripting language used to automate and customize tasks within the PCB design environment. It allows users to write scripts that can manipulate design objects, automate repetitive tasks, and create custom functions to enhance the design workflow.
- Key aspects of PCB Editor Skill
  - Automation
  - Customization
  - Data manipulation
  - User interaction
  - No platform dependencies

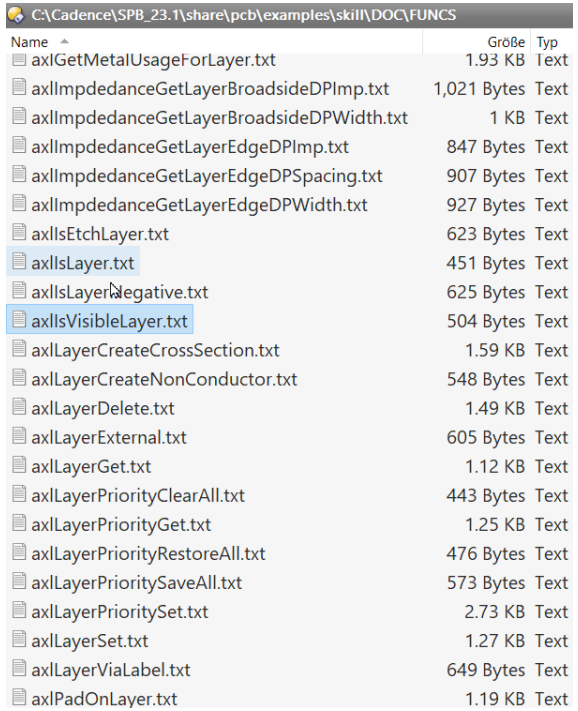
```
procedure( my_pp()
let( (report_file port)
  report_file =  "./my_pick_and_place.txt"
  port = outfile(  report_file "w" )
  fprintf( port  "Refdes    Footprint     Location\n"      )
  fprintf( port  "=====================================\n" )
  foreach( cmp  axlDBGetDesign()->components
     fprintf( port "%L  %L  %L\n"  cmp->name   cmp->symbol->name  cmp->symbol->xy )
  )
  close(port)
  when( isFile( report_file )
     axlUIViewFileCreate( report_file "My Report" nil )
  )
  t
);let
);proc

axlCmdRegister(  "pp"  'my_pp )
```



Getting Started with Skill

- Start an interpreter window by typing **`set TELSKILL`** and start talking with the database
  - No compiling necessary
- Write some commands e.g.
  `printf( "Hello world\n" )`
- Refer to documentation axl API, which give you a list of commands which allow you to access information from the database
- Extend your skills with Skill by testing, writing, checking etc. Be curious!





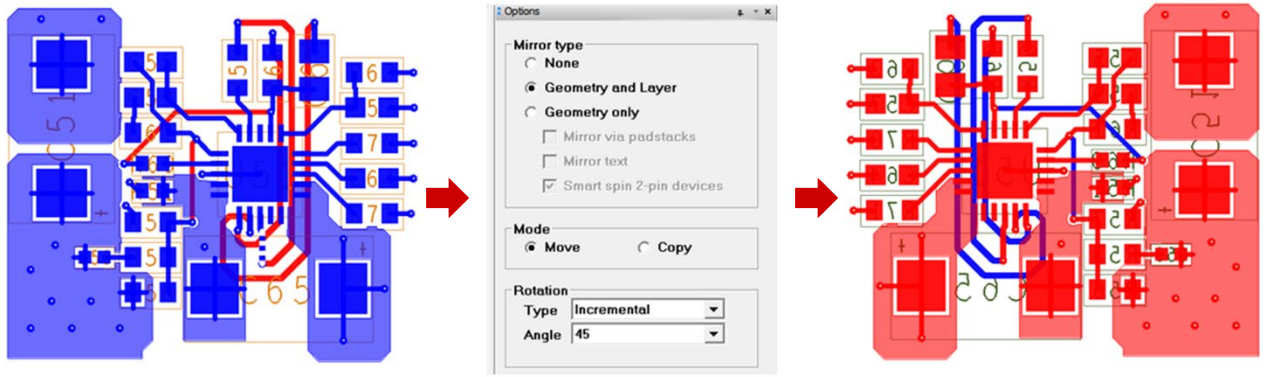
FloWare Modules PCB Editor

- Advanced Mirror
- Advanced Testpoint Check
- Anti Tamper Mesh PCB
- AOI Check
- Assign Net to Via
- Barcode Generator
- Batchplot
- CAF-DRC
- Change Width
- Class Color
- Cleanliness Check
- Coil Designer
- Contour Place
- Cross Copy
- Cross Section Generator
- Custom Variables
- Design Compare
- Digital Soldermask
- Drafting Utilities
- Drawing Designer (legacy)
- Drawing Size
- Drawing View Manager
- Edge Plating
- FPGA Utilities
- Highlight Dummy Pins
- IBIS Prototype Modeler
- Label Generator
- Label Tune
- Mask Generator
- NC Panel Route
- Net Color View
- Net Min Gap
- Padstack Finder
- Padstack Usage
- Panelization
- PCB Library Plot
- Polar Grid Utilities
- Post Processing
- Push to Grid
- Quick Symbol Edit
- Replace Via
- Shape Utilities
- Shield Generator
- Shield Routing
- Silkscreen
- Snap Generator
- SVG Export
- Synchronize Testprep
- Variant 3D
- Variant Assembly
- Variant BOM
- Z-DRC

Videos available on YouTube

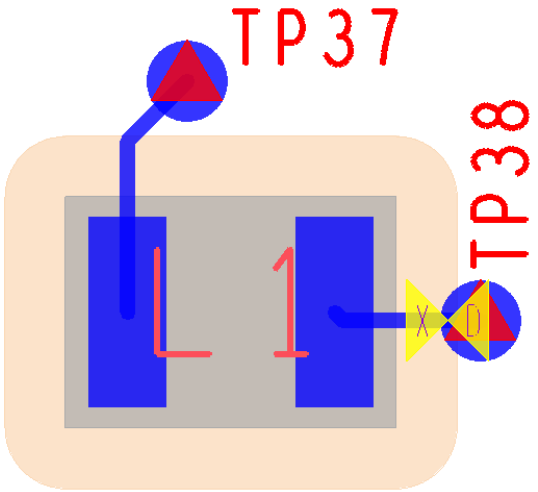
Advanced Mirror

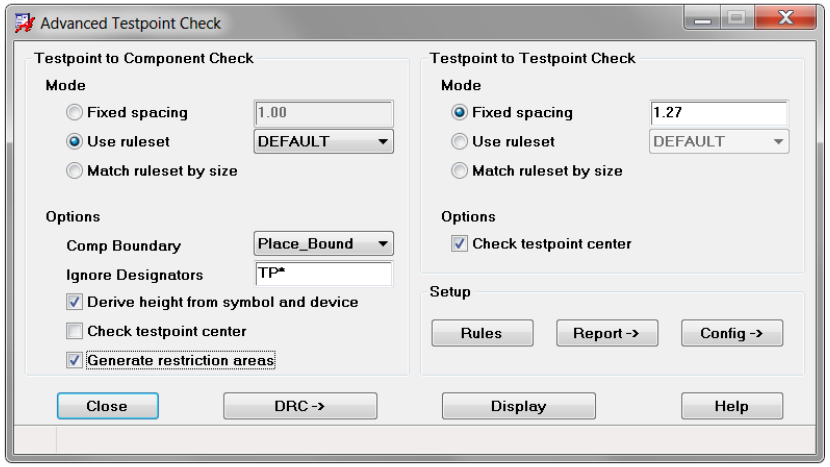
- Enables mirror operations while moving or copying elements
  - Mirror across subclasses **(Geometry and Layer)**
  - Mirror on the same subclass **(Geometry only)**
- Including placement and routing
- Selection through window or single pick, dynamic preview
- Special handling for symbols, vias and text in **Geometry only** mode



Advanced Testpoint Check

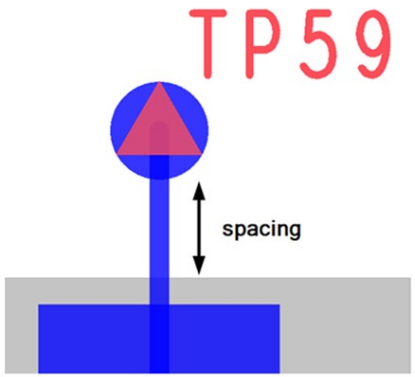
- Addresses various rules for testpoint checking
  - Testpoint to Testpoint check
  - Testpoint to Component check taking component height into account
  - Visualization of restriction areas
  - DRC marker generation
  - Constraints reuse through configuration files

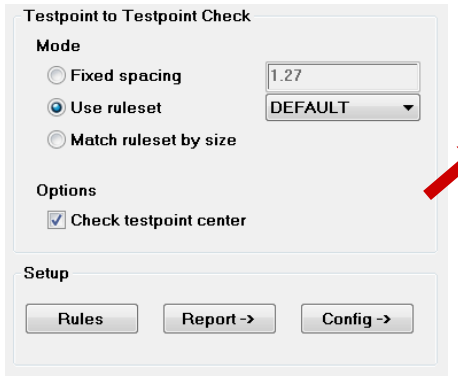


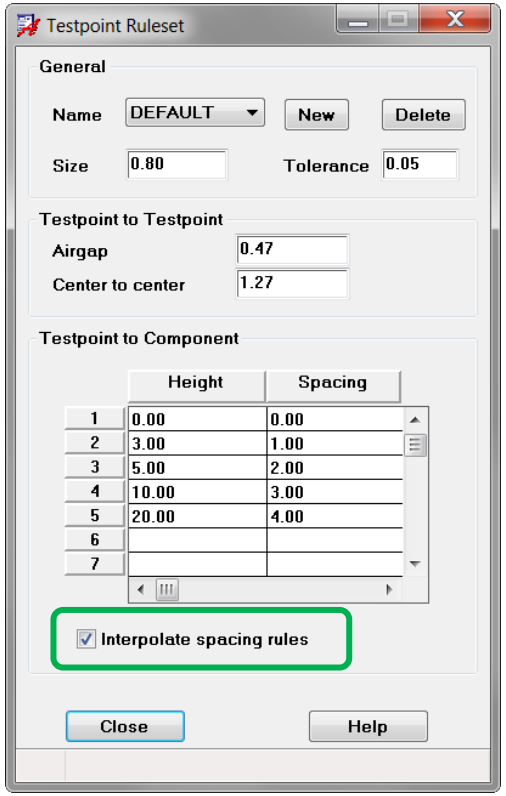


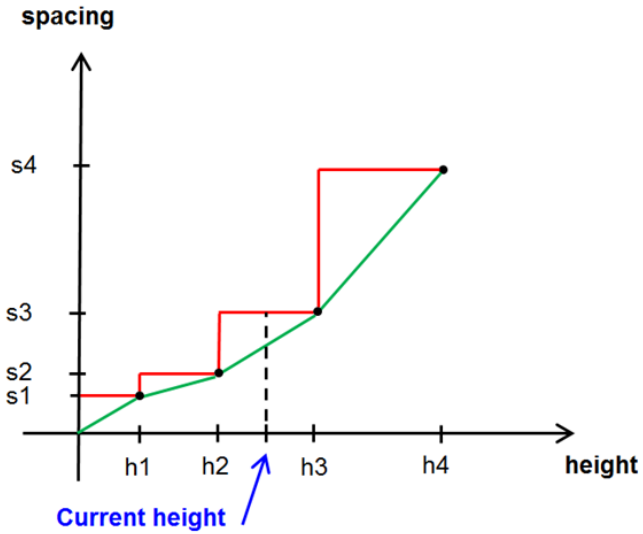
Advanced Testpoint Check

- Spacing rules may be specified
  - As fixed spacings
  - Using rulesets, which account for component height



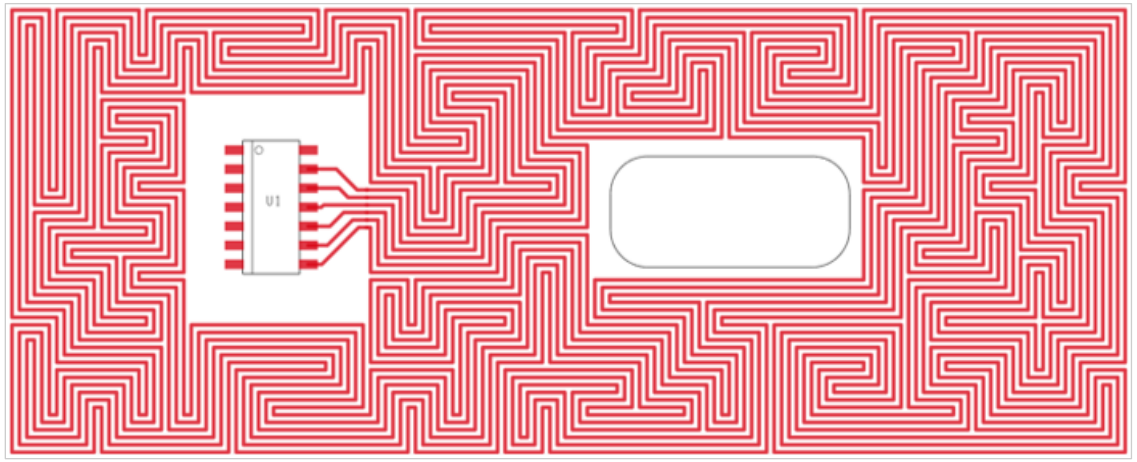


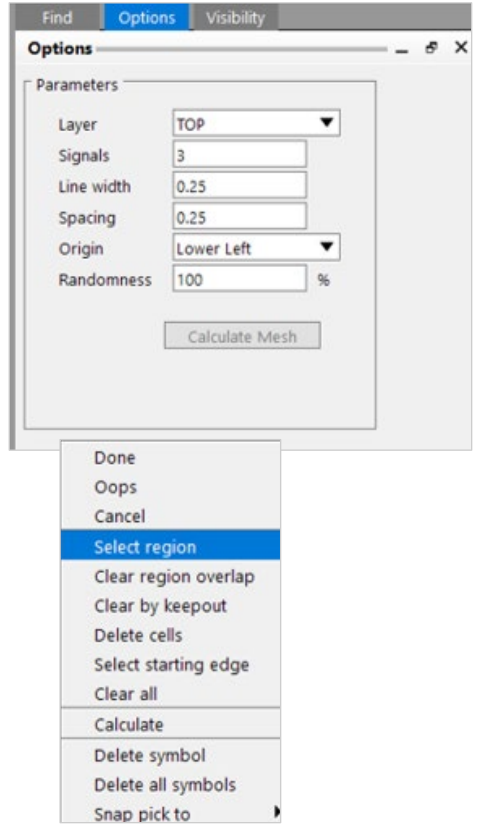




Anti Tamper Mesh PCB

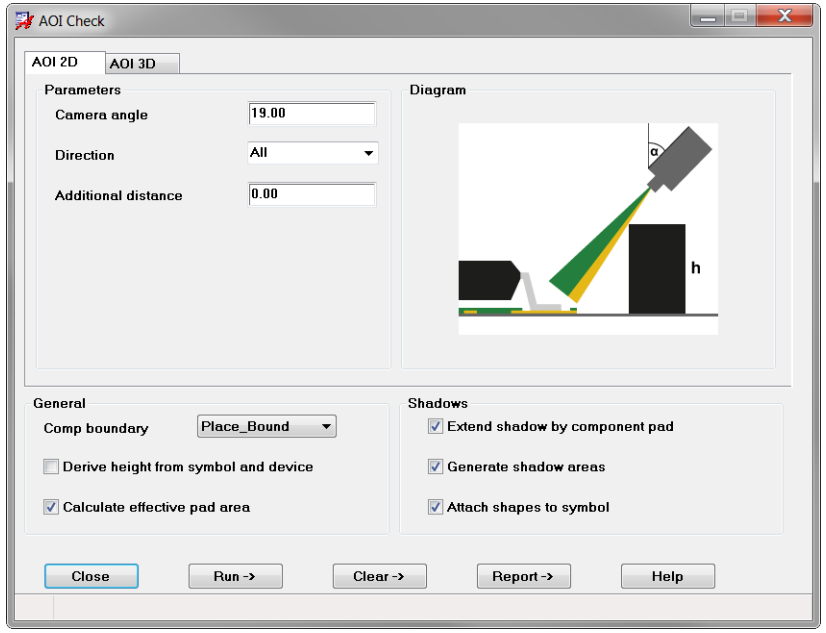
- Useful for Hardware Security Modules (HSM)
  - In order to actively detect and respond to external attacks a convoluted maze of wires (mesh) can be used to monitor changes in resistance, capacitance, breaks, shorts etc.
- Features
  - Number of signals, width, spacing, …
  - Region select, keepouts, destination layer, …
  - Randomness

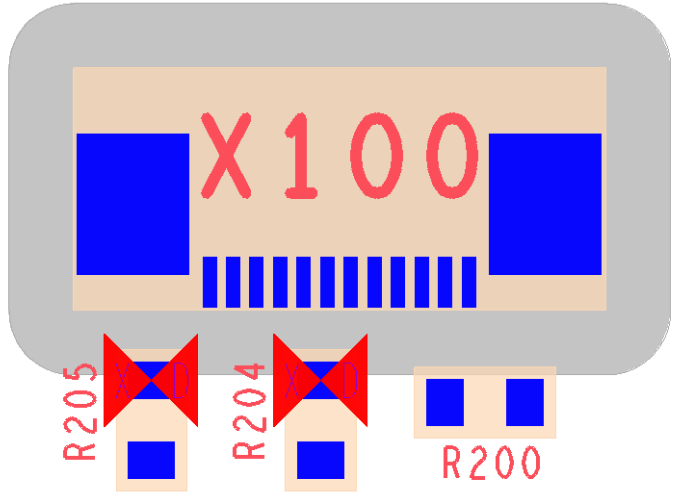


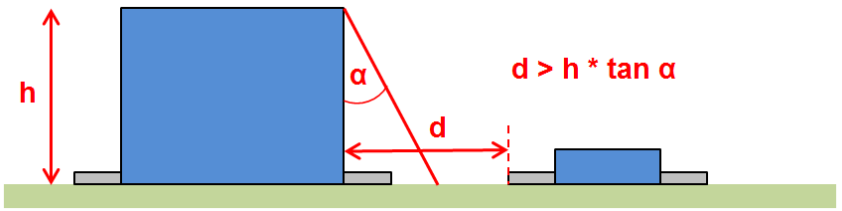


AOI Check

- Helps users to check AOI related rules directly in **PCB Editor**
- Shadowing can cause serious issues in verification process

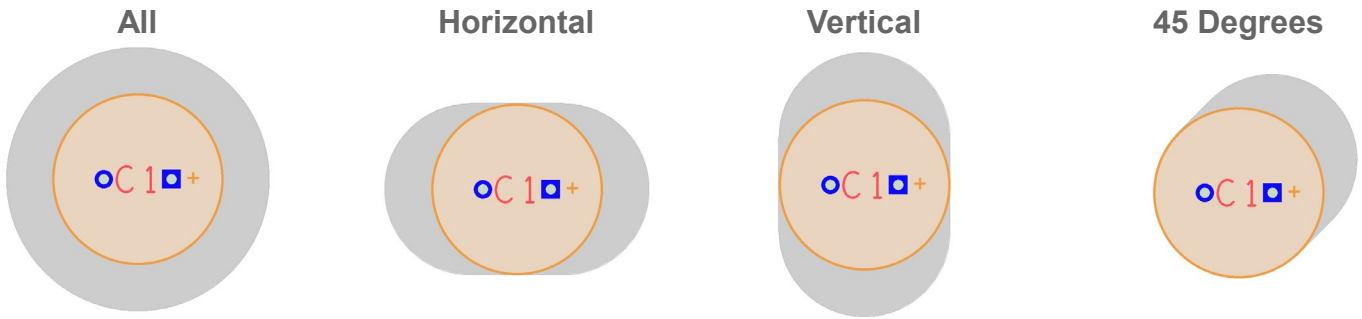




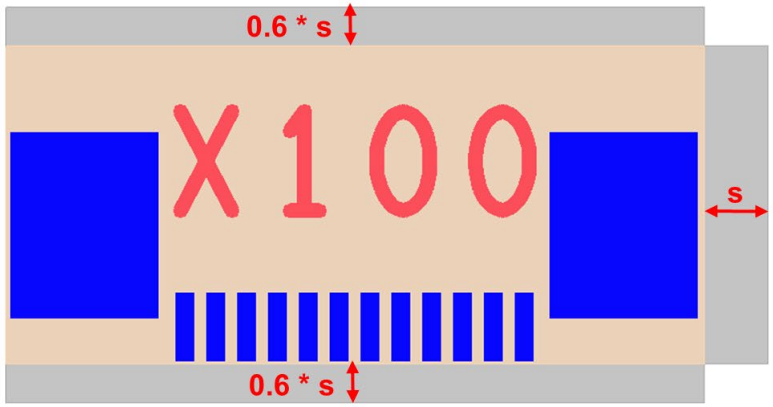


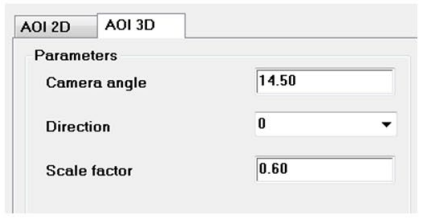
AOI Check

- Shadows can be calculated in various directions based on specified camera angles taking component height into account



- Special rules apply to 3D inspection systems

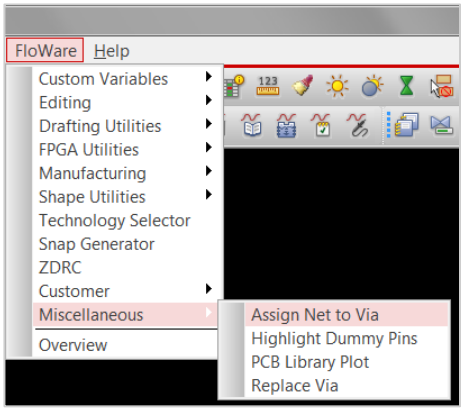


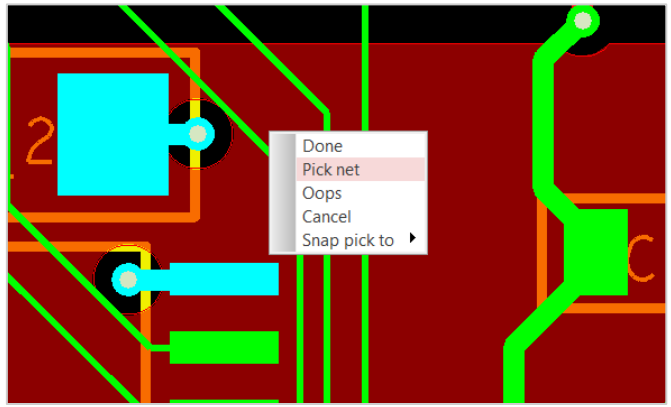


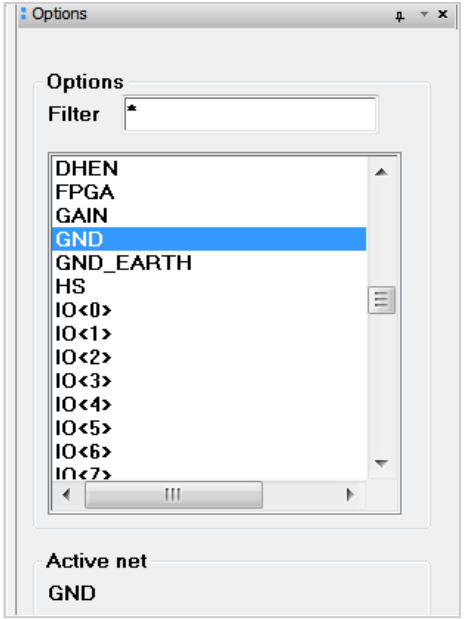
SMT flow direction

Assign Net to Via

- Enables users to change the net on existing vias
- No need to delete and route new ones
- Use model
  - Select net from list (including wildcard support) or by context **RMB > Pick Net**
  - Click on one or more vias
  - Choose **RMB > Done** to confirm

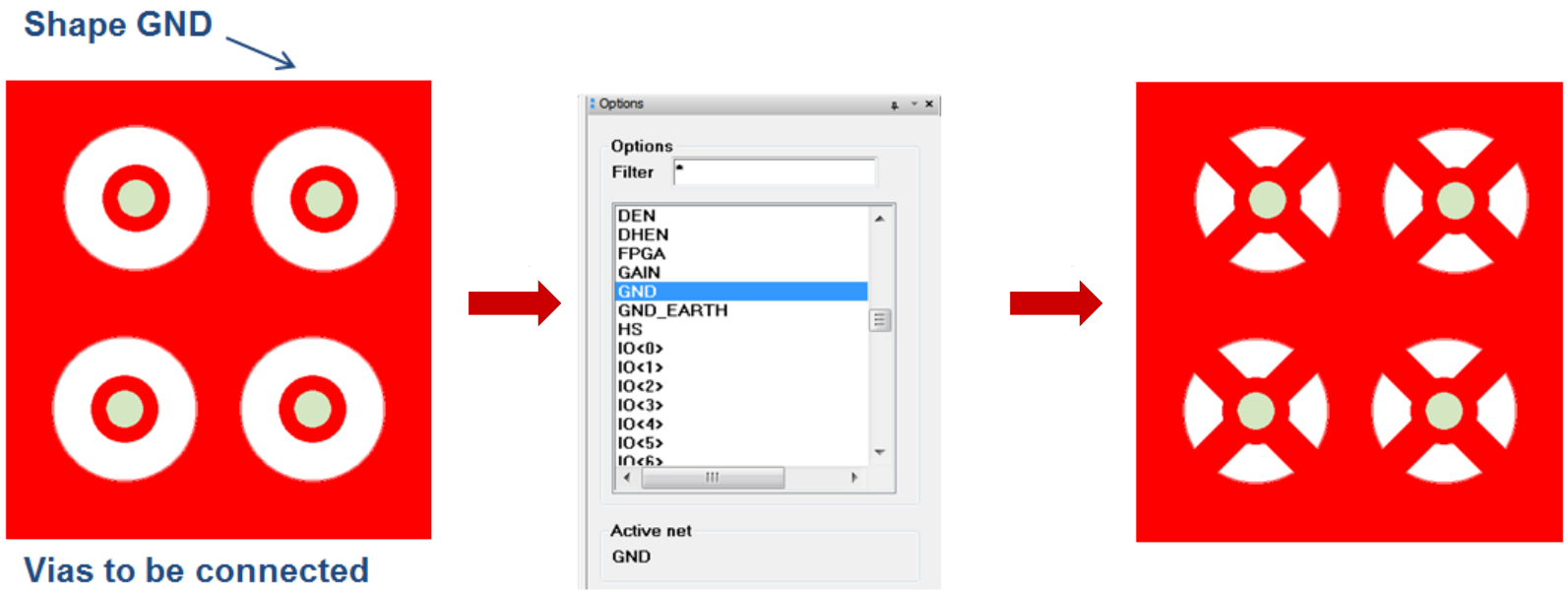






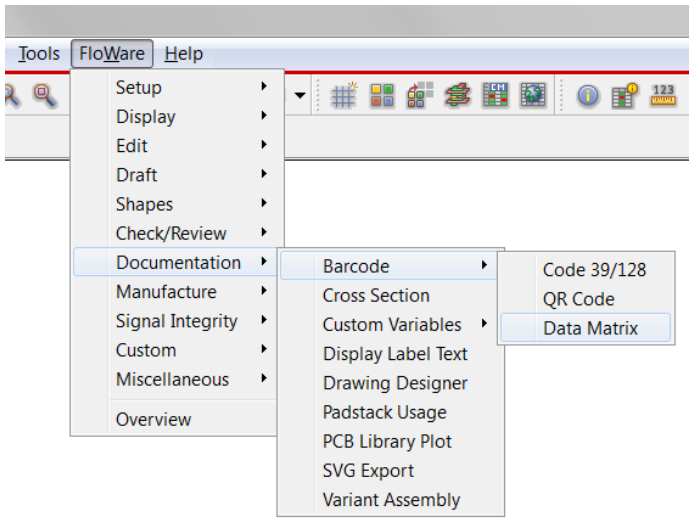
Assign Net to Via

Example

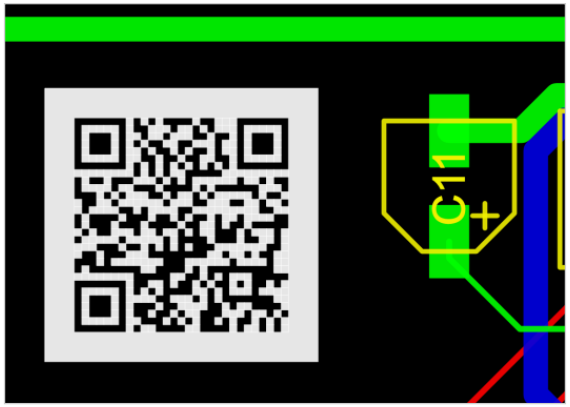


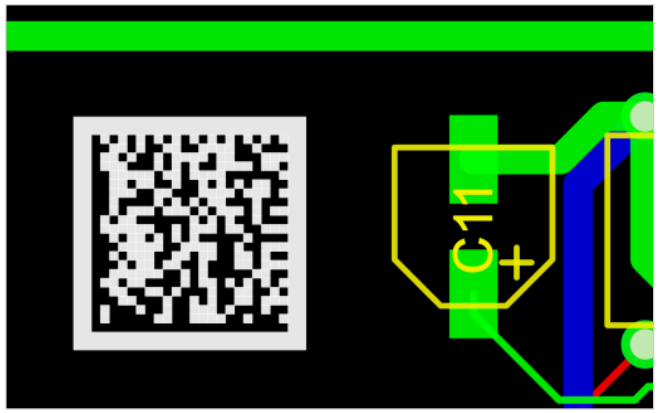
Barcode Generator

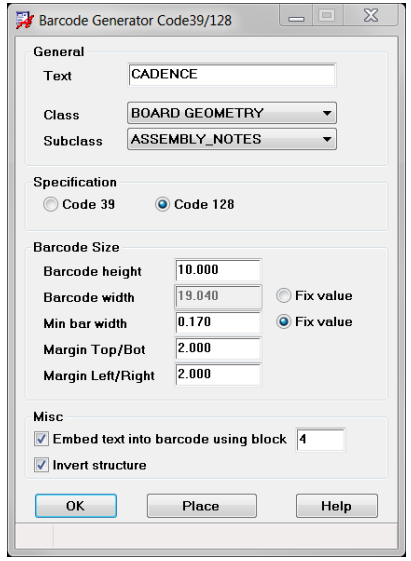
- Prints barcodes on a PCB layer as part of the manufacturing process
- Supporting definitions
  Code 39, Code 128, QR Code and Data Matrix
- Adjustable parameters corresponding to selected code
- Additional drawing options
  (e.g. show text, inverted display)
- Dynamic preview during parameter change
- Parameter preset through configuration file

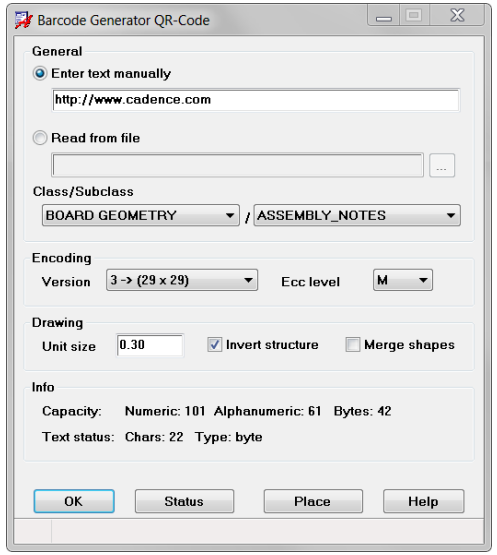


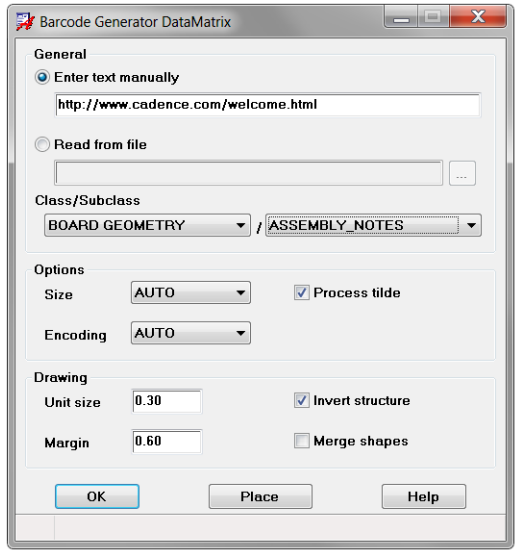
Barcode Generator





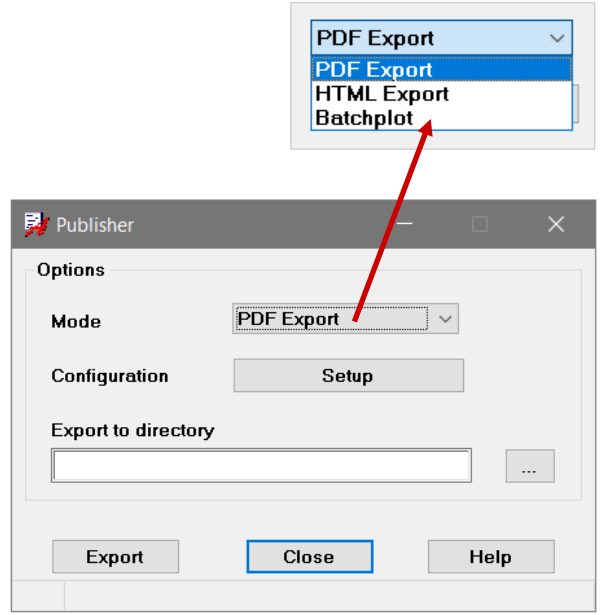






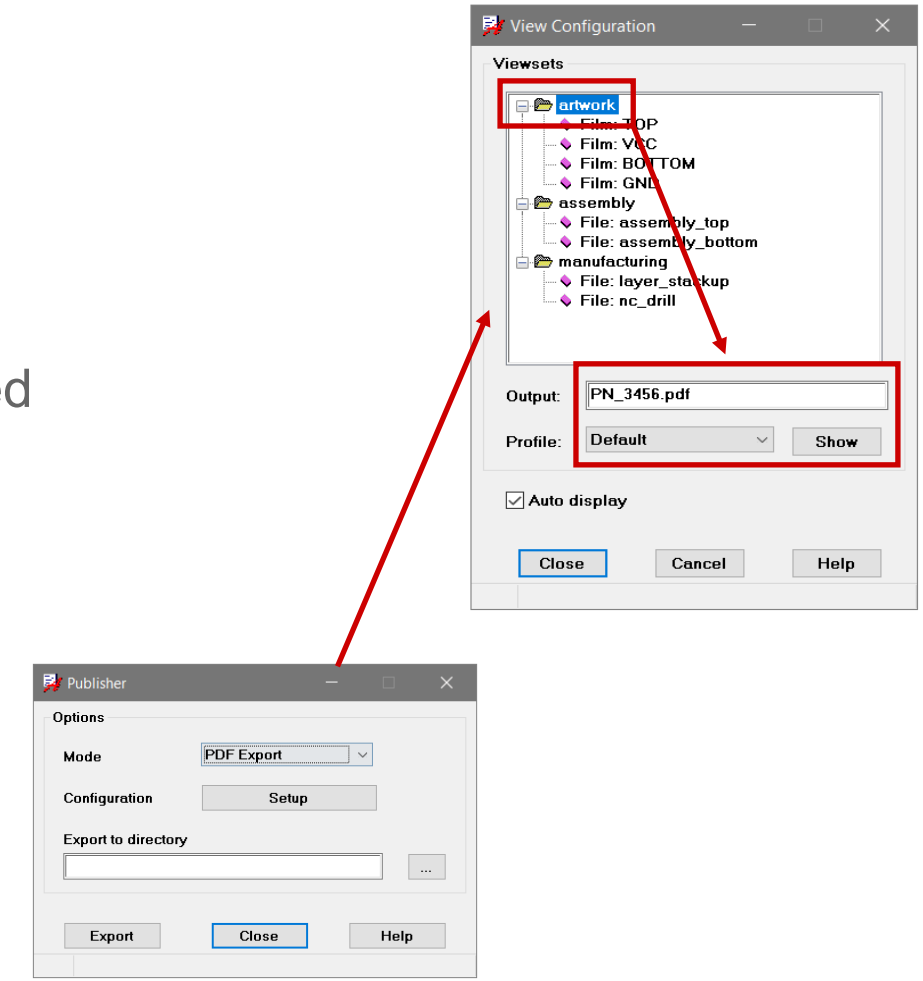
Batchplot

- **Creates documentation**
  - Fully automated
  - Multipage or single page files
  - Visibility control based on views (color views as well as artwork views), similar to visibility panel
  - Order of view items can be changed by user
  - Plotsets allow grouping views into separate PDF files
  - Load and save configuration to disk
  - Three modes
    - PDF Export from Allegro / OrCAD PCB Editor
    - HTML Export
    - Batchplot (legacy)



Batchplot

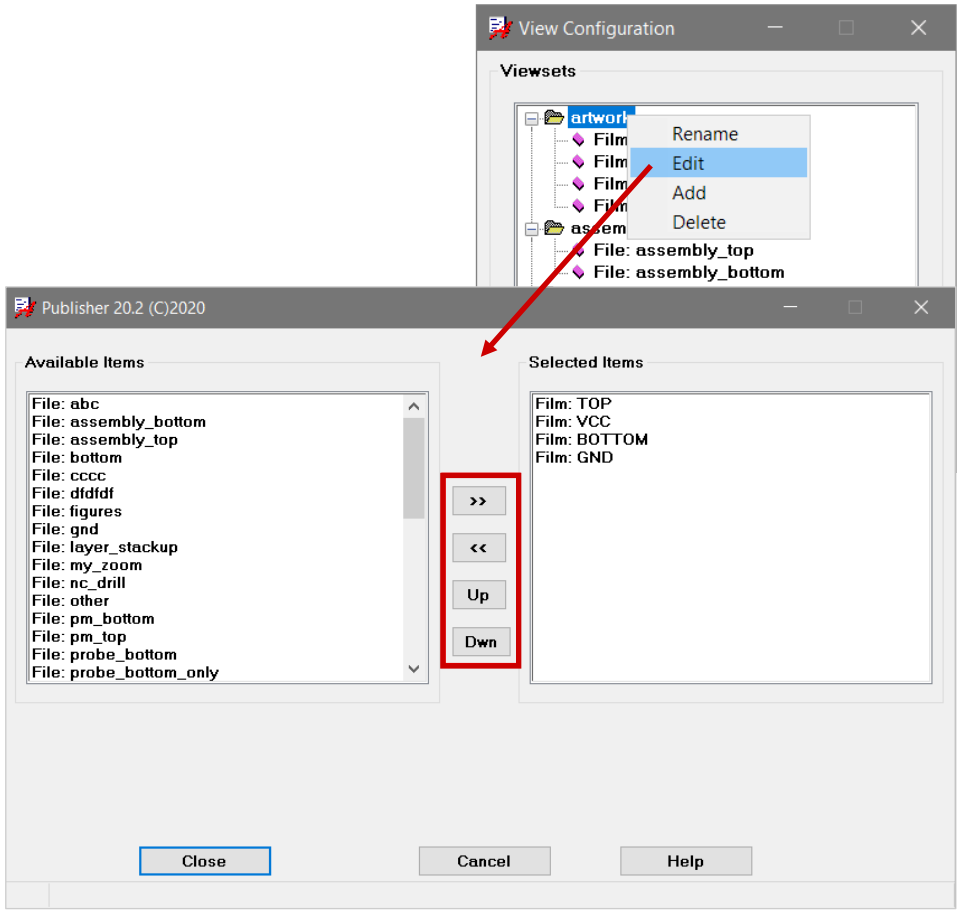
- Multiples viewsets can be defined
- A viewset may contain
  - Film records
  - Color views (!!)
- Each viewset corresponds to one PDF file to be generated
  - Name of the PDF file can be specified (output)
- Each viewset may reference a profile to be used during PDF export
  - E.g. black white print only
  - With / without meta data
  - …
- Single push button to generate all data ...



Batchplot

Setup Viewsets for PDF Export

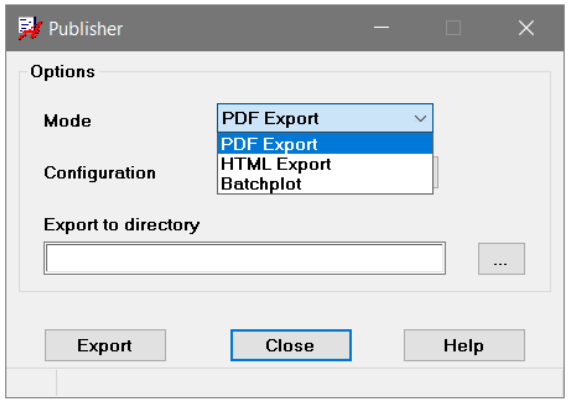
- Use context menu in tree view
  - Rename
  - Edit
  - Add
  - Delete
- Edit views
  - Select film views
  - Select color views
  - Change order

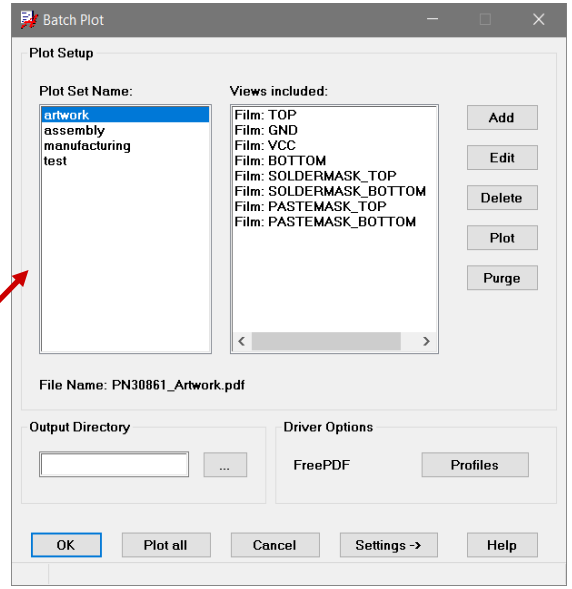


Batchplot

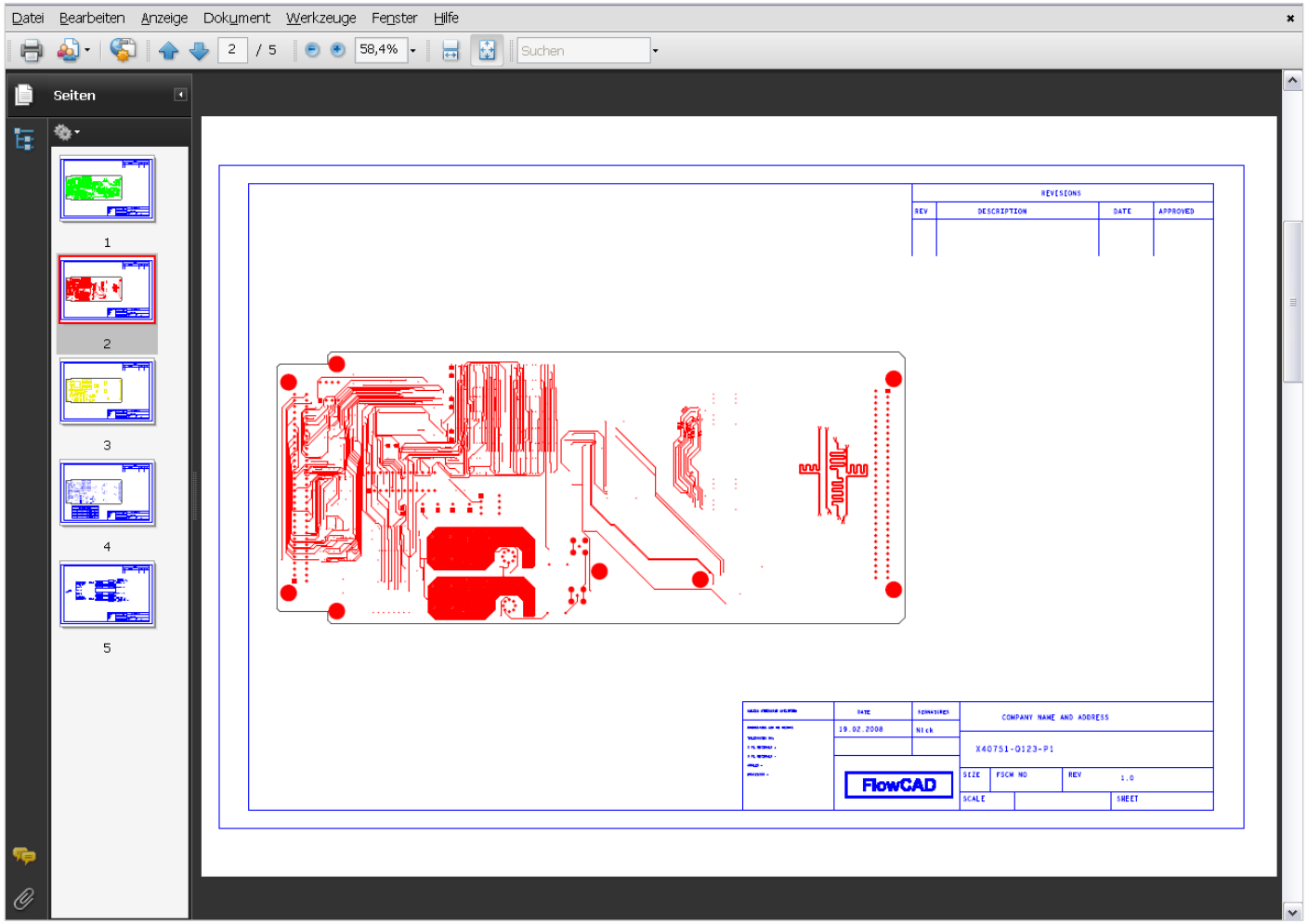
Other Modes

- HTML Export
  - Generates an HTML report including SVG graphics
  - Setup regarding viewsets and profiles similar to PDF Export
- Batchplot (legacy)
  - Selecting Setup will launch the existing / legacy application
  - Still available and supported





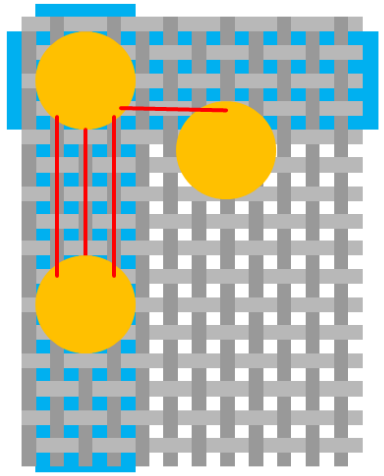
Batchplot

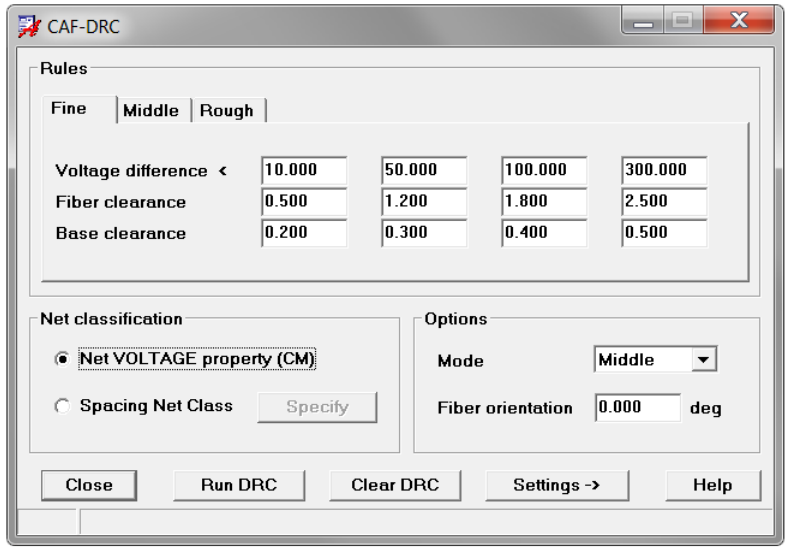


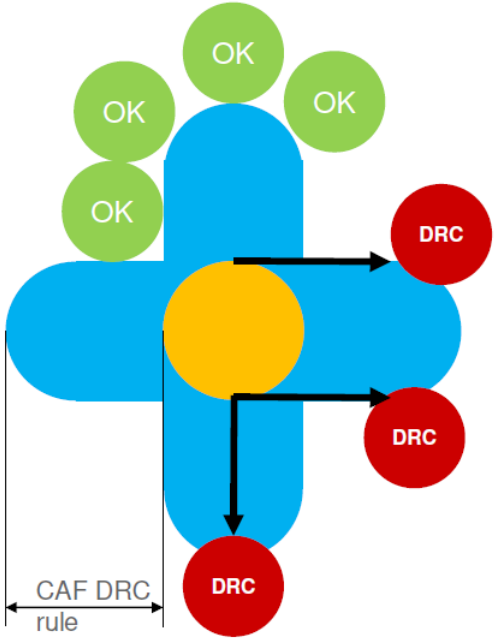
Final document opened with Acrobat Reader

CAF-DRC

- Special DRC for Conductive Anodic Filaments (CAF) on PCBs
- Performs Hole-to-Hole clearance checks along the fiber structure
- Based on voltage classification
- Adjustable fiber orientation

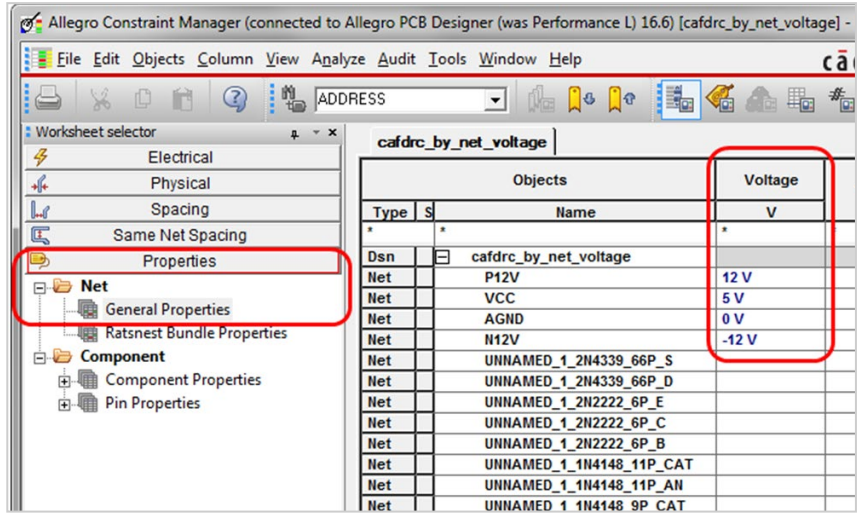


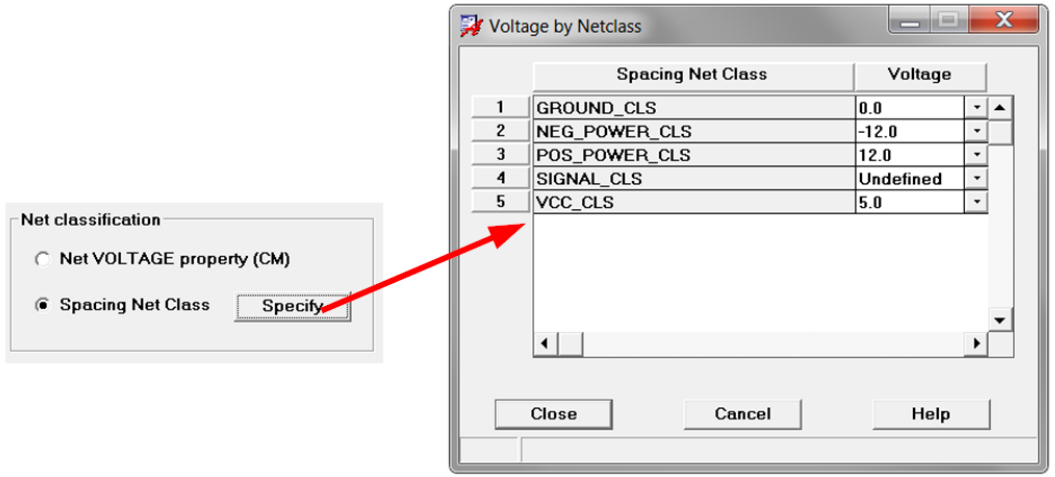




CAF-DRC

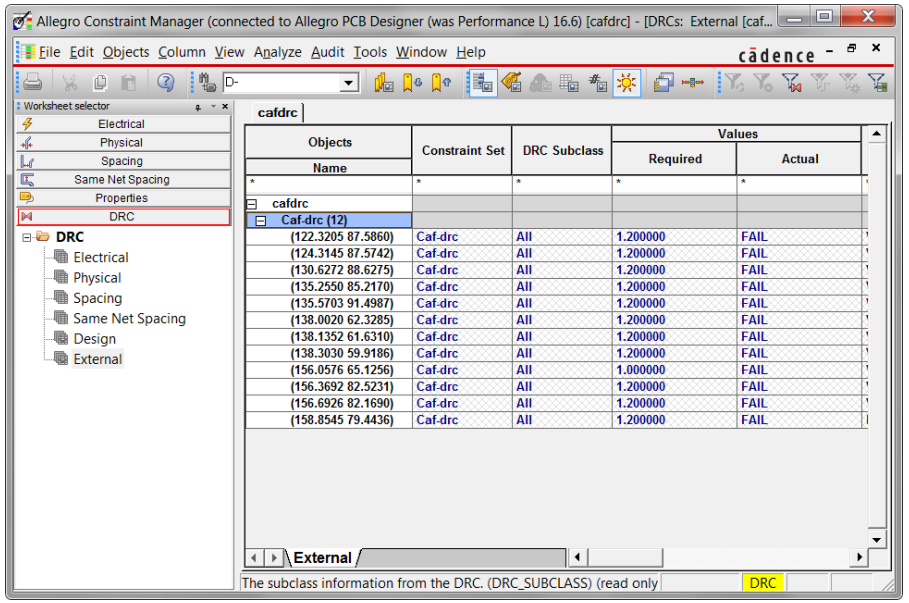
- **Use model**
  - Classify nets by voltage property or by spacing net class
  - Launch application
  - Specify rules and select mode to be used
  - Export / import rules for reuse purposes
  - Run DRC

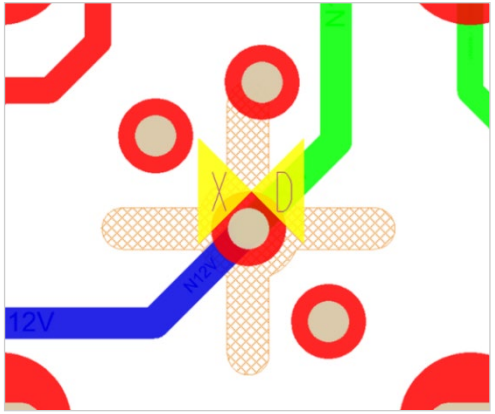


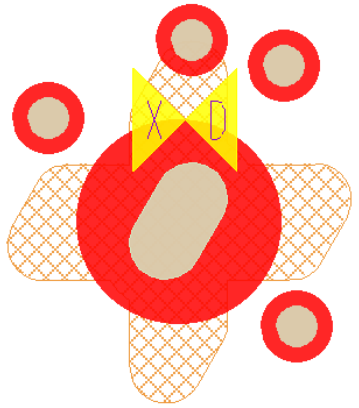


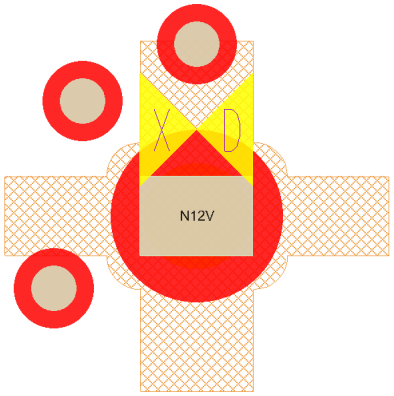
CAF-DRC

- **Results**
  - DRC markers in PCB Editor and Constraint Manager including cross probing
  - Visualization of DRC polygons on DRAWING FORMAT subclasses CAFDRC_DV1, _DV2, DV3 and _DV4
  - Handles all drill and slot types



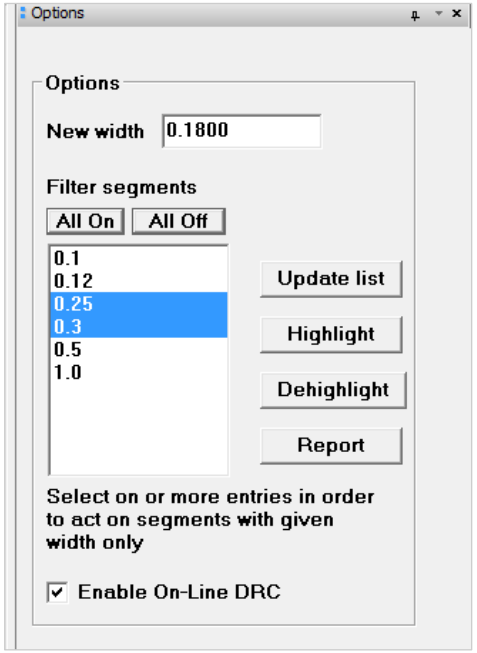


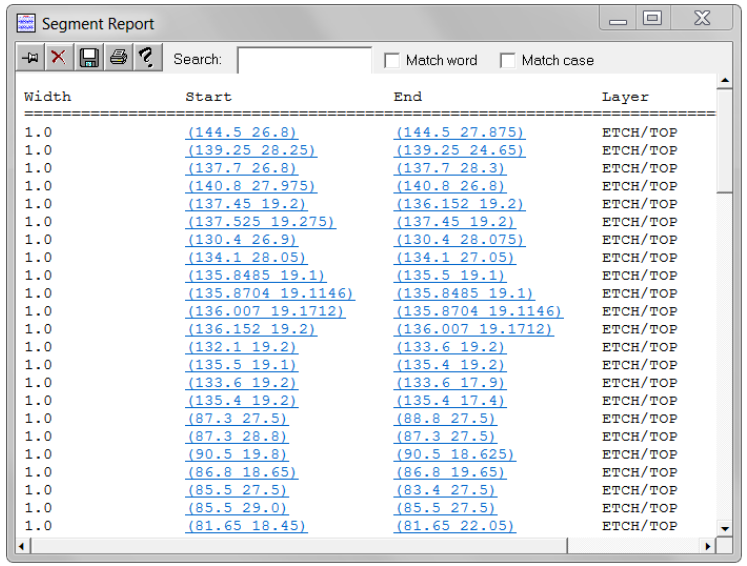




Change Width

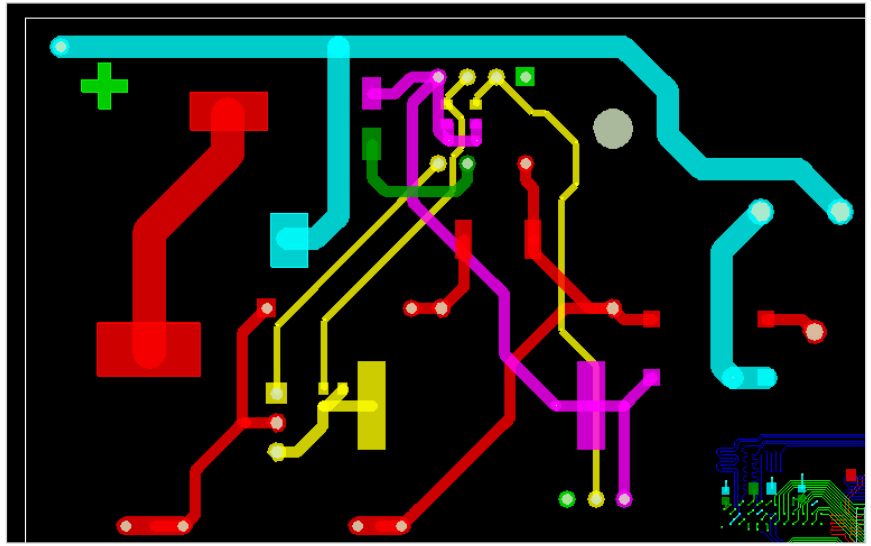
- Change the width of clines and clines segments
- Supporting a filter mechanism in that the changes are only applied to segments matching a given width
- Select by Pick, Window, Temp Group or Find By Name
- Highlight and report functionality including cross probing

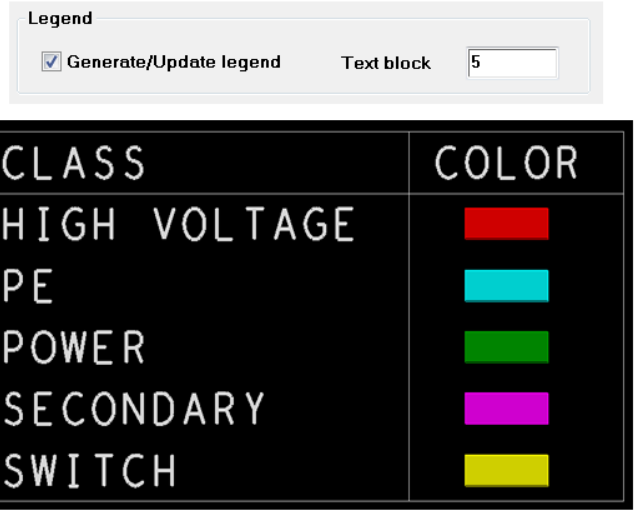


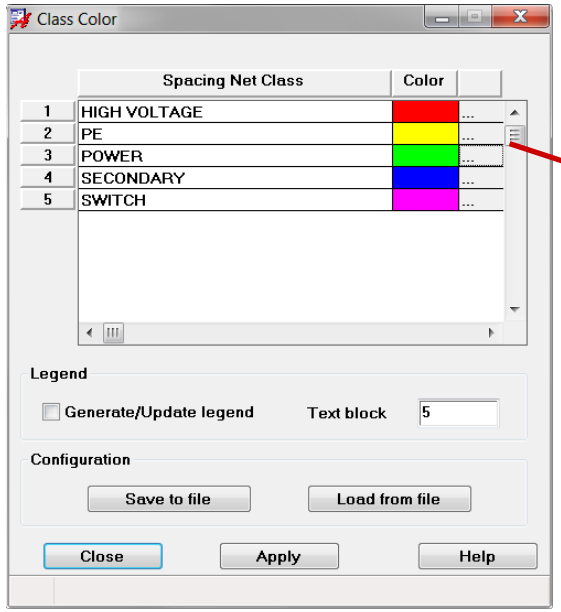


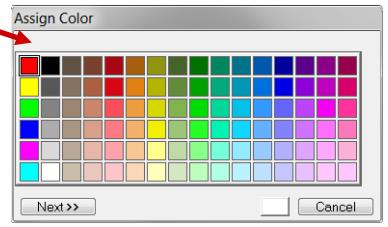
Class Color

- Enables users to color spacing net classes for review and documentation purposes
  - Color chooser
  - Legend support
  - Settings stored in database
  - Export / import settings



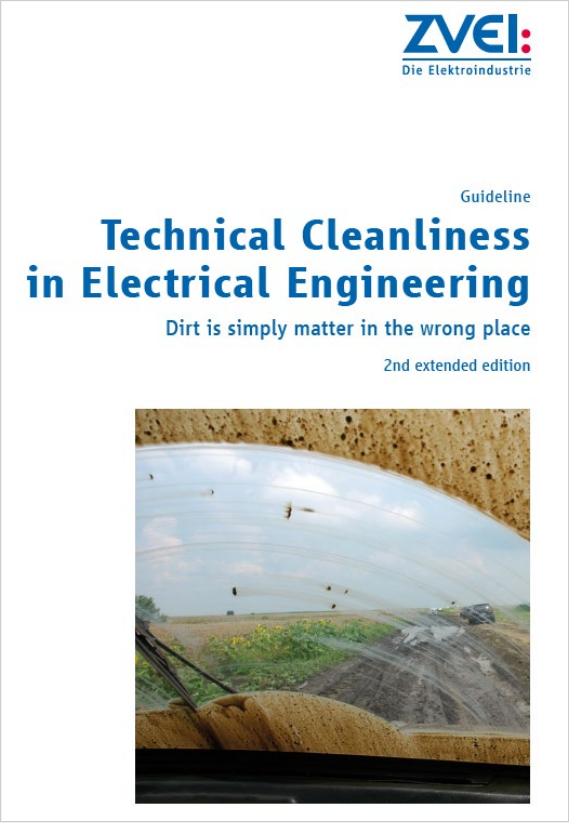






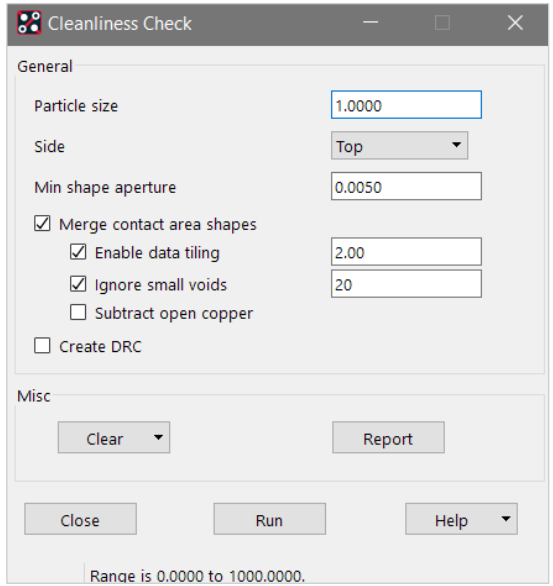
Cleanliness Check – Technical Cleanliness

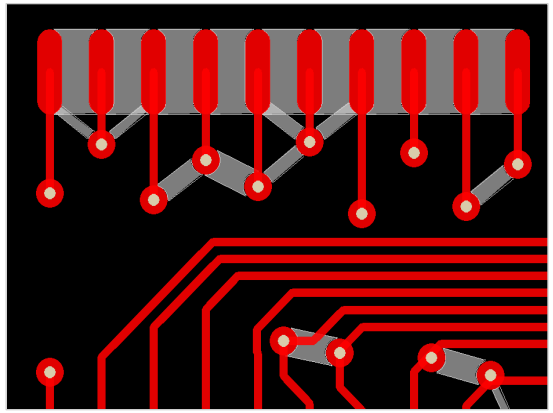
- Technical Cleanliness refers to the performance of components, assemblies and systems related to particle contamination in automotive and other applications
- On PCB's such particles (e.g. conductive particle from aluminum cover) may cause short circuits
- The probability failure depends on
  - Particle size
  - Contact area size
  - Number of contact areas
- For more information refer to document ZVEI Guideline for Technical Cleanliness from https://www.zvei.org/



Technical Cleanliness

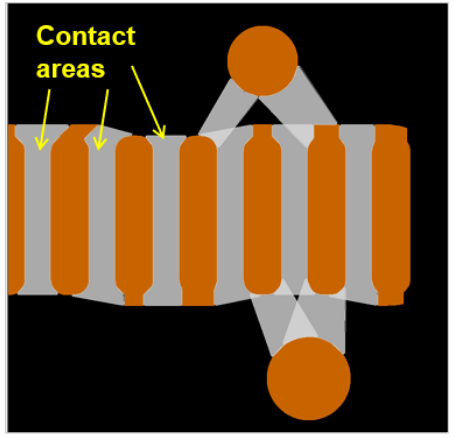
- Analyzes the PCB layout for contact areas caused by particles with a given size
- The contact area specifies the area in which a particle will cause a short, no matter how the particle is oriented
- Cleanliness Check calculates and visualizes contact areas using shapes and writes a report
- By sweeping the particle size the information from the output can be used to feed cleanliness assessment calculator from ZVEI

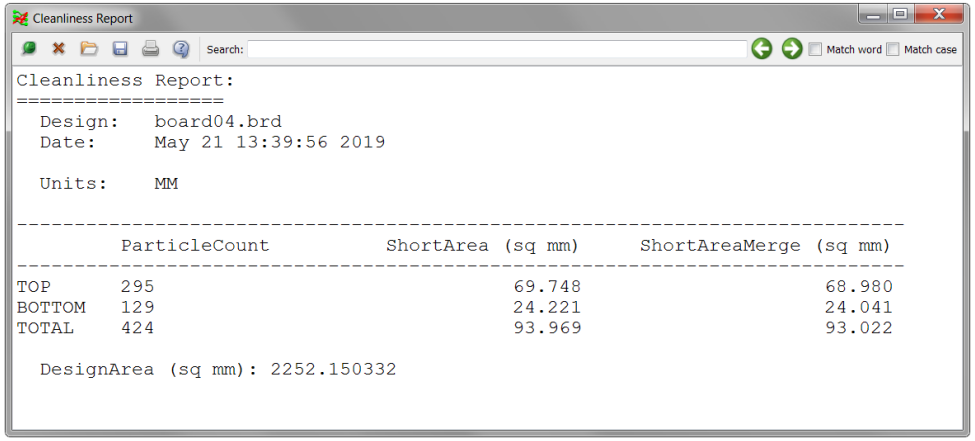




Technical Cleanliness

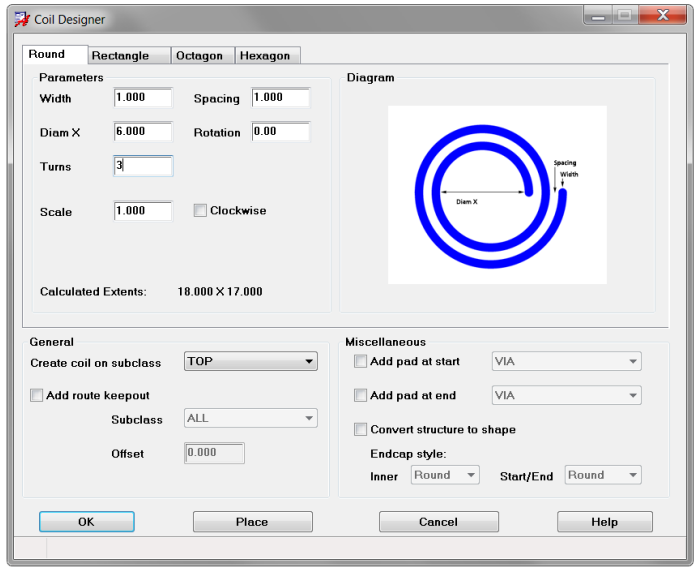
- Menu button Report
- Particle count per layer
- Short Area
  - Sum of particle shape areas from layer **CLNS_CONTACT_TOP (BOTTOM)**
- Short Area
  - Shape area on merged layer **CLNS_RESULT_TOP (BOTTOM)**
- Design Area
  - Area from **DESIGN_OUTLINE** minus **CUTOUT**

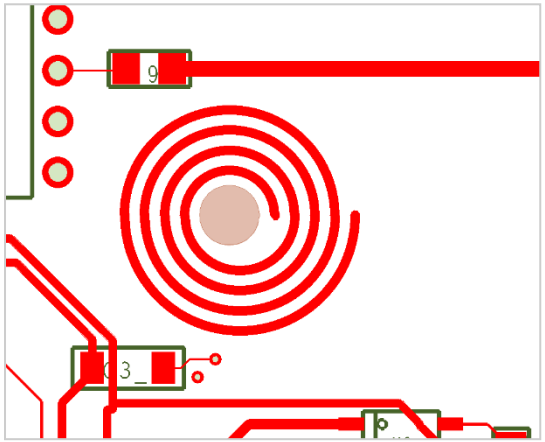




Coil Designer

- Includes useful functions when designing planar spiral inductors on a PCB
- Support for different spiral pattern
  - Round
  - Rectangle
  - Octagon
  - Hexagon
- Features
  - Parameterized input in terms of width, spacing, number of turns, etc.
  - Support for rotation, flipping and scaling
  - Dynamic preview during parameter change

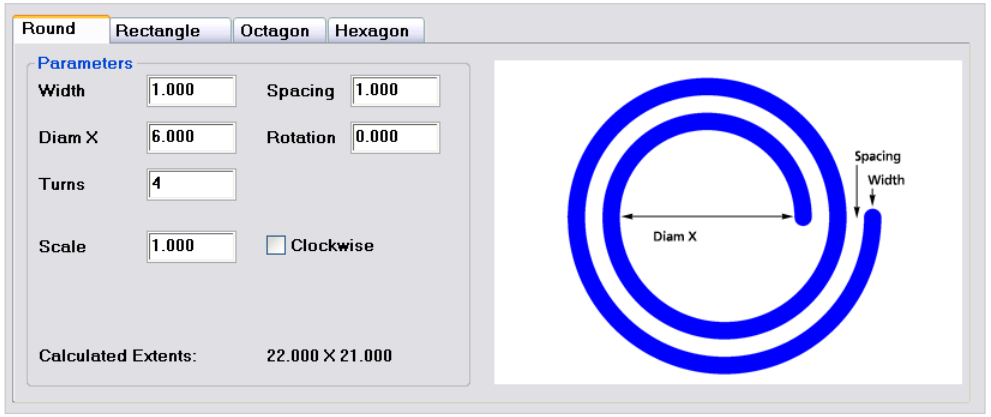




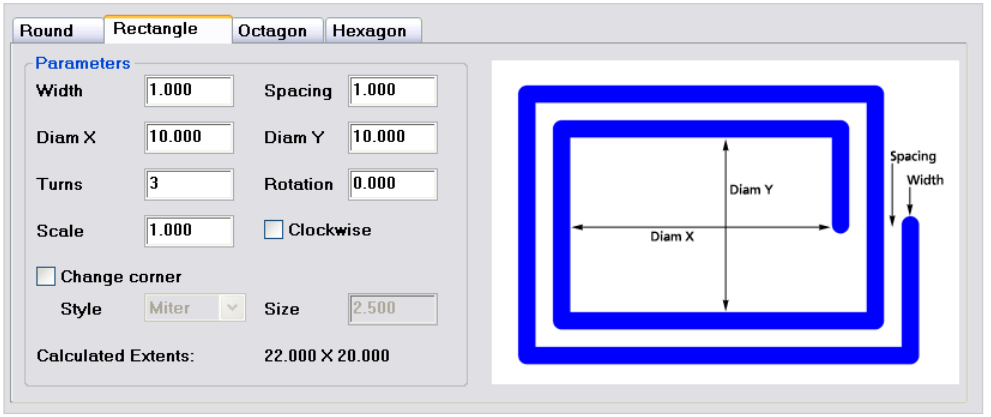
Coil Designer

Basic spiral patterns

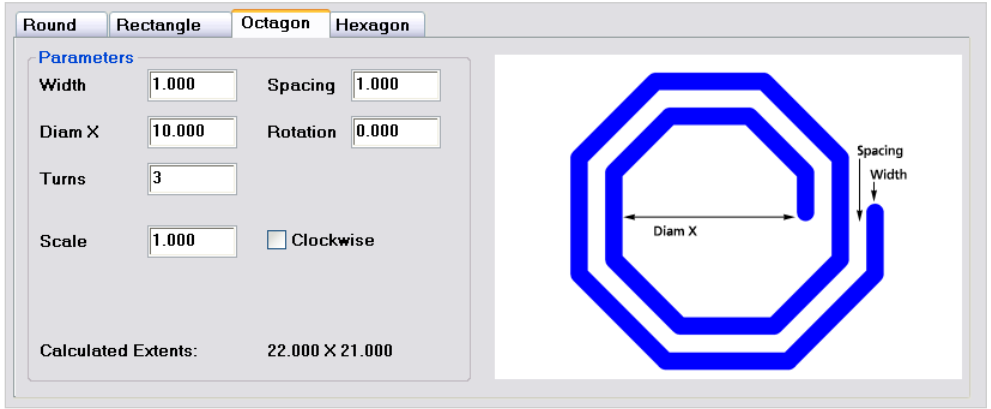
Round



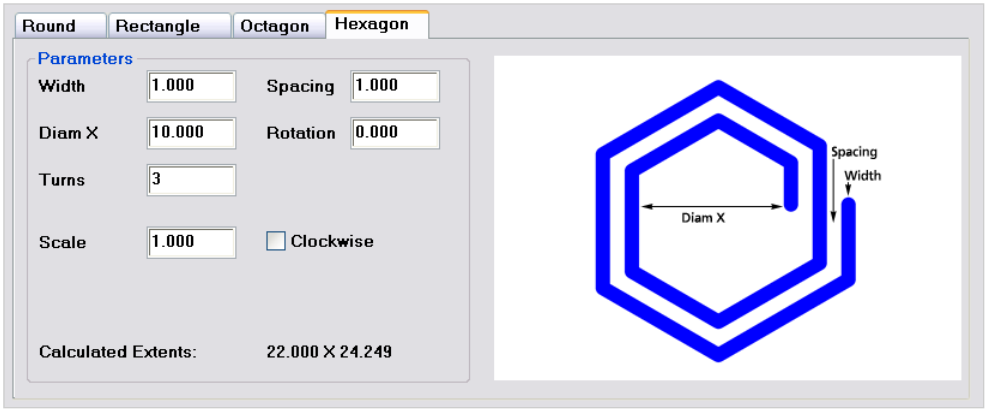
Rectangle



Octagon



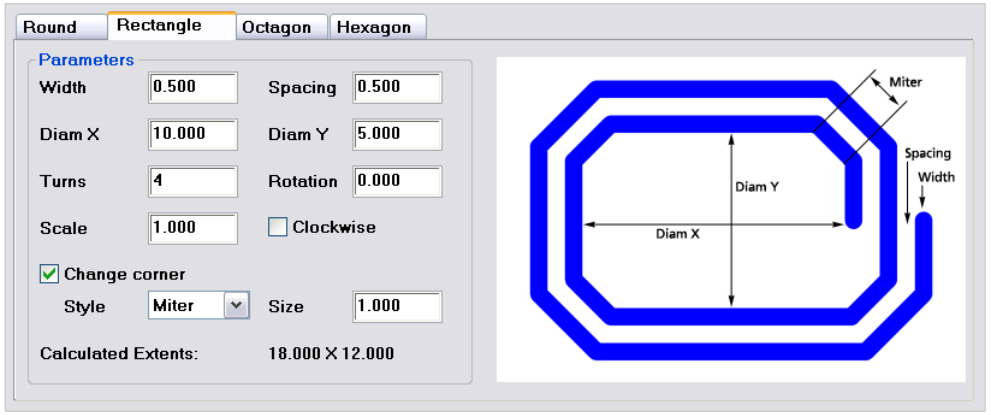
Hexagon

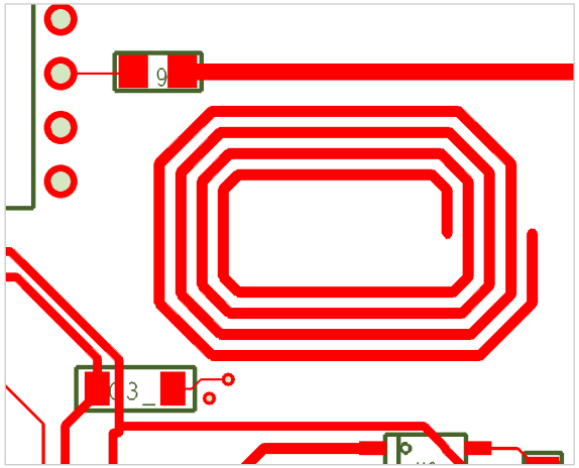


Coil Designer

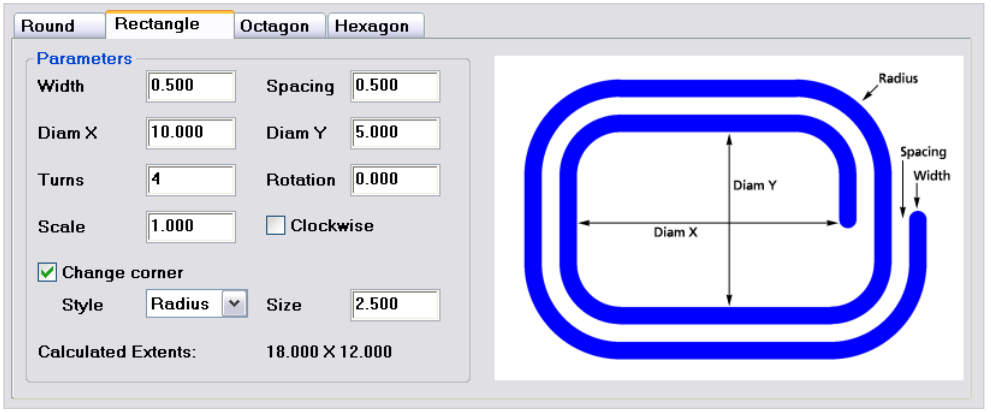
Rectangle spiral with corner modifications

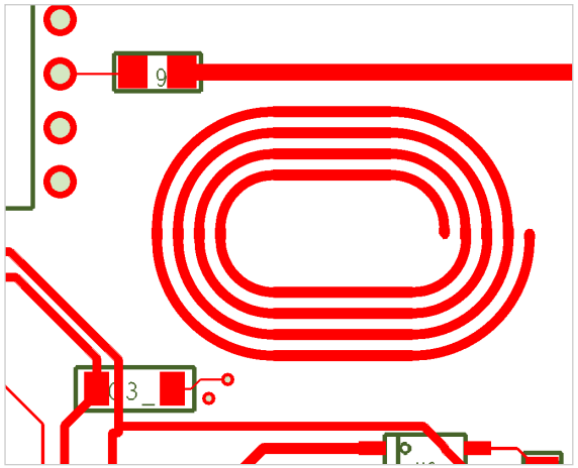
Mitered corners





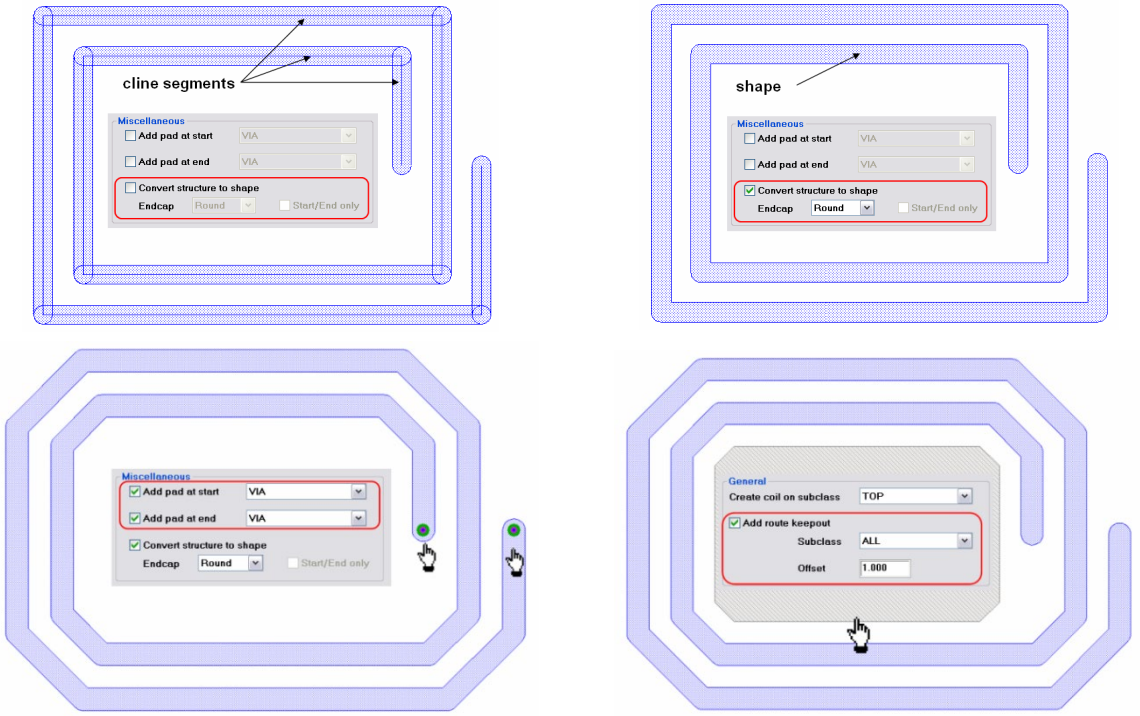
Rounded corners





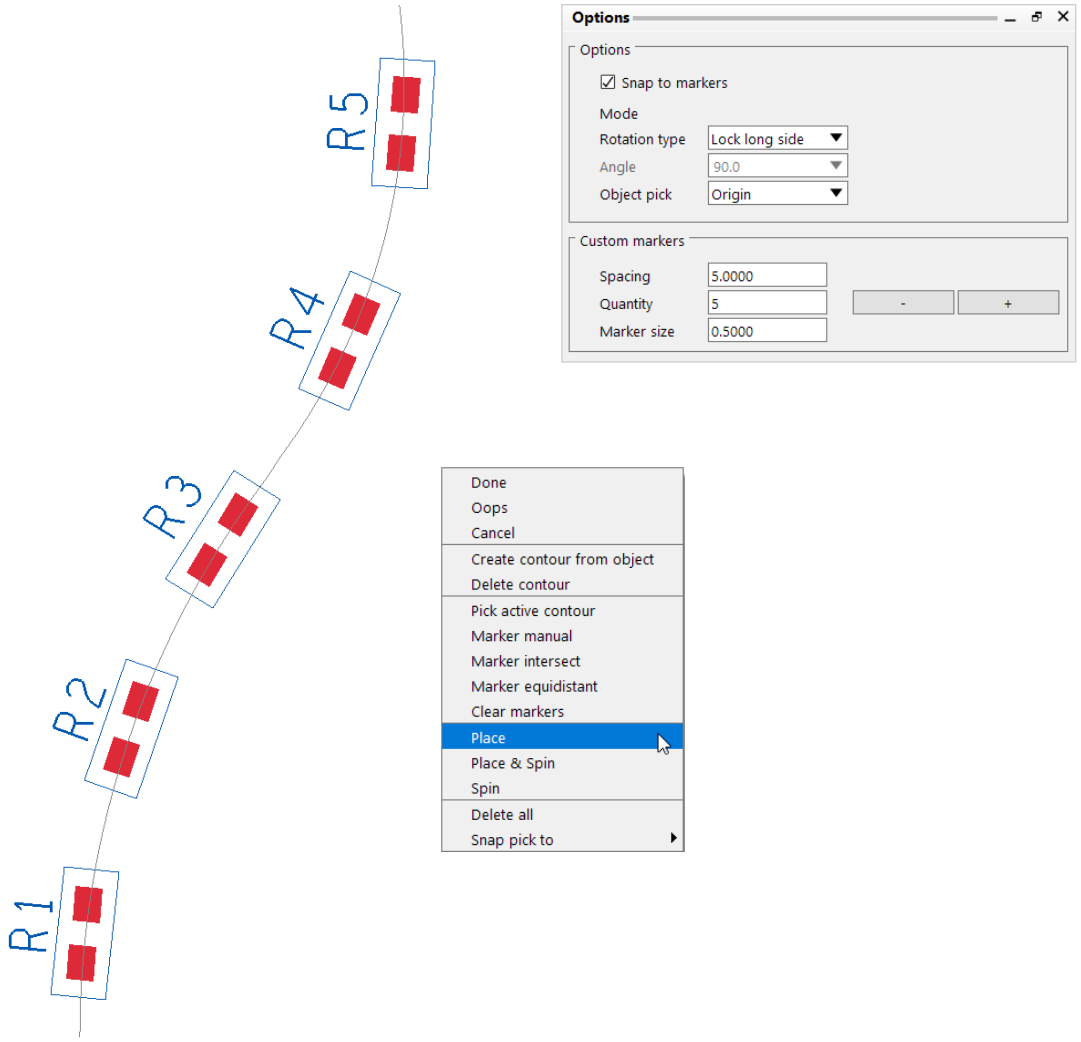
Coil Designer

- Other features
  - Realization as a combination of cline segments or one single shape
  - Addition of padstacks to the start / end points
  - Automatic generation of route keepouts in the inner area



Contour Place

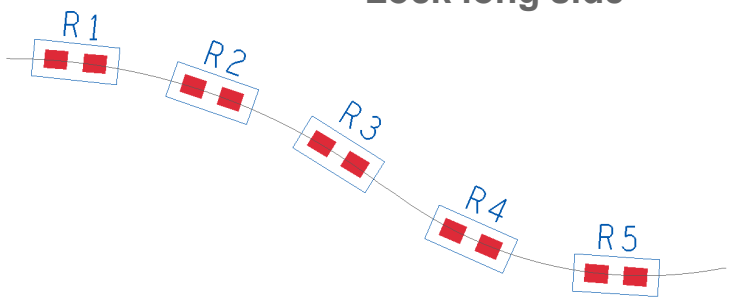
- Interactive placement along contour
  - Automatic snap to contour path
  - Place, Place & Spin, Spin
- Various alignment options
  - Lock long side
  - Lock short side
  - Relative
  - Absolute
- Custom snap marker
  - For accurate control
  - Manual markers
  - Markers by intersection
  - Equidistant markers

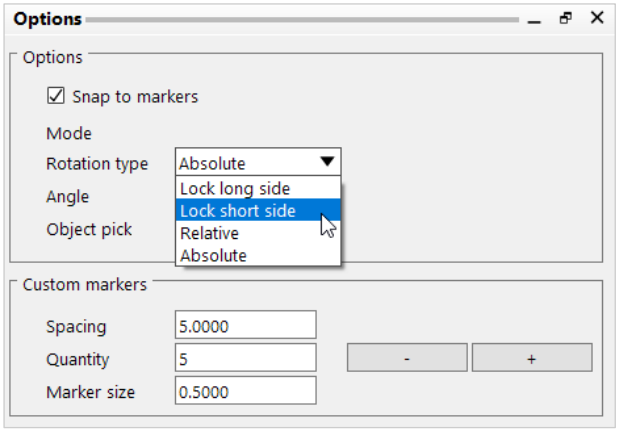


Contour Place

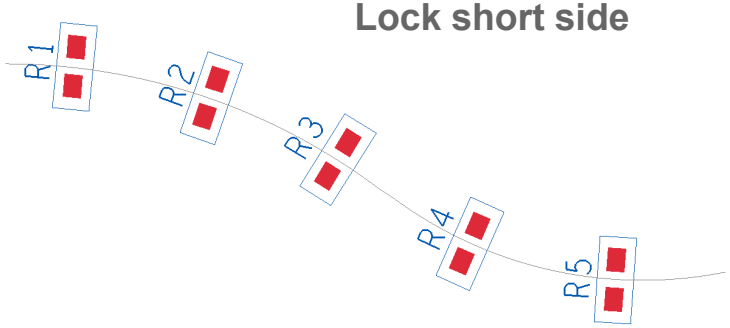
- Alignment options

Lock long side

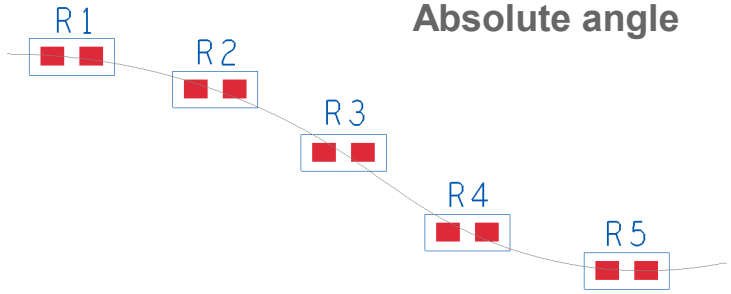




Lock short side

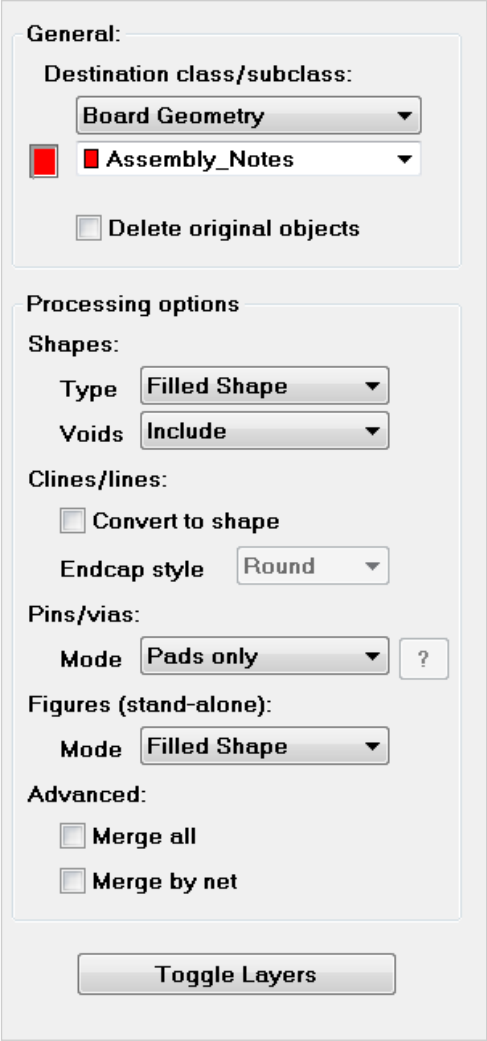


Absolute angle



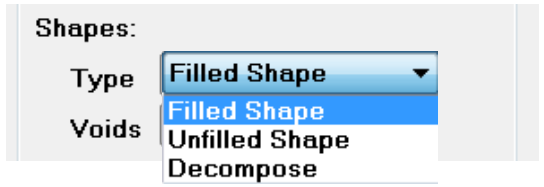
Cross Copy

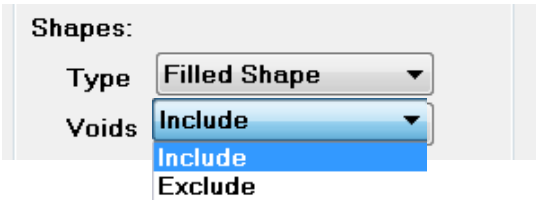
- **Problem**
  - Customer needs to move objects from one class / subclass to another
  - Command **Edit > Copy** does not support a destination layer
  - Customer gets error messages, e.g. **E – Changing shape to a different class is not supported**
  - Customer has to find workarounds (e.g. export subdrawing, text edit clipboard file, import subdrawing)
- **Solution**
  - **Cross Copy** closes the gap
  - Can move or copy objects to any destination layer for various purposes
  - In contrast to **Create Detail,** objects are not destroyed (e.g. text will stay text!)

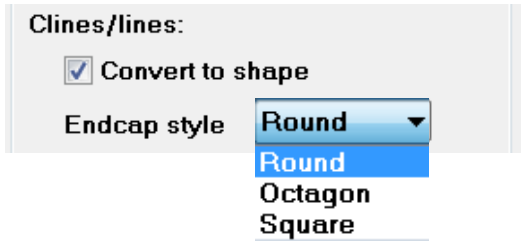


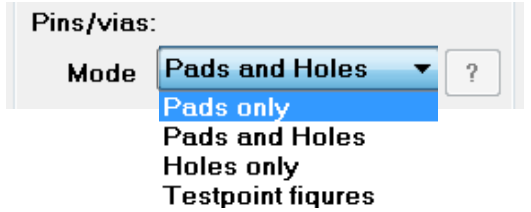
Cross Copy

- Advanced features
  - Shape processing
    - Include / exclude voids
    - Fill or decompose with / out voids
    - Unfill shape
  - Clines / lines processing
    - Can be converted to shape
    - Various endcap types
  - Padstack processing (pins and vias)
    - Drawn as shape on destination layer
    - All visible layers are merged
    - Resulting pad shape can be voided by drill hole information
  - Merging support
    - Selected data (find filter settings) is merged





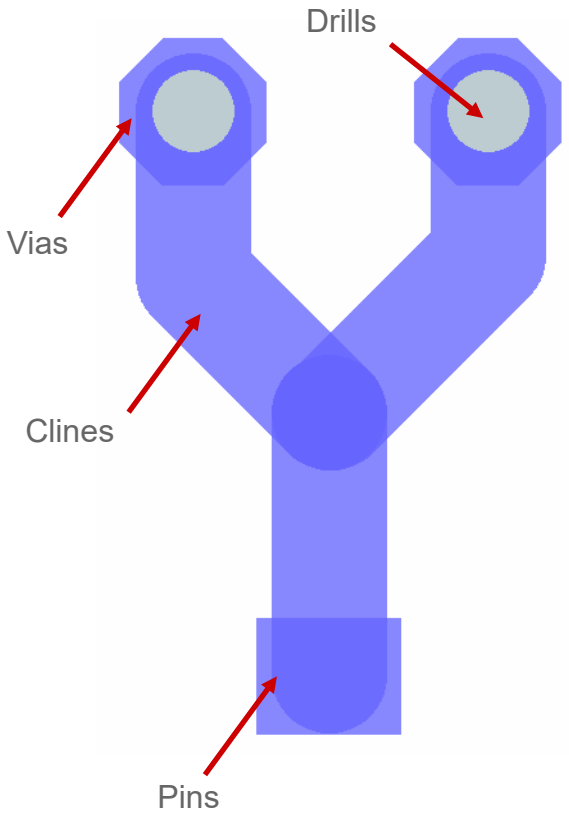


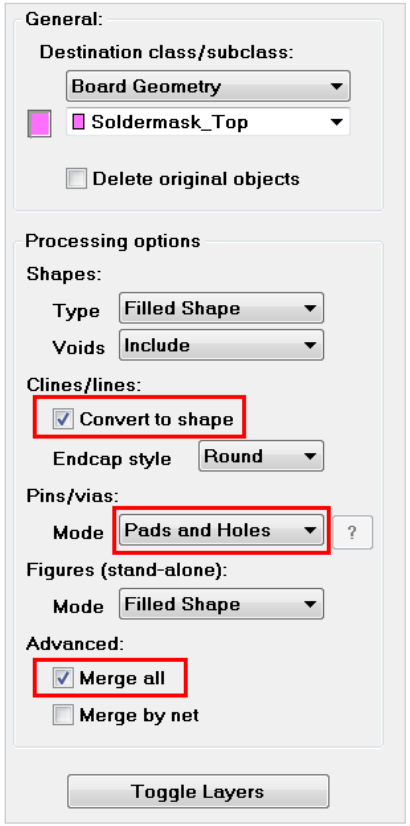


Cross Copy

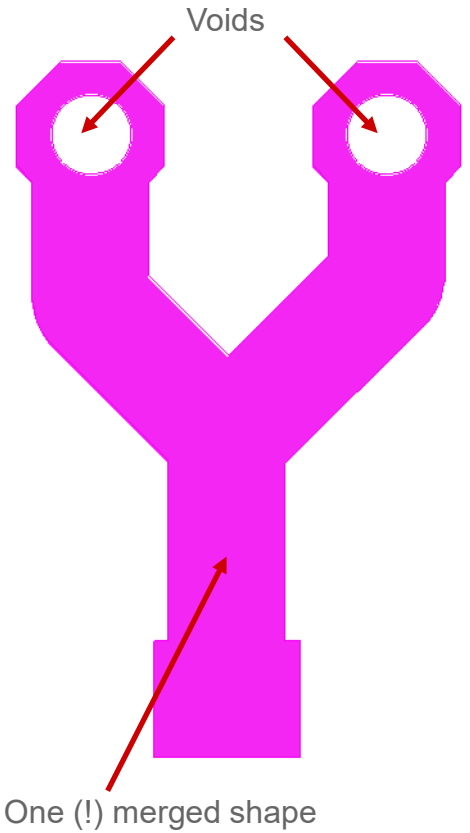
Example: Merging data to soldermask shape

Selection



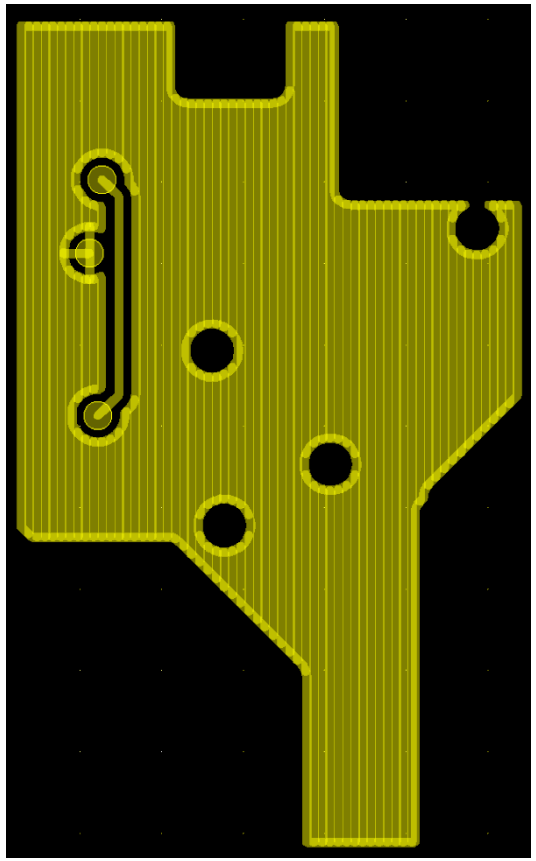


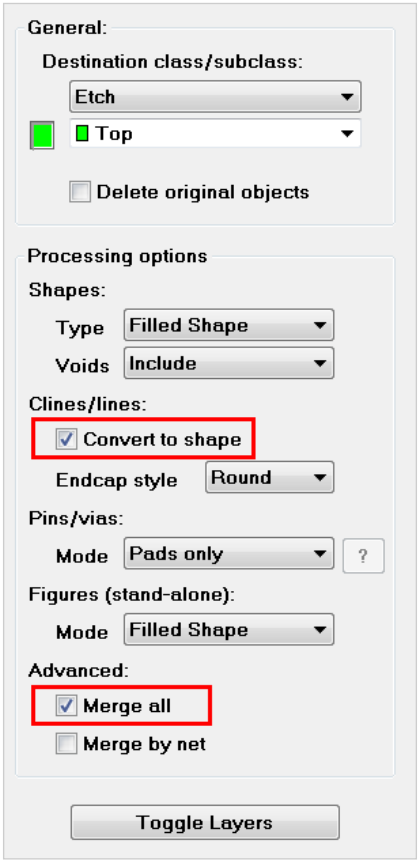
Result

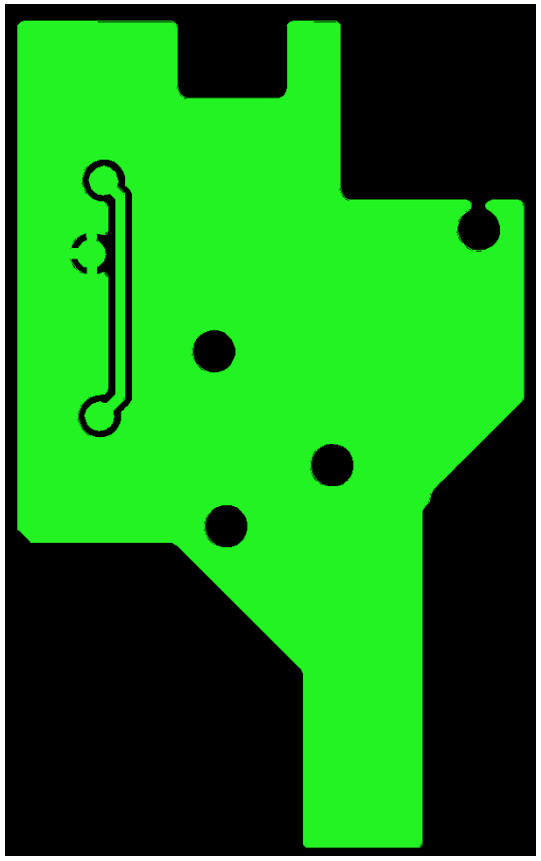


Cross Copy

Example: Converting pseudo shapes (stroked lines) to real shapes



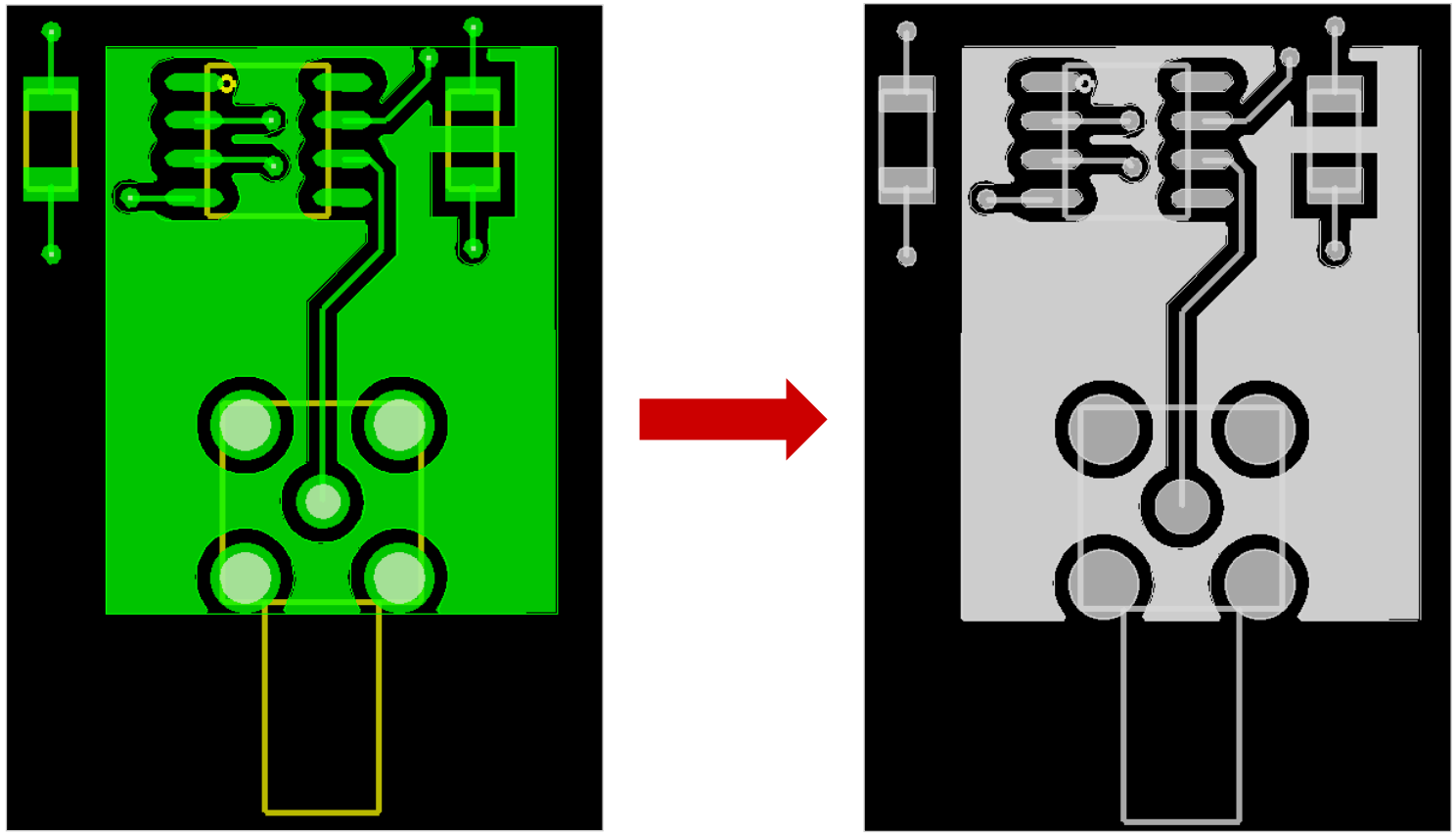




Note: Typical situation after importing third party Gerber data into Allegro – copper needs to be reanimated!!!

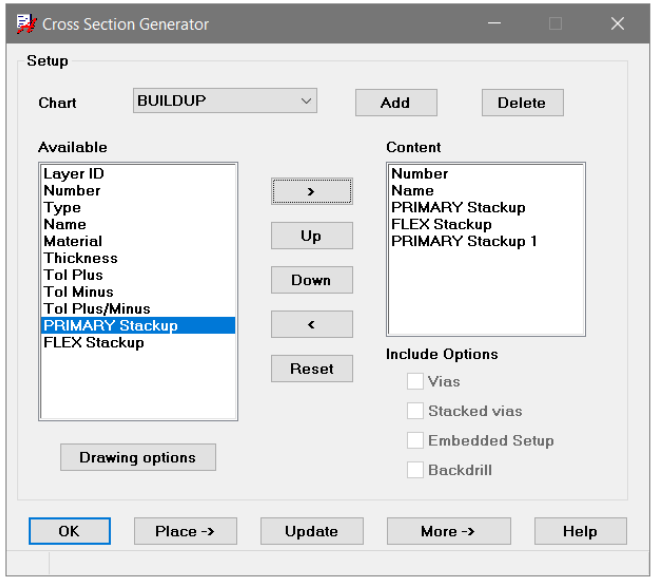
Cross Copy

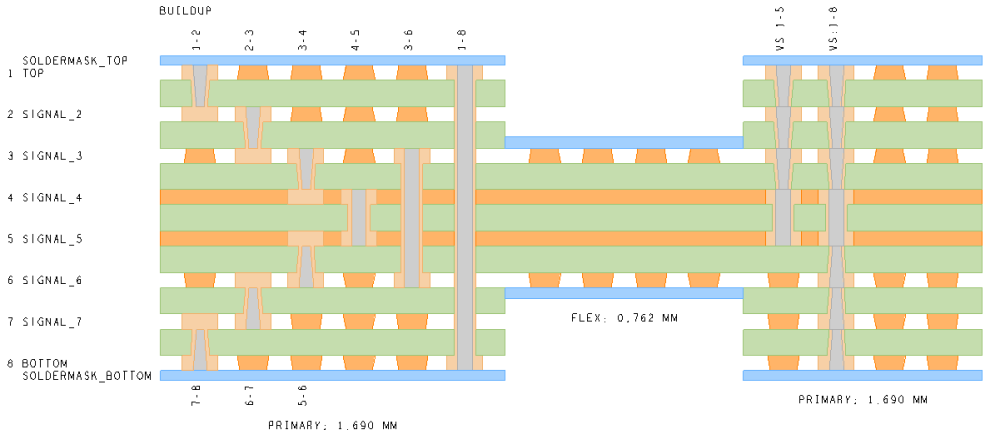
Example: Backup data on Board Geometry / Assembly_Notes for documentation purposes



Cross Section Generator

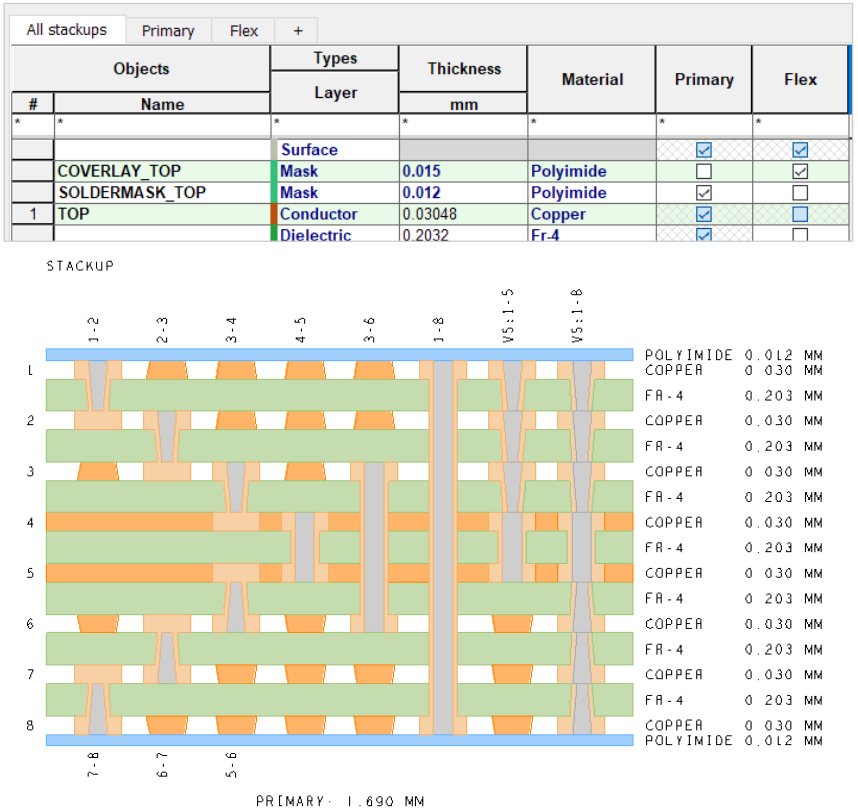
- Enhanced support for rigid-flex applications
- Customizable content
  - Custom charts with more meaningful visualization
  - Layer attributes, order, …
  - Colors, fill styles, …
  - Vias, stacked vias, backdrill and embedded status support
- SVG export
  - Export graphics for documentation purposes
- Configuration stored in db
- Automatic update

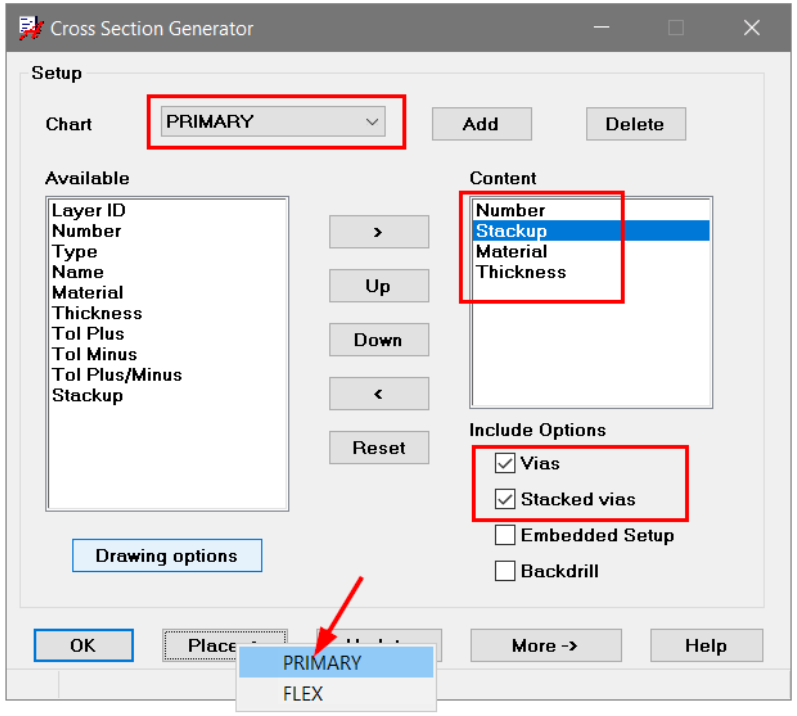




Cross Section Generator

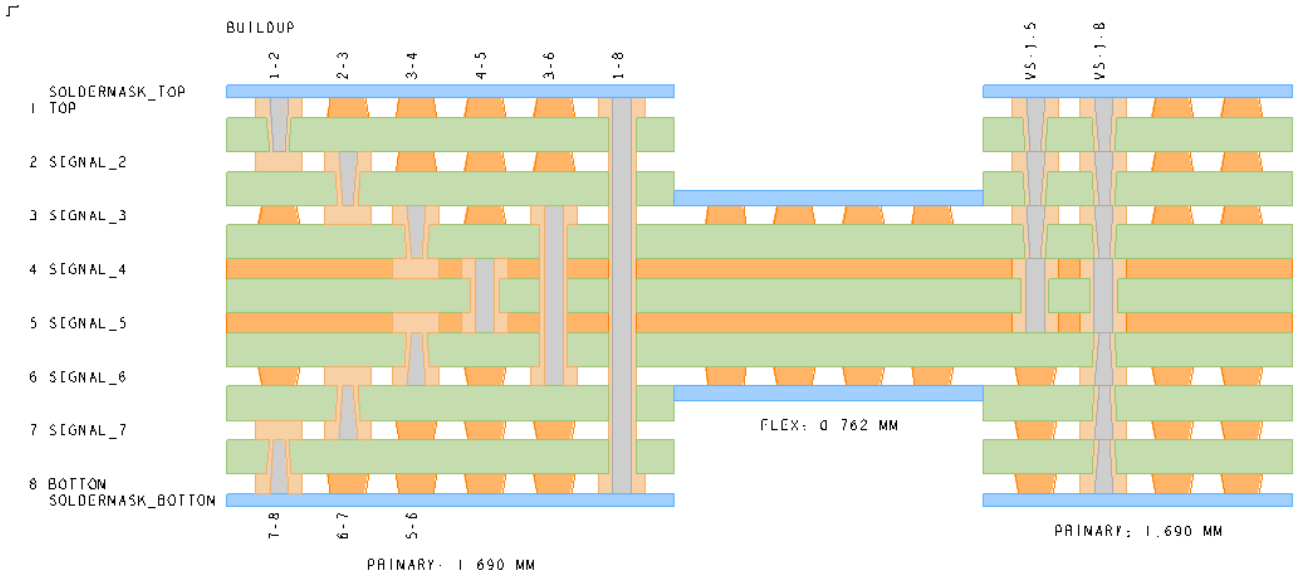
- Content can be defined for each stackup from cross section individually
- Also symbols can be placed individually

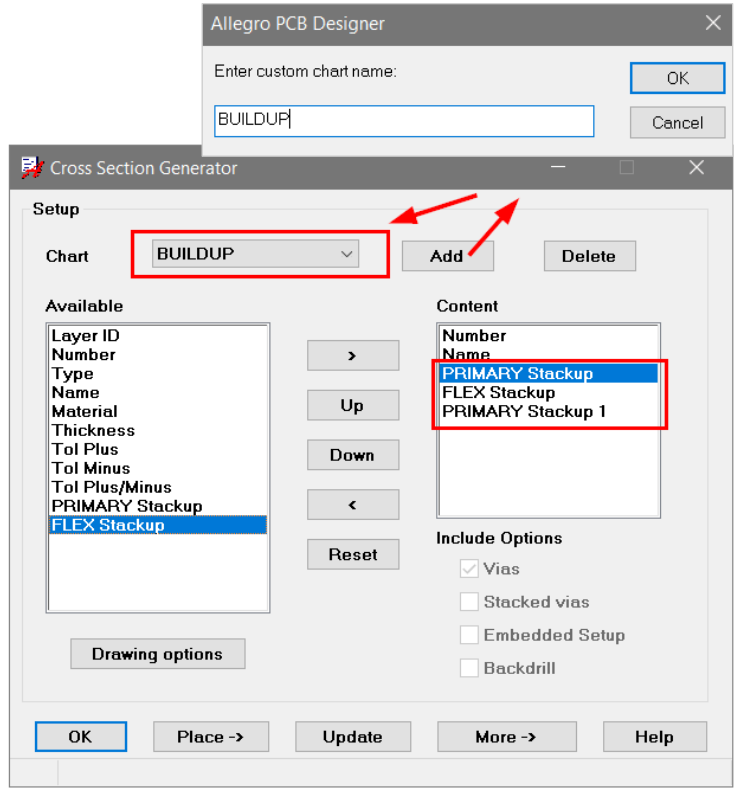




Cross Section Generator

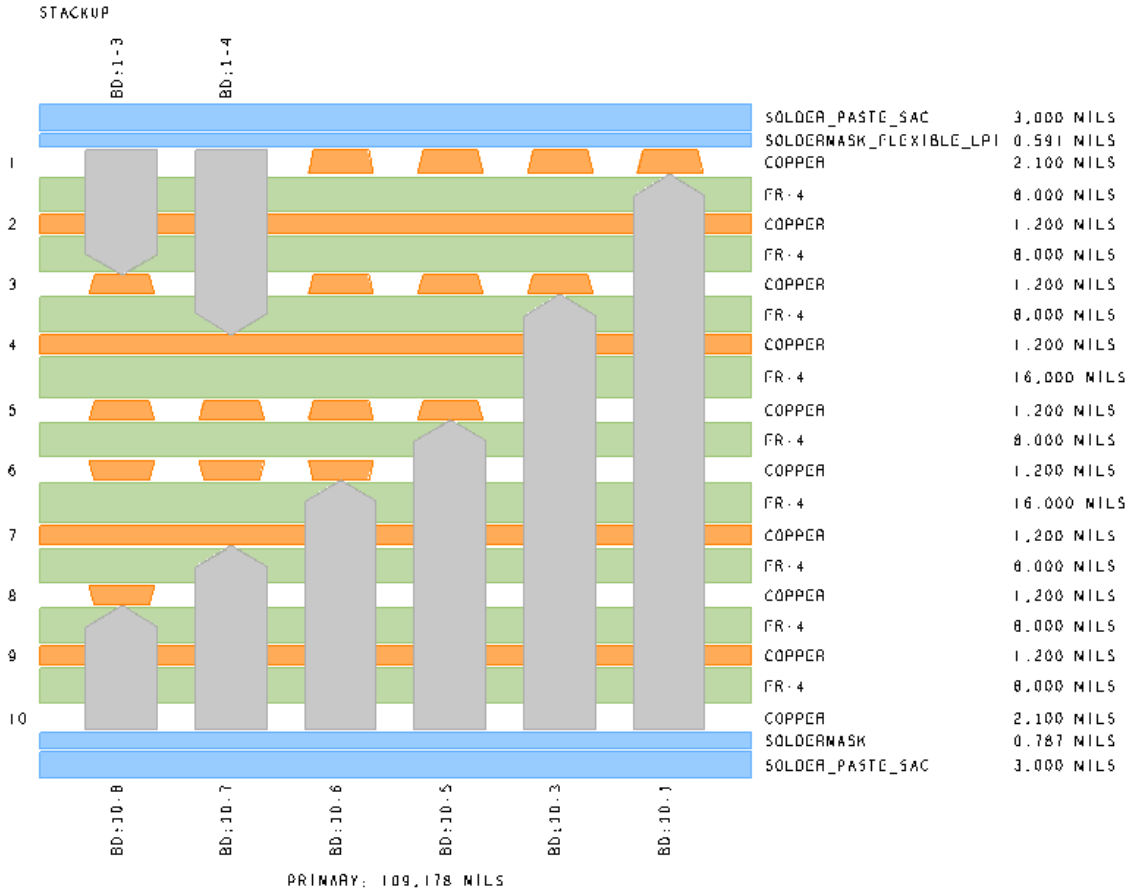
- A custom chart let's you combine stackups in an arbitrary order
- Feature many customer were asking for ...
- Additional information (vias, stacked vias, etc., can be applied to each stackup item individually)

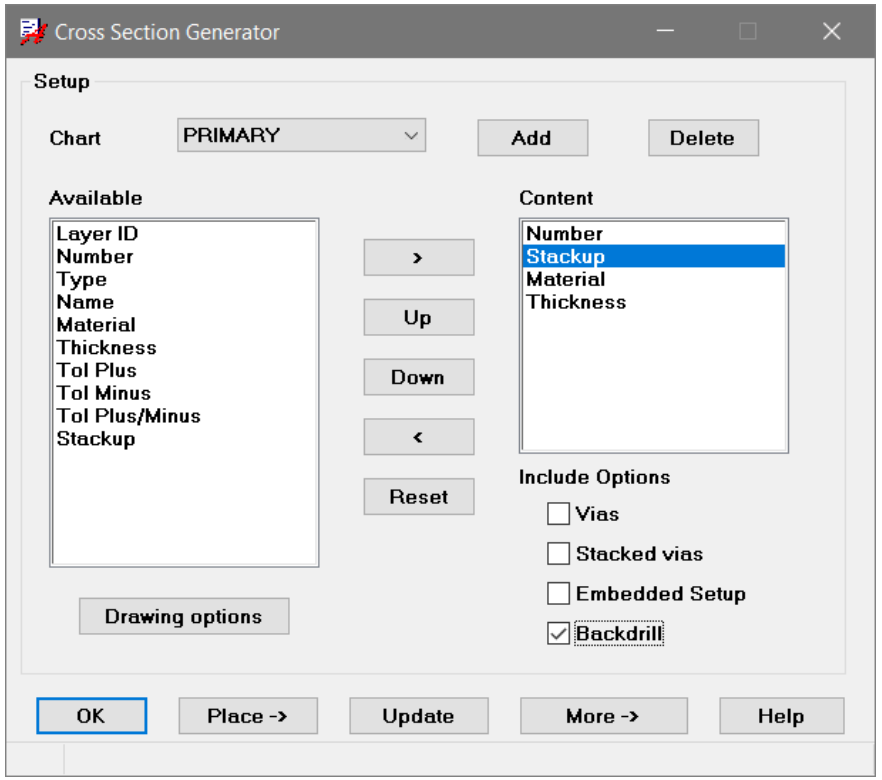




Cross Section Generator

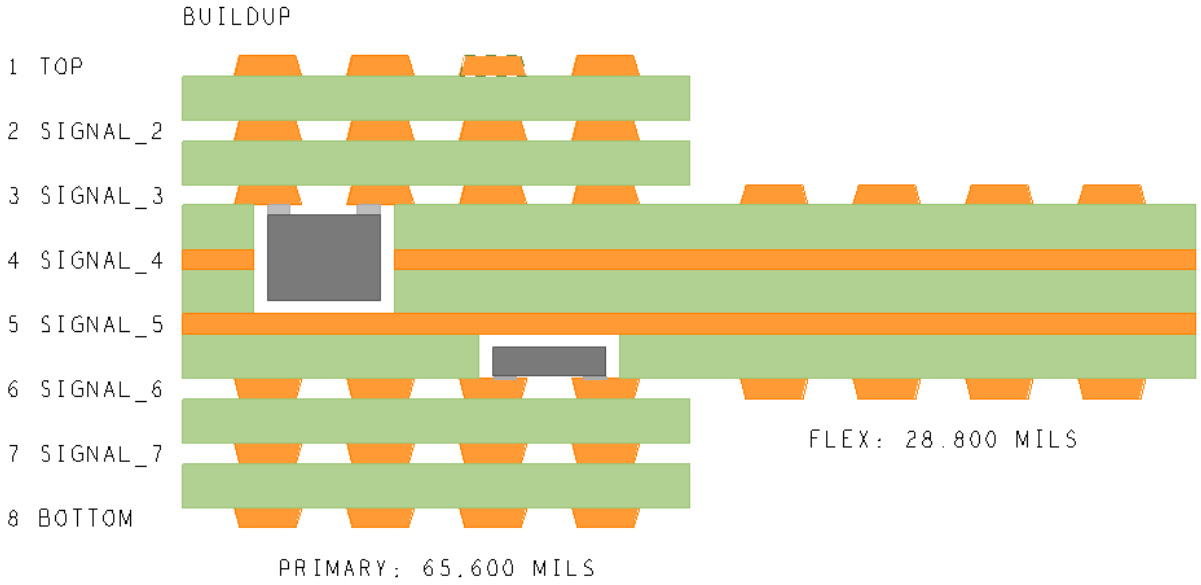
- Backdrill support

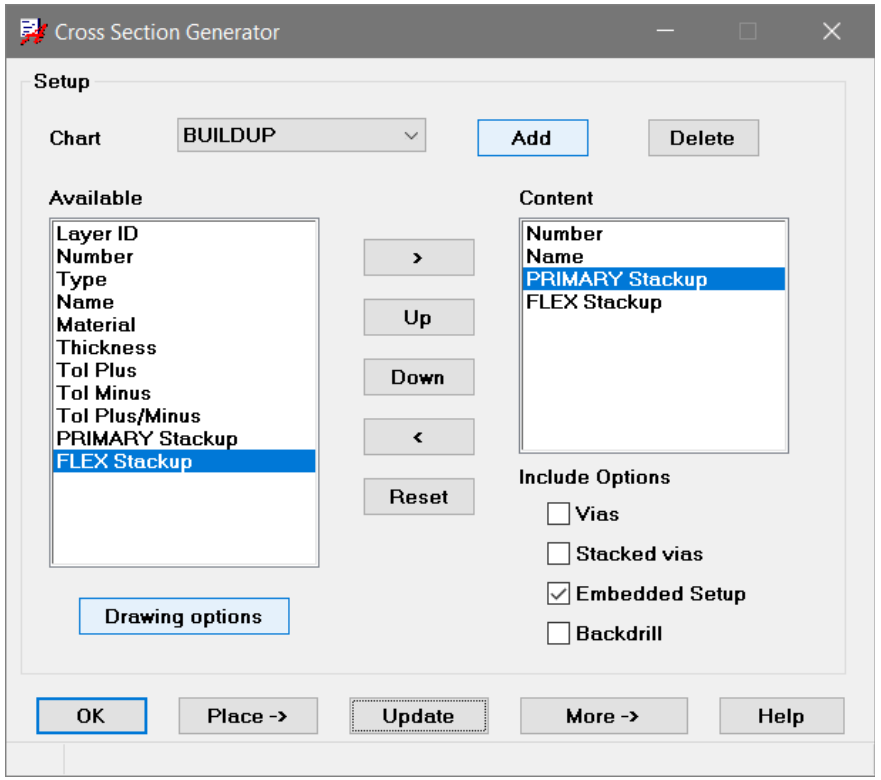




Cross Section Generator

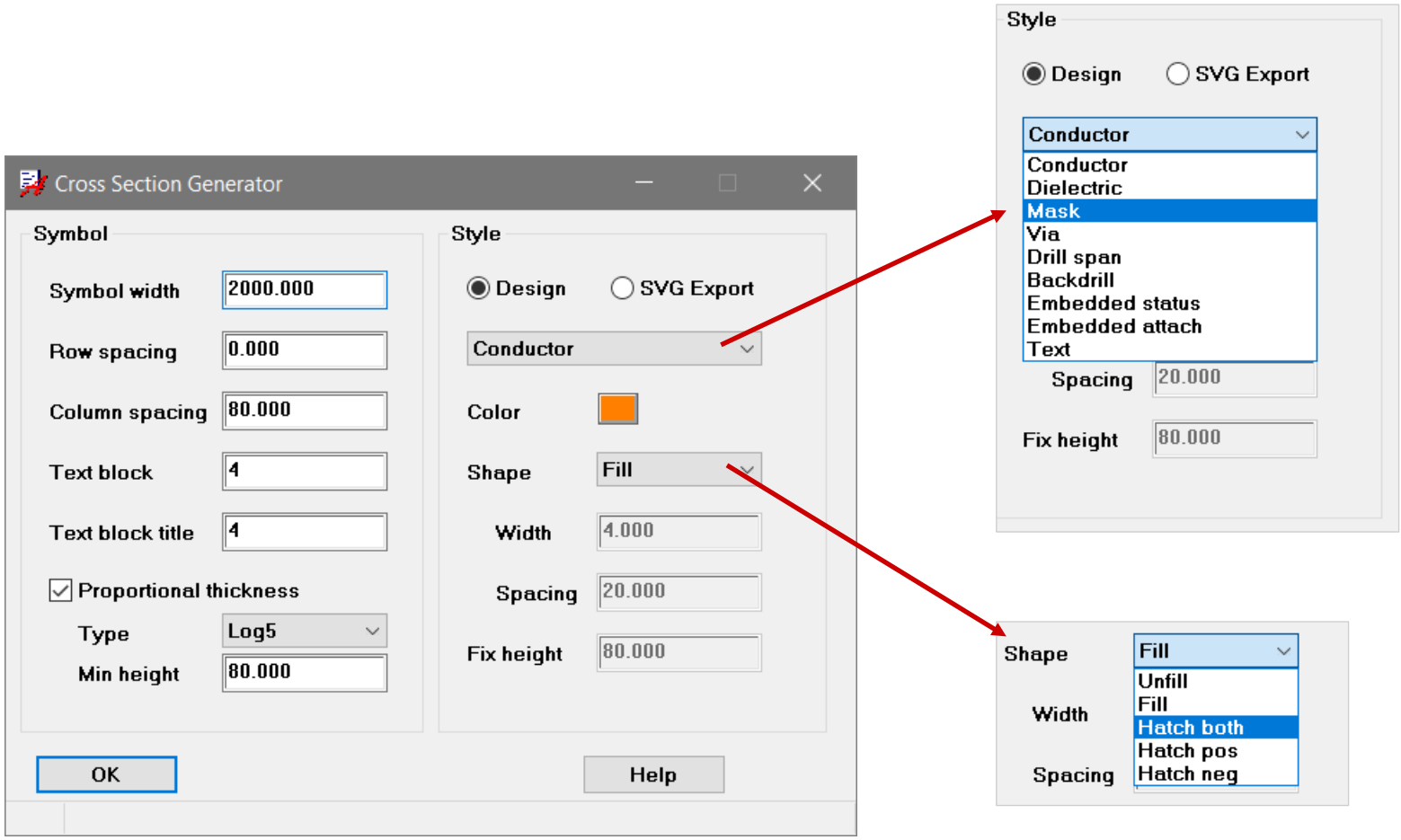
- Embedded component support





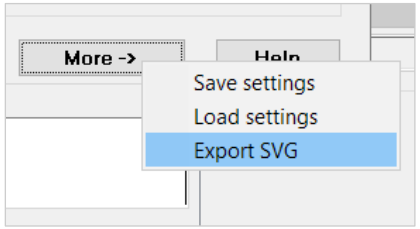
Cross Section Generator

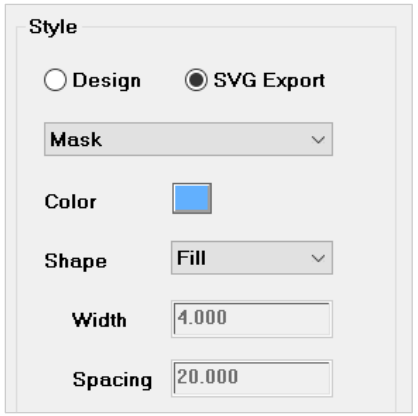
- Various drawing options

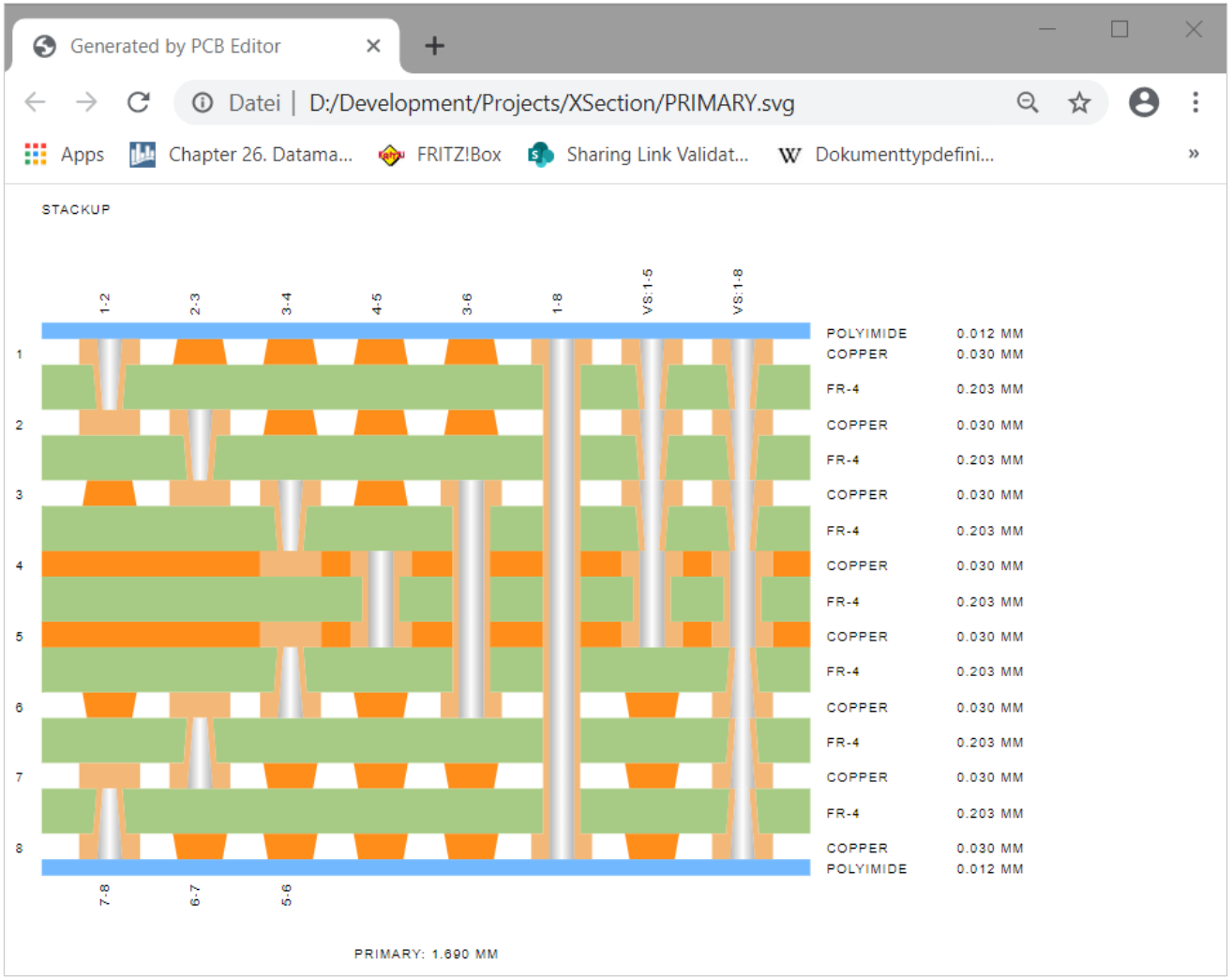


Cross Section Generator

- Export SVG
  - Mainly for documentation purposes
  - Separate color profile can be defined

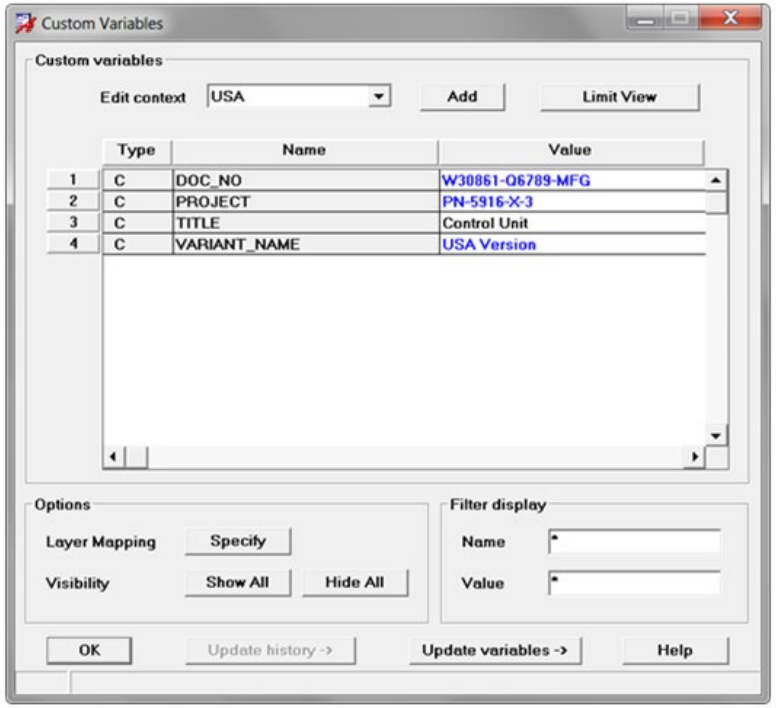


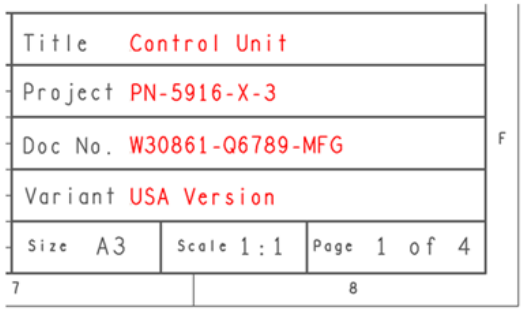




Custom Variables

- User defined variables in PCB Editor, useful for title blocks, etch texts etc.
- Similar to Design Entry HDL
- Automatic update of variables across all subclasses
- Variant support
- History capabilities
- Variable values can be sourced from external control file or even cpm-file





Custom Variables

Define Placeholders

Parameters

Variable name:

PART_NUMBER

Display value:

<PART_NUMBER>

Destination layer

Drawing Format

Title_Block

Attributes

Block 3 Rot 0.0000

Align Left Mirror No

Advanced

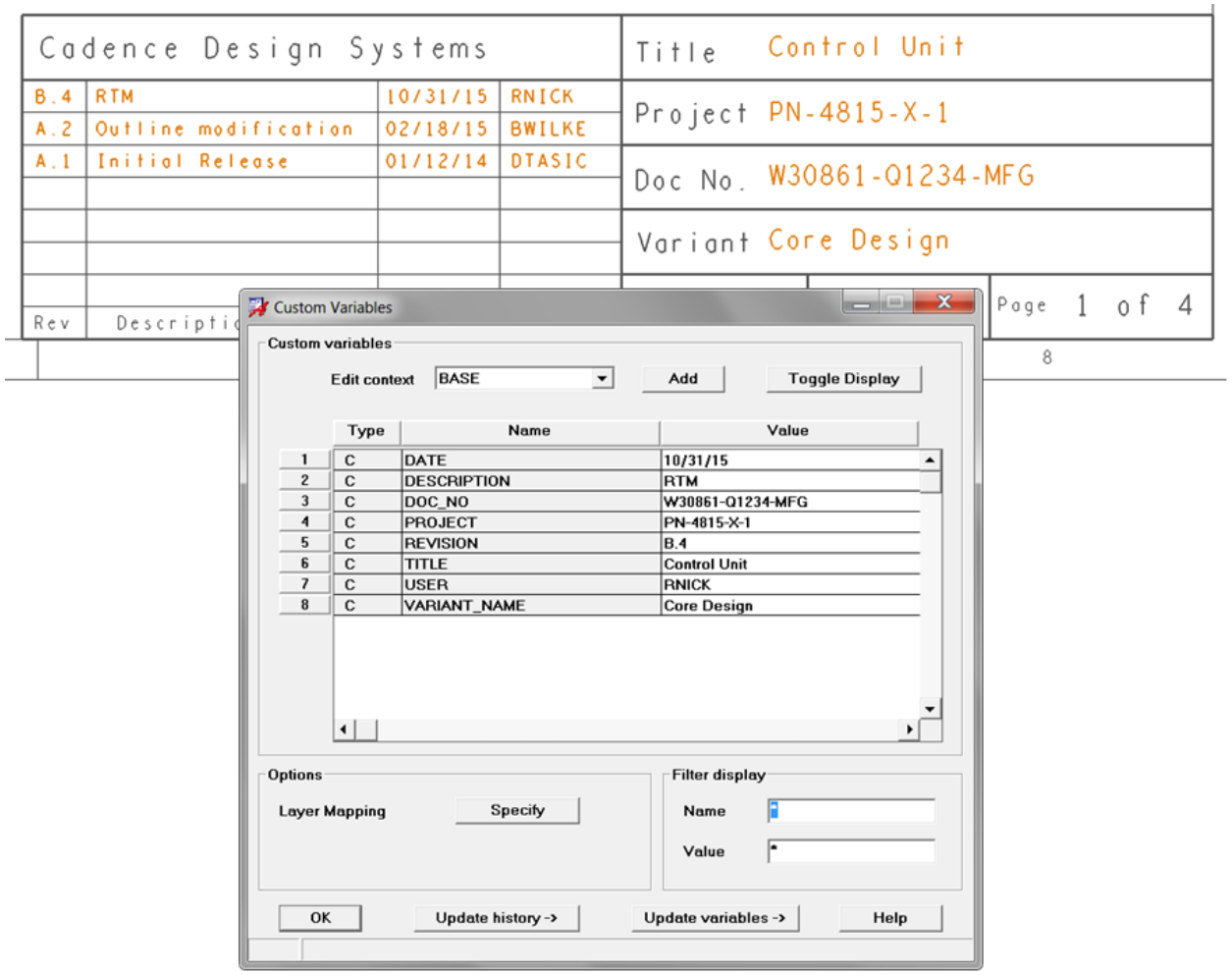
Type Standard

History None

Mode

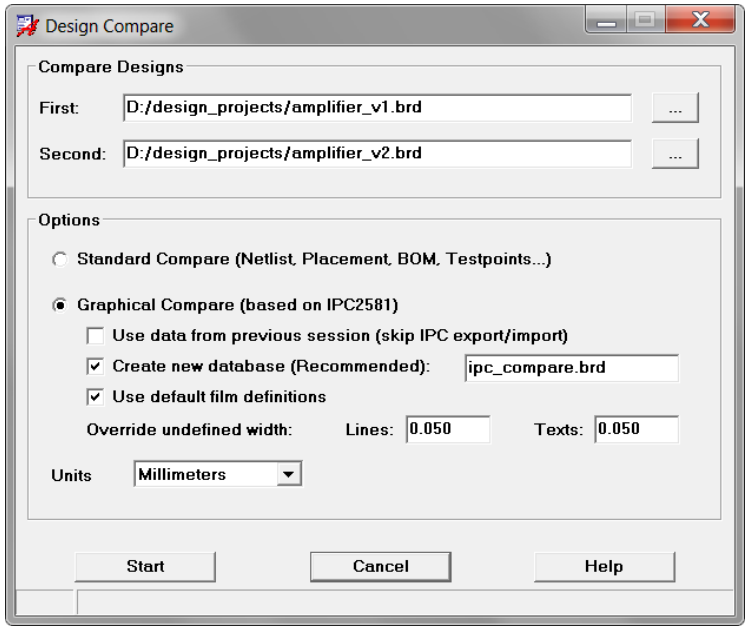
- Add placeholder
- Modify placeholder
- Delete placeholder

Update Example



Design Compare

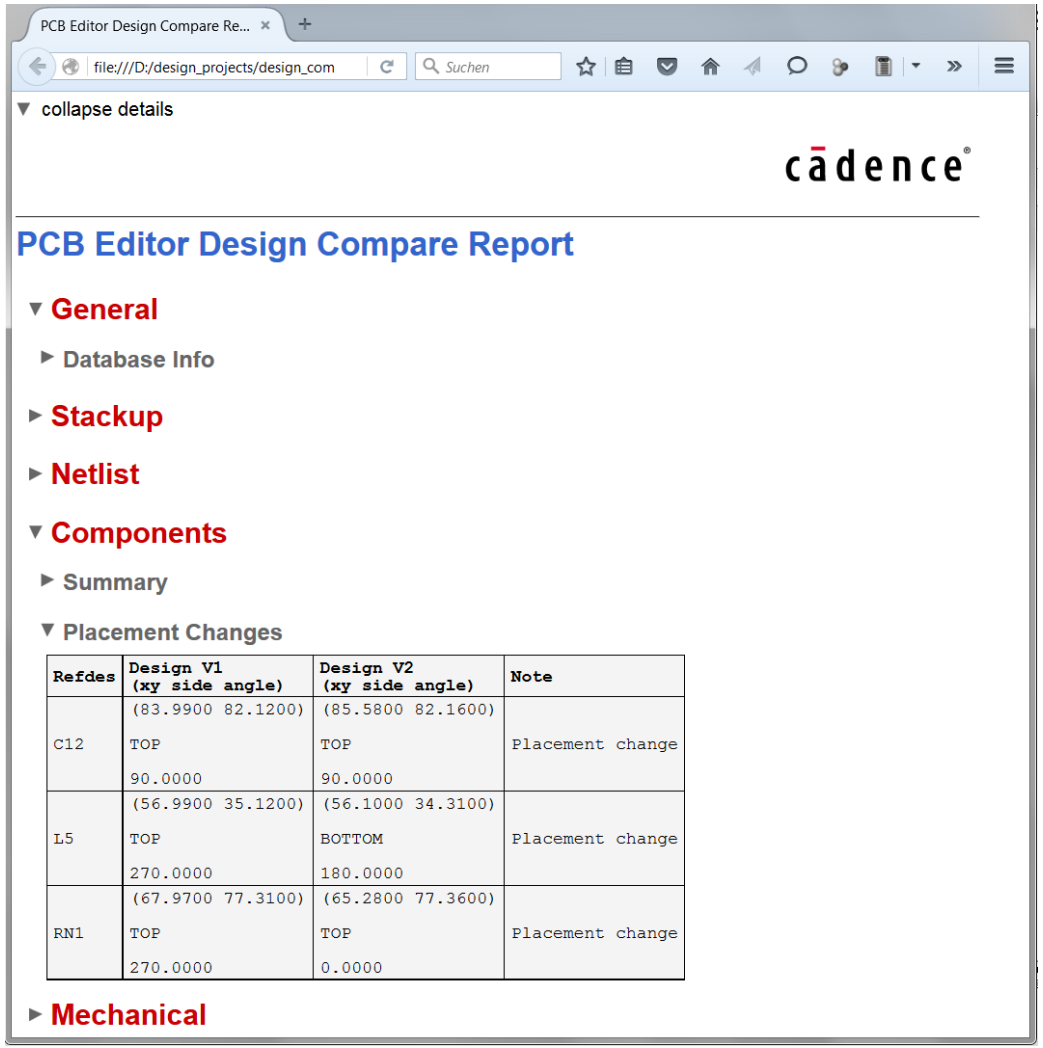
- Compares two databases and identifies the differences
- Useful when tracking changes in the product lifecycle
- Two modes
  - **Standard Compare**
    Generates an HTML report with differences that apply to netlist, placement, BOM, testpoints, etc.
  - **Graphical Compare**
    Based on IPC-2581 all or individual layers can be compared graphically, differences will be highlighted, markers can be generated



Design Compare

Standard Compare

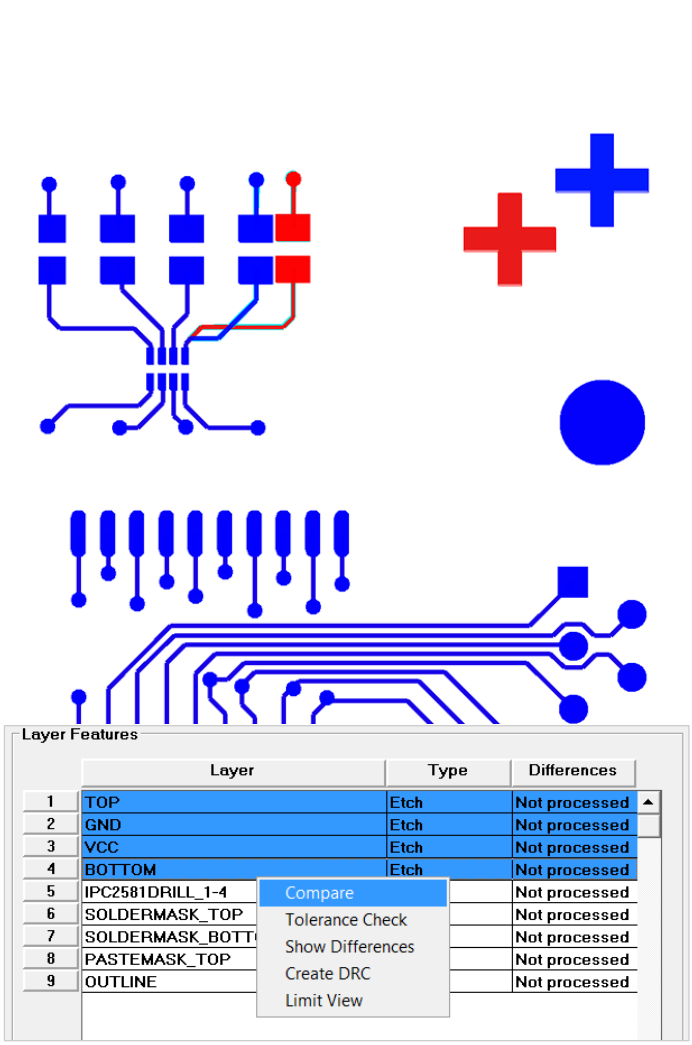
- HTML based report
- Expand / collapse functionality facilitates navigation

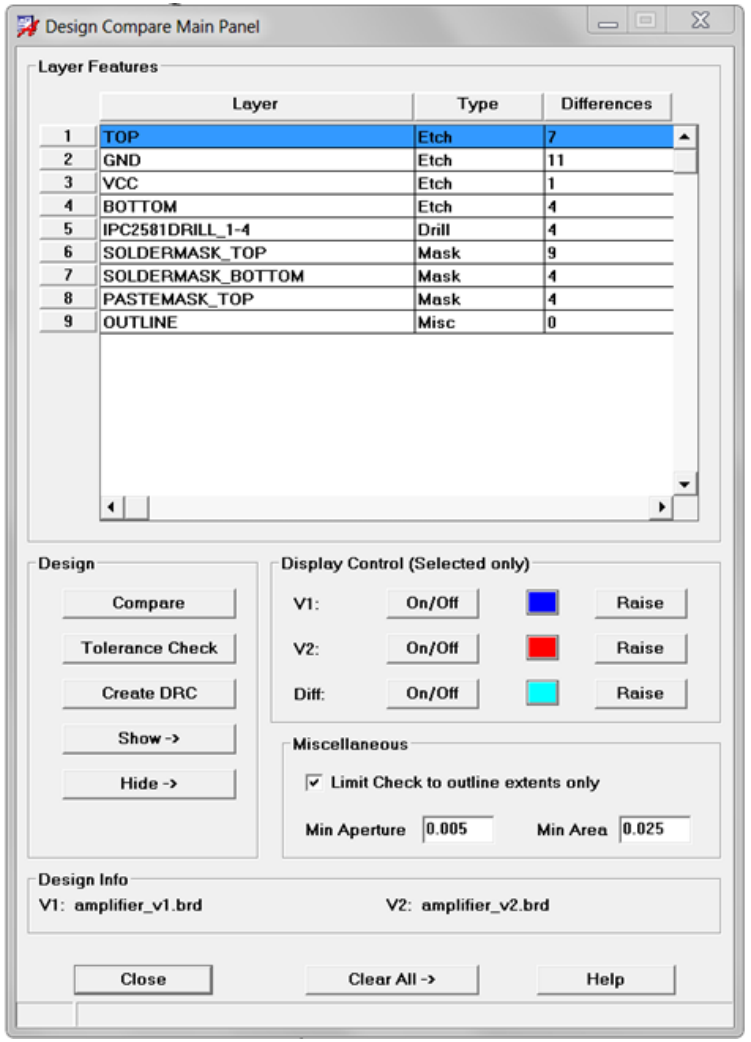


Refdes	Design V1 (xy side angle)	Design V2 (xy side angle)	Note
C12	(83.9900 82.1200) TOP 90.0000	(85.5800 82.1600) TOP 90.0000	Placement change
L5	(56.9900 35.1200) TOP 270.0000	(56.1000 34.3100) BOTTOM 180.0000	Placement change
RN1	(67.9700 77.3100) TOP 270.0000	(65.2800 77.3600) TOP 0.0000	Placement change

Design Compare

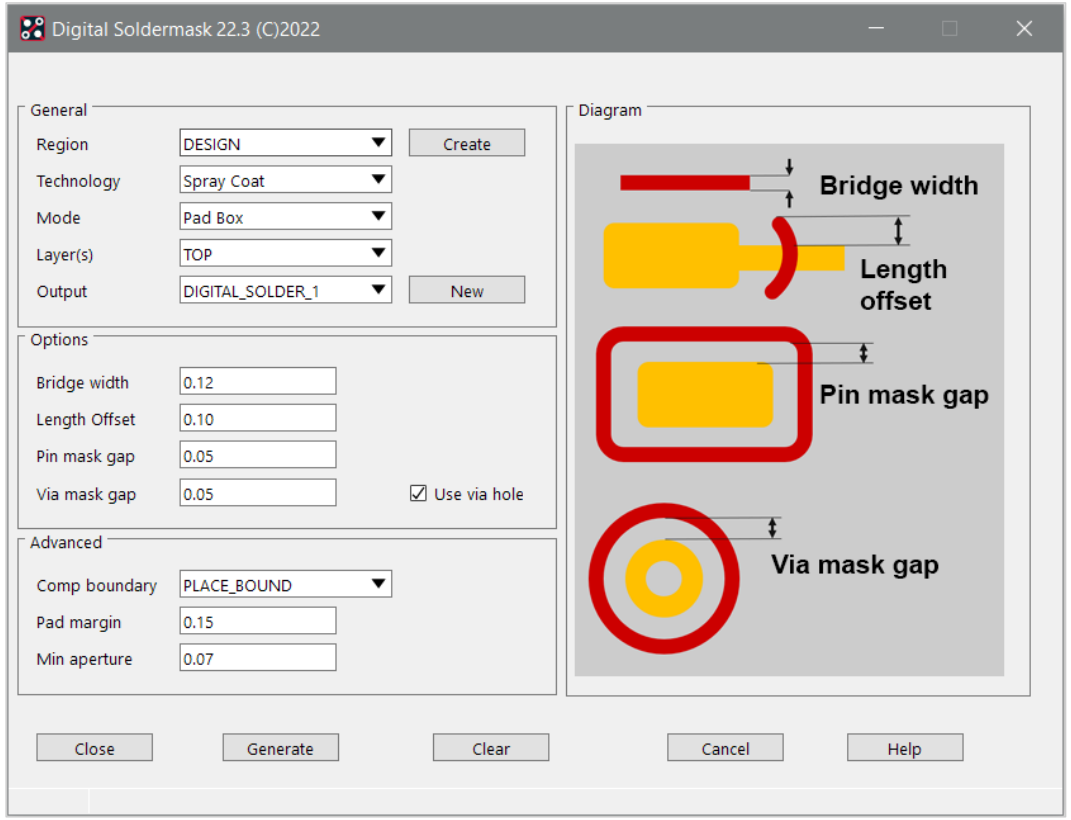
Graphical Compare





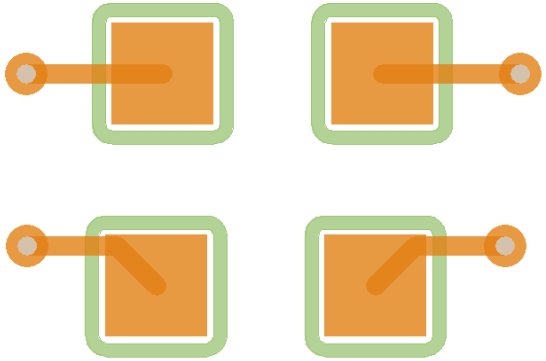
Digital Soldermask

- Additional features accounting for new technologies
- Developed together with Würth Elektronik
- Various modes
  - Pad ring / box
  - Trace mode
  - Component mode
  - By region
- Parameters
  - Bridge width
  - Pin, via gap
  - Length offset
  - …

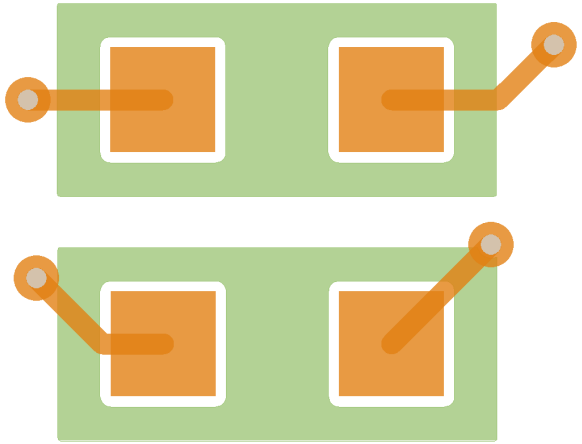


Digital Soldermask

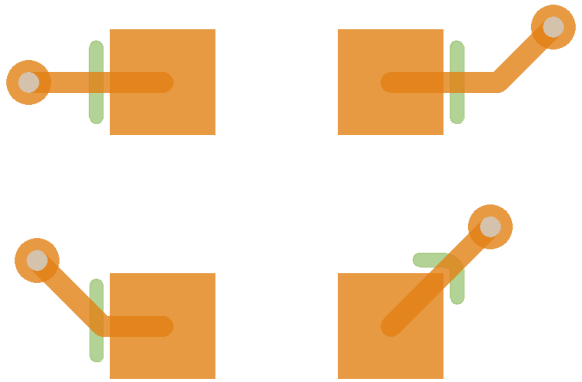
Pad box



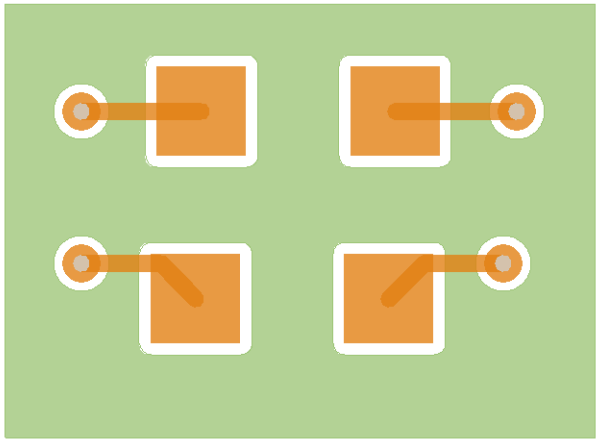
Component boundary



Trace mode



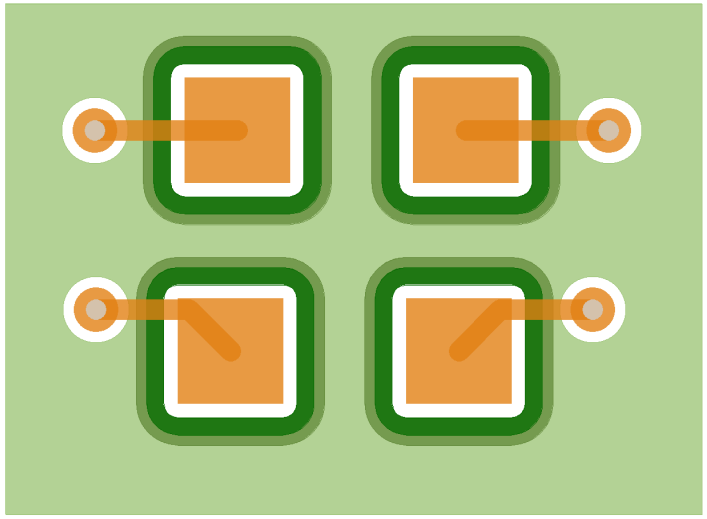
Soldermask region



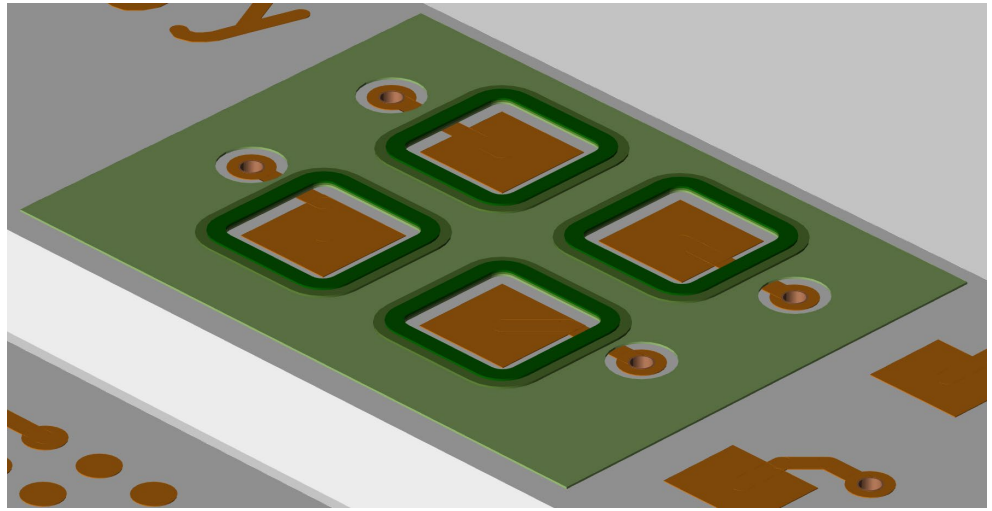
Digital Soldermask

- Techniques can be combined and used to create multiple masks on separate layers, accounting for mask thickness and thickness requirements

2D



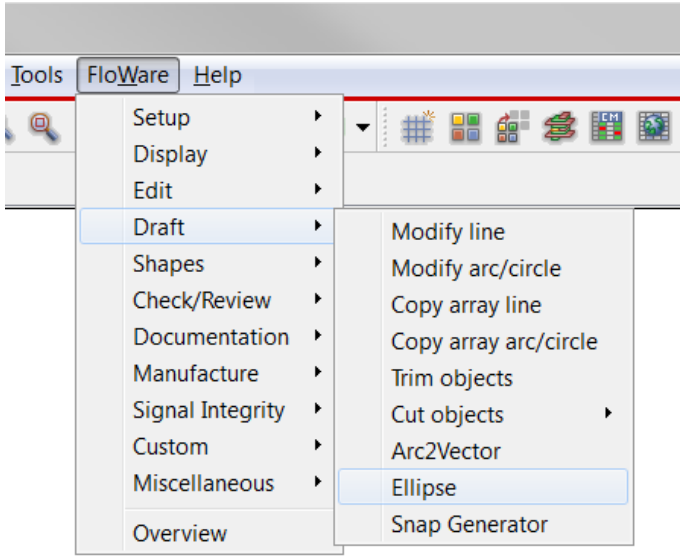
3D canvas



- In example above:
  - Solder mask region on Digital_Soldermask_1_TOP
  - Pad box on Digital_Soldermask_2_TOP
  - Pad box on Digital_Soldermask_3_TOP

Drafting Utilities

- Includes useful functions for drafting purposes
- Functions support dynamic preview before changes are committed
- Several functions
  - Modify line
  - Modify arc / circle
  - Copy array line
  - Copy array arc / circle
  - Trim objects
  - Cut objects
  - Arc2Vector
  - Ellipse



Drafting Utilities

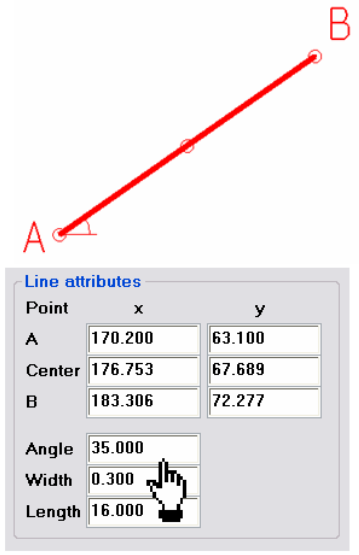
Modify line

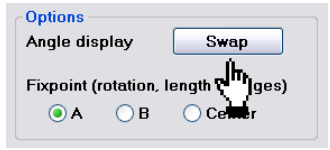
– Change line attributes on a parameter basis: Coordinates as well as angle, width and length

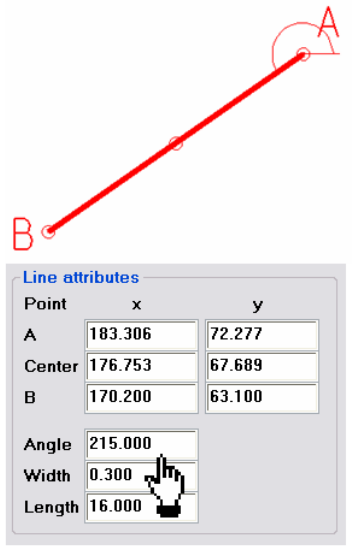
– Angle display can be swapped

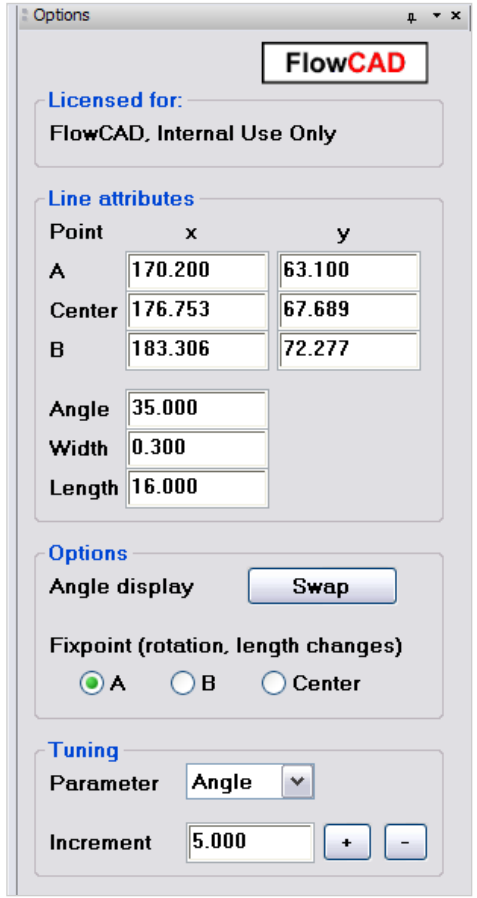
– Fix point for rotation and length changes can be chosen

– Fine-tuning capabilities for angle, width and length







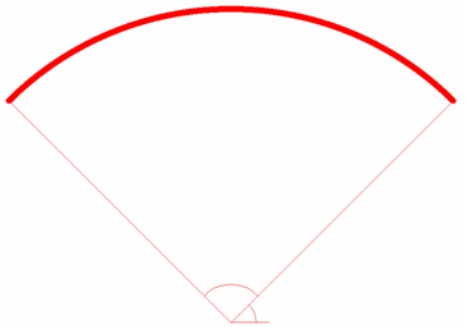


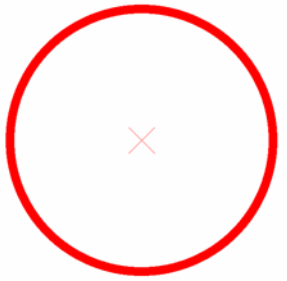
Drafting Utilities

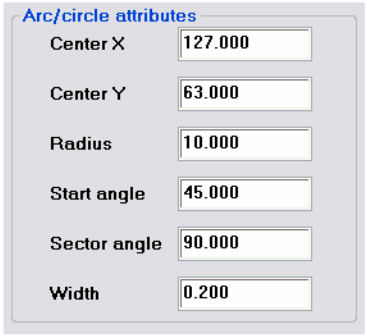
Modify arc / circle

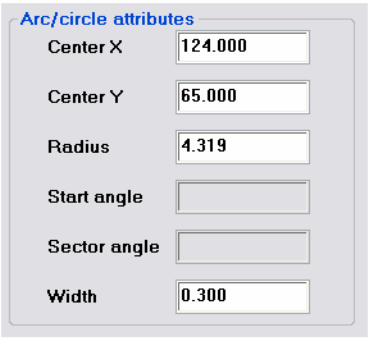
– Change arc or circle attributes on a parameter basis:
  Center coordinate as well as radius, start angle, sector angle and width

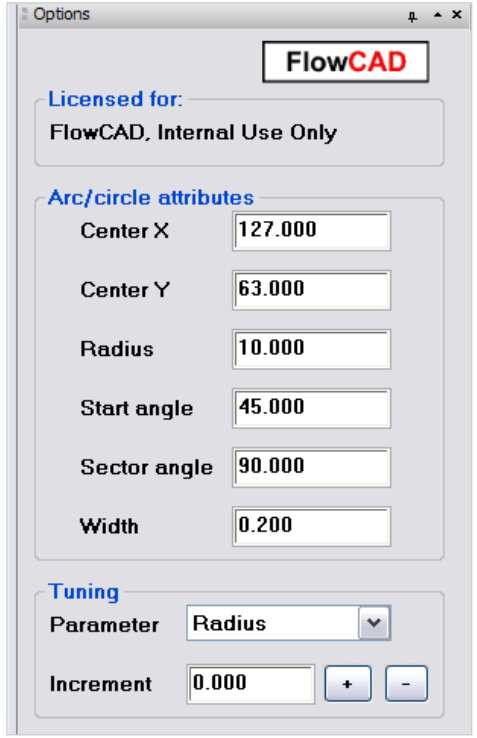
– Fine-tuning capabilities











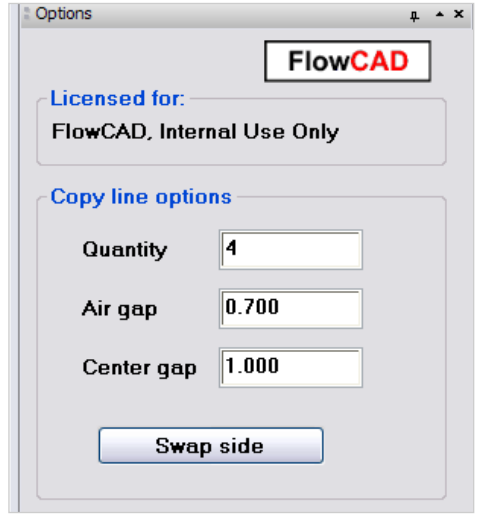
Drafting Utilities

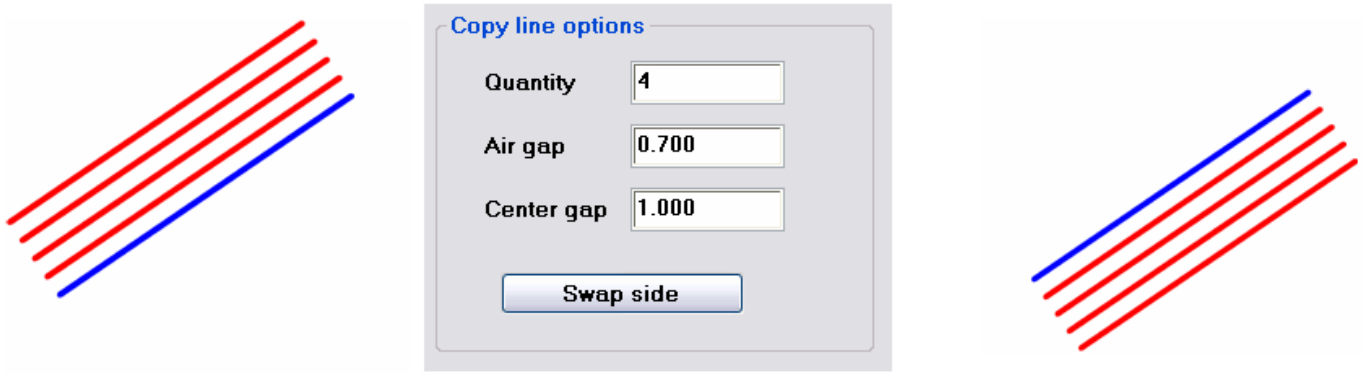
Copy array line

– Copies lines in parallel to a selected object

– Number of copies can be specified as well as air gap (or center gap respectively)

– Swap side

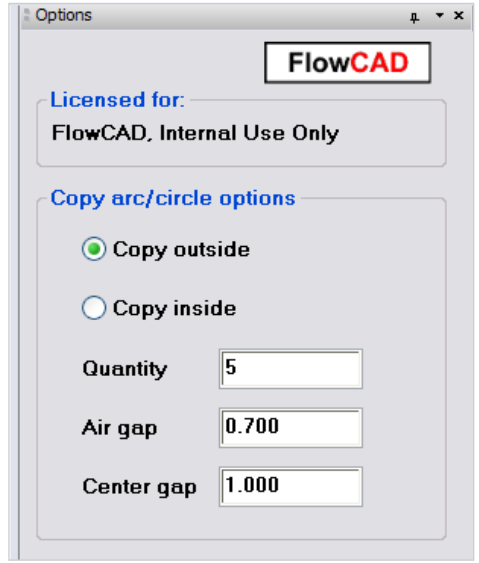


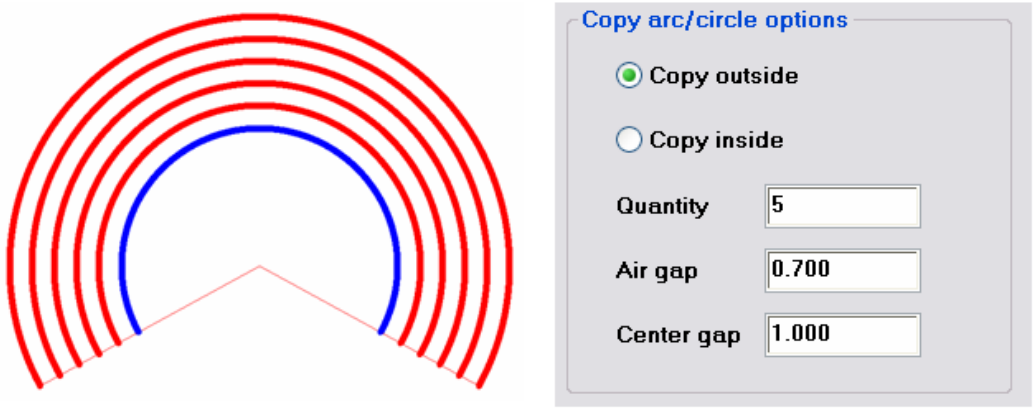


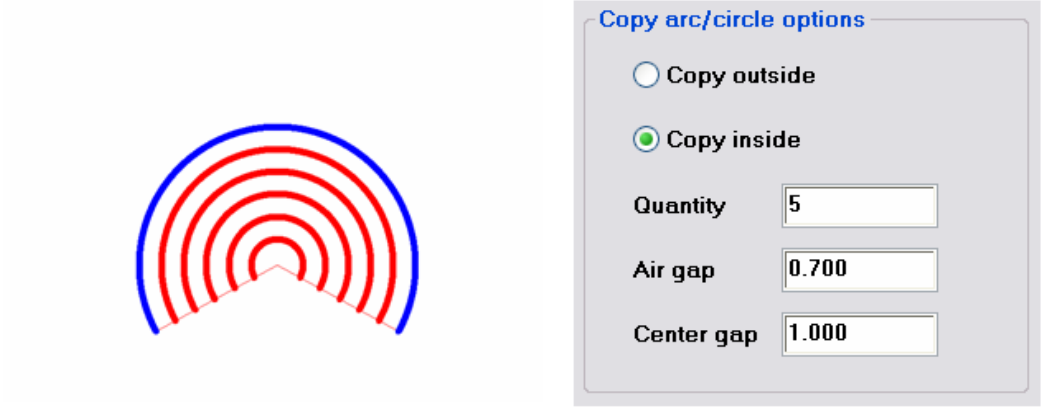
Drafting Utilities

Copy array arc / circle

- Copies arcs in a concentric way to a selected object
- Number of copies can be specified as well as air gap (or center gap respectively)
- Direction can be chosen



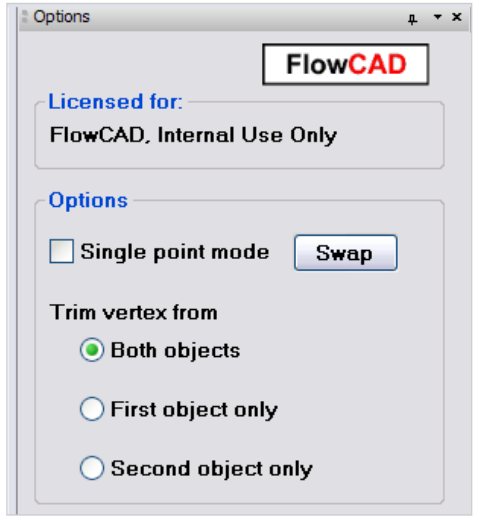


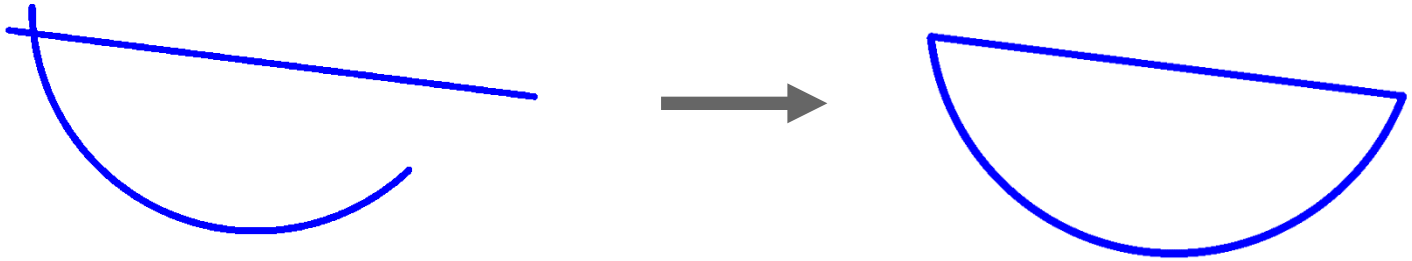


Drafting Utilities

Trim objects

- Trims object endpoints to calculated intersections
- Works with arcs and line objects
- Single point mode when two intersections are found (in case of arcs), ability to swap
- Trim vertex for both objects, first only or second only

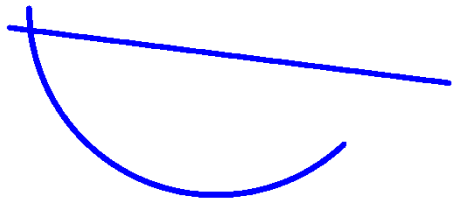




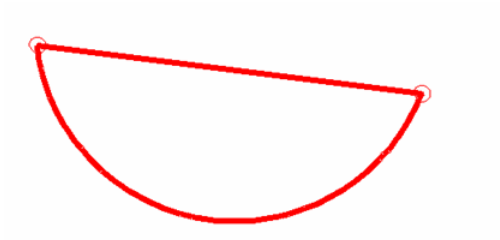
Drafting Utilities

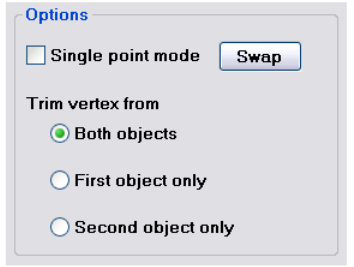
Trim objects: Single point mode

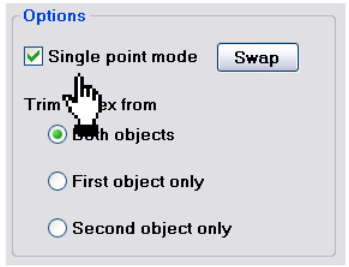
Original objects

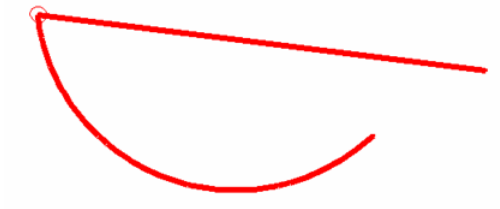


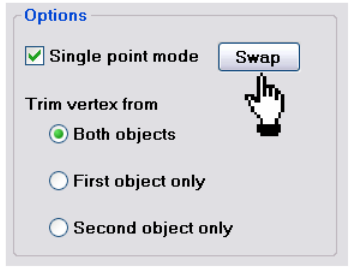
Result





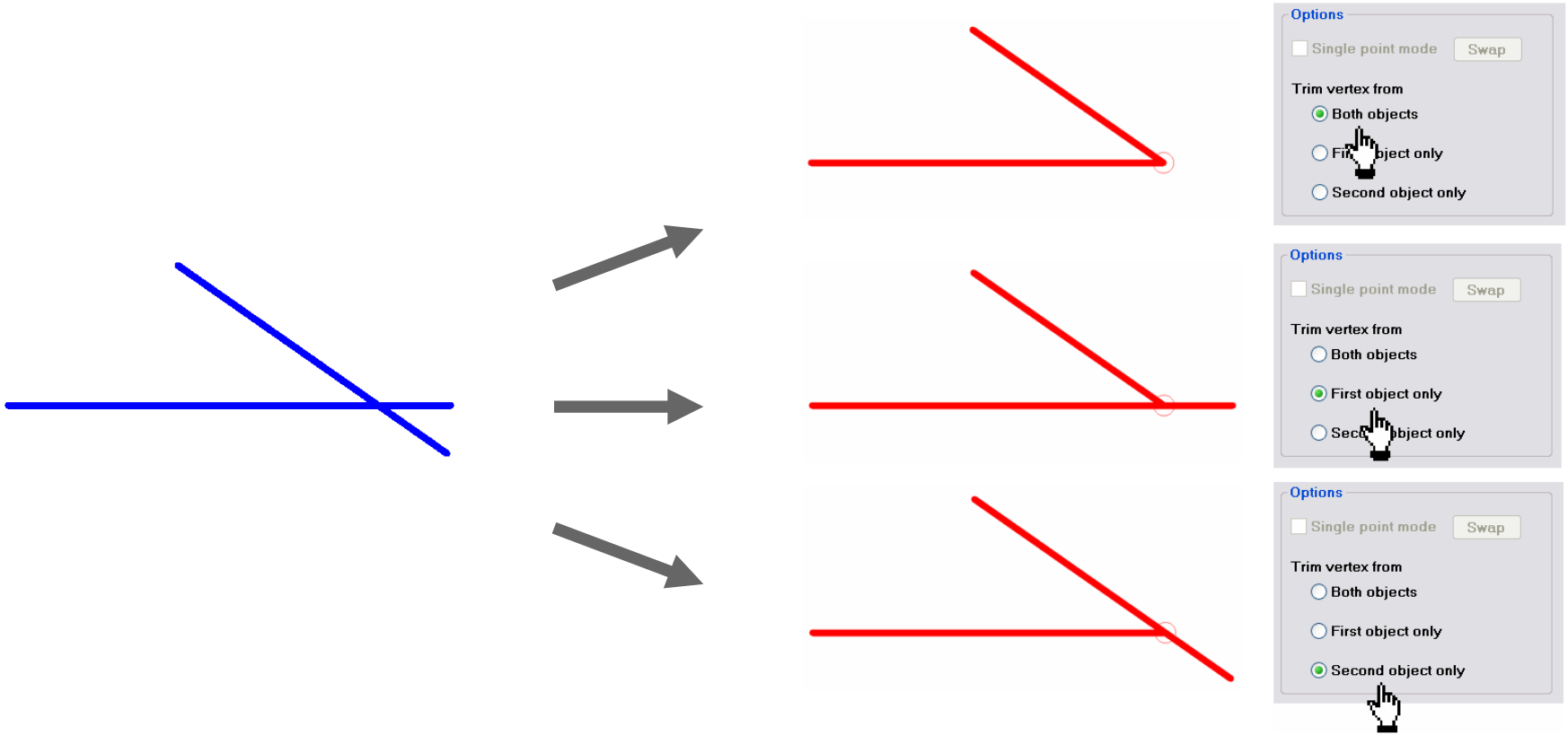






Drafting Utilities

Trim objects: Trim vertex from …



Drafting Utilities

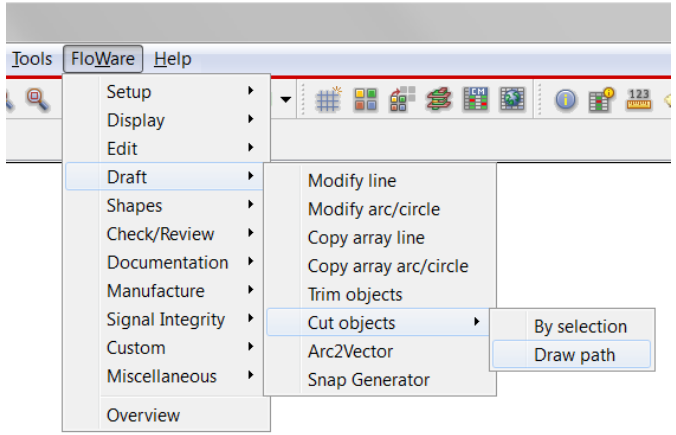
Cut objects

– Enables users to cut line, arc or circle objects for various purposes

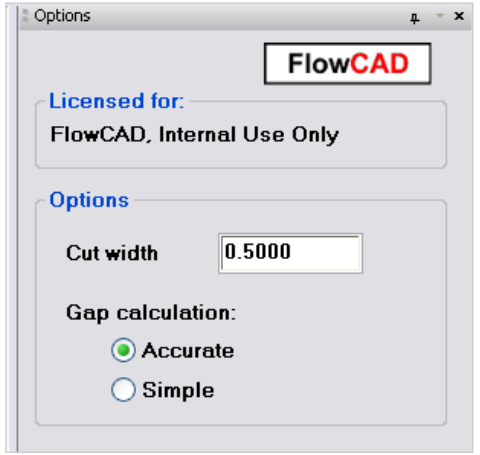
– Two commands

- Cut objects > By selection
- Cut objects > Draw path

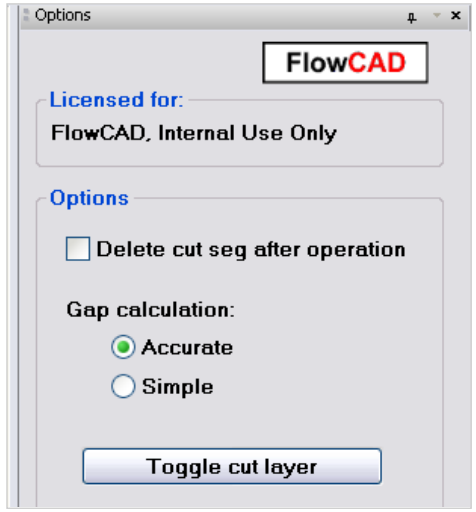
– Useful when layout portions need to be isolated before moving them to a new location



Cut objects > Draw path

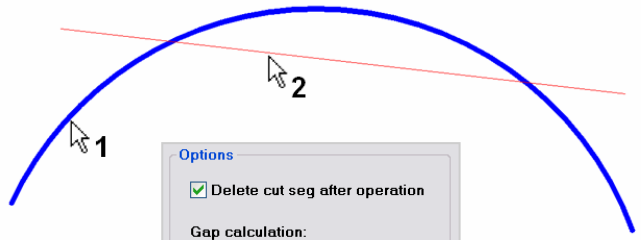


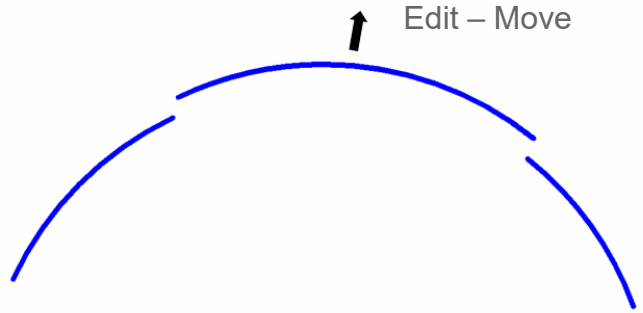
Cut objects > By selection



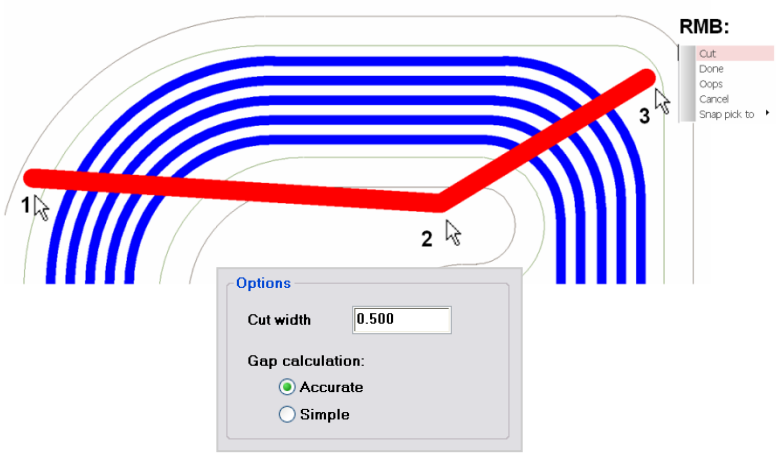
Drafting Utilities

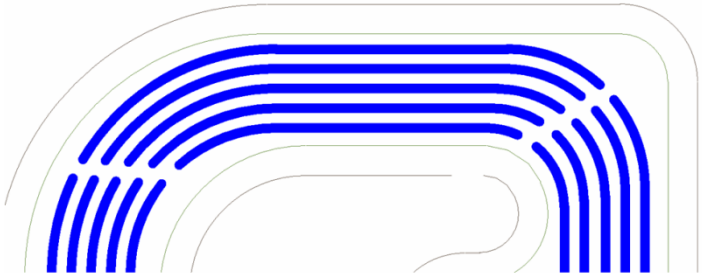
Cut objects – By selection





Cut objects – Draw path



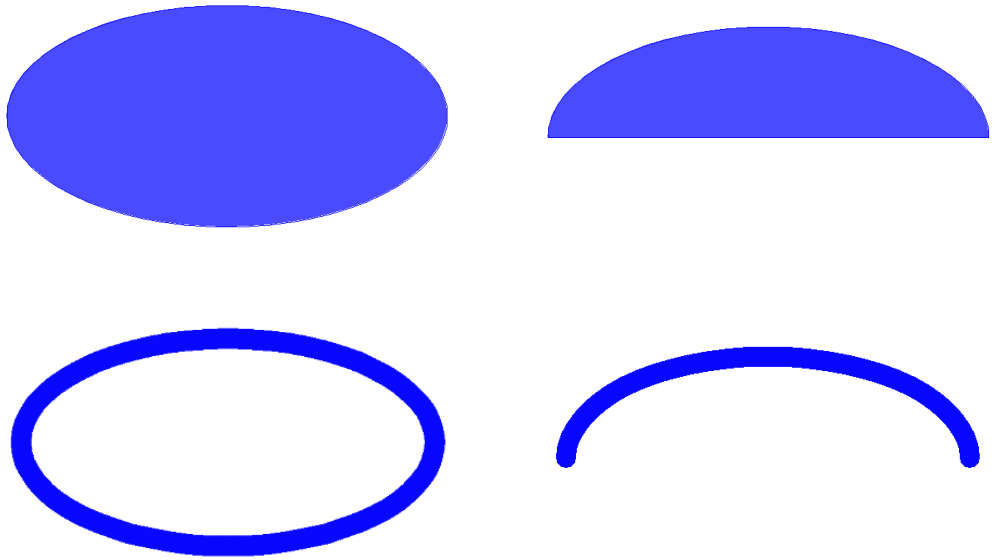


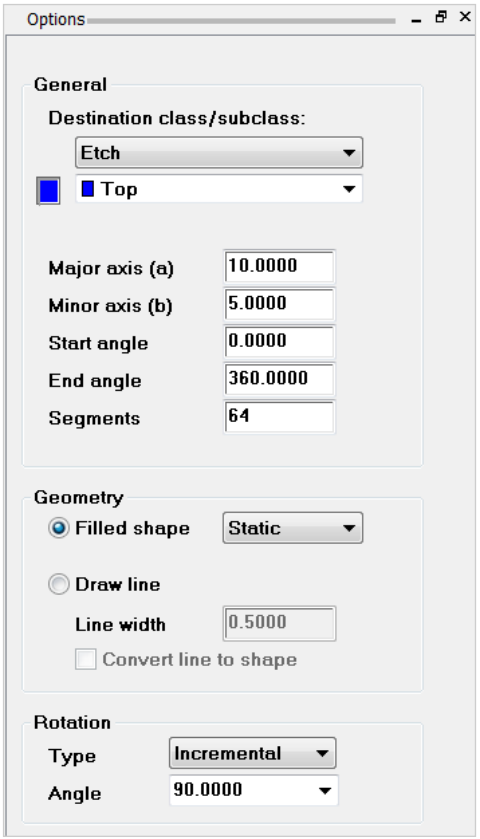
Minimum cut width limited by database resolution

Drafting Utilities

Ellipse

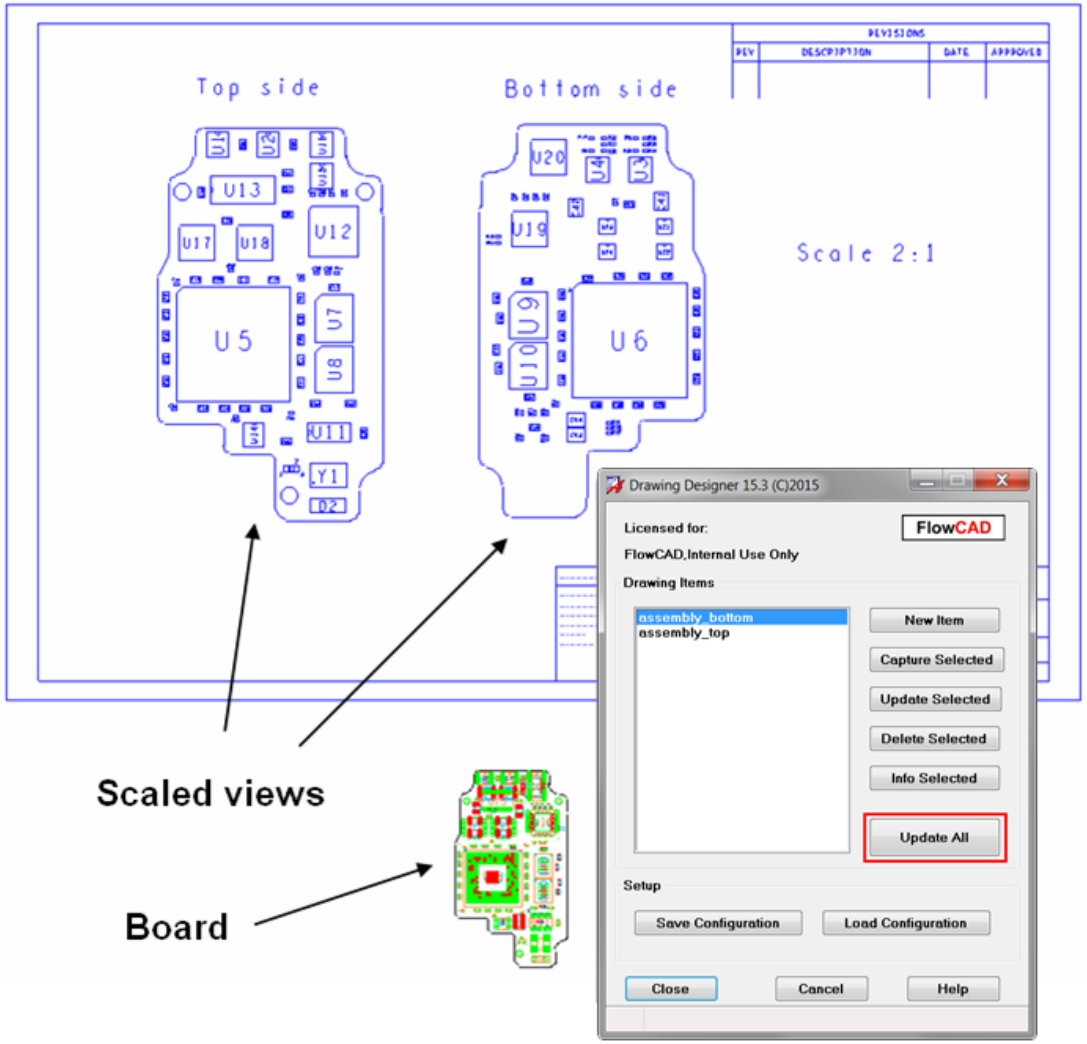
– Useful for pad shapes and RF applications
– Axis parameter **a** and **b**
– Geometry
  • Full
  • Partial (specify start, end angle)
– Type
  • Solid filled shape
  • Draw line path
– Number of segments



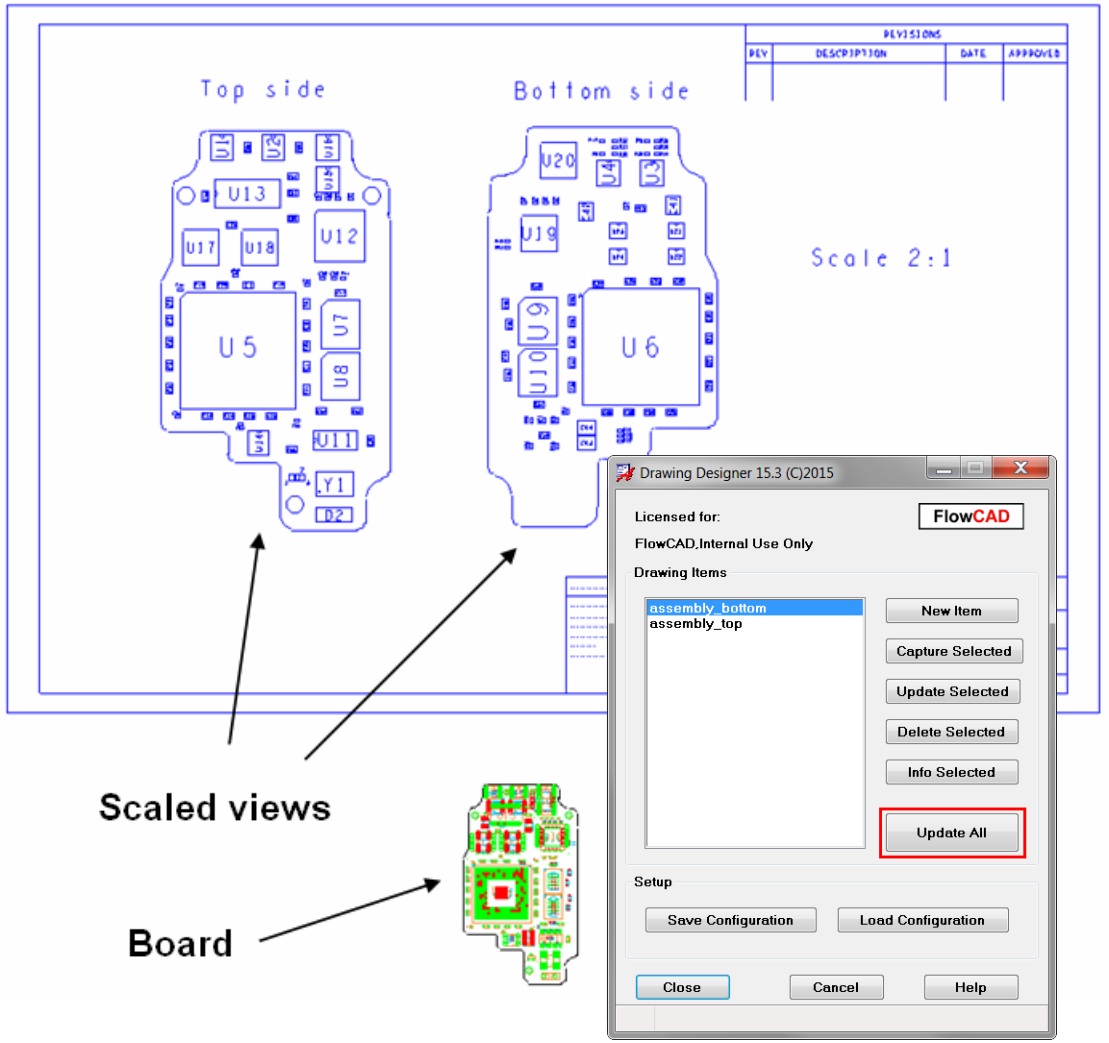


Drawing Designer

- Useful when creating manufacturing drawings
- Records the creation of scaled views (including mirroring and rotation)
- Automatic updates
- Configuration stored in database
- Configuration export and import

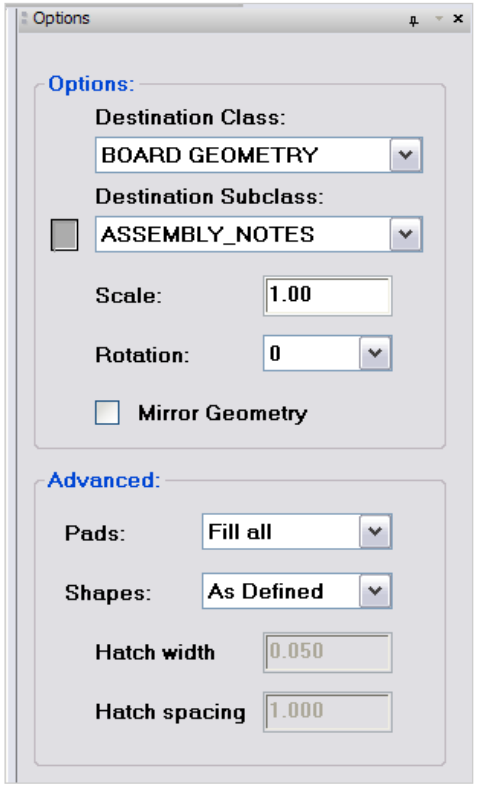


Drawing Designer

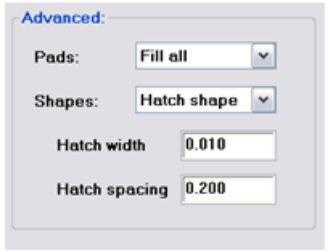


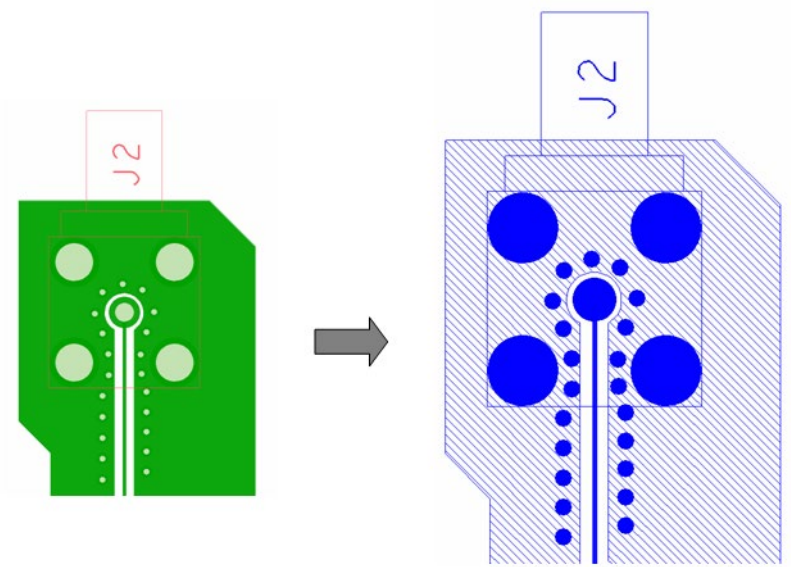
Drawing Designer

- Ministatus panel offers various options when creating new drawing items
  - Destination layer where data is written to
  - Scale, rotation, mirror of the item
  - Pad style: filled, unfilled
  - Shape: As defined, unfill all, hatched



Example

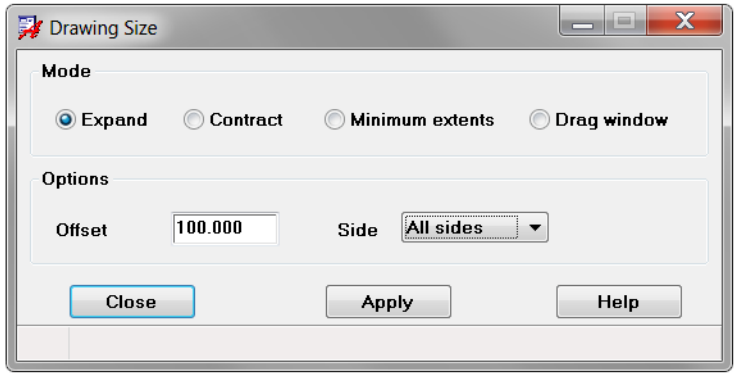


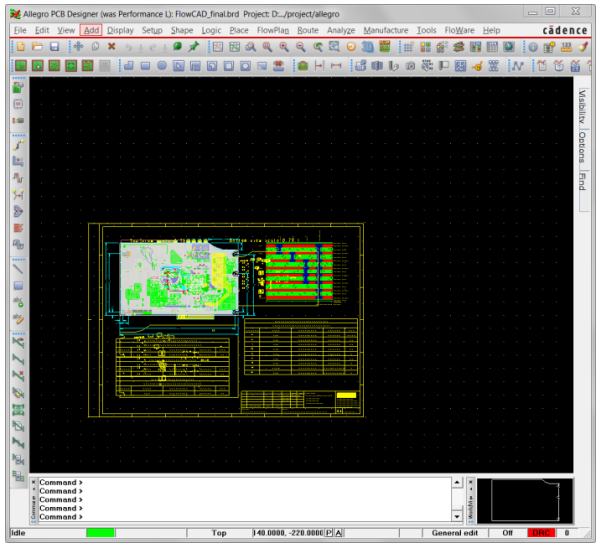


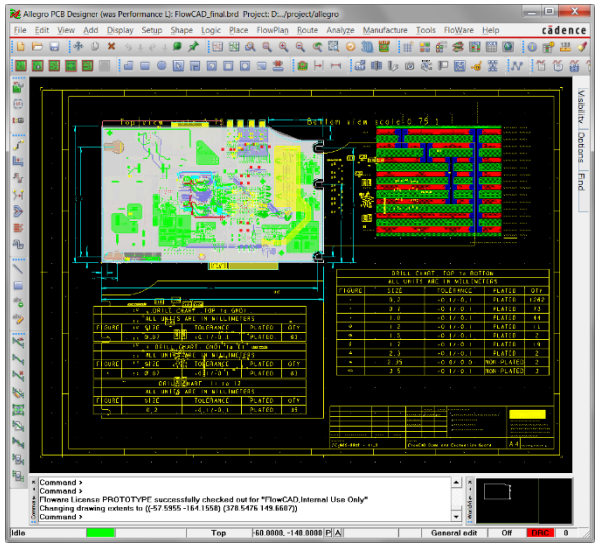
Note: Hatch option only applies to solid filled shapes

Drawing Size

- Let‘s you change the design extents in a quick and easy way
- Useful if you want to reduce design extents to minimum values
- Settings can be applied to all or individual sides

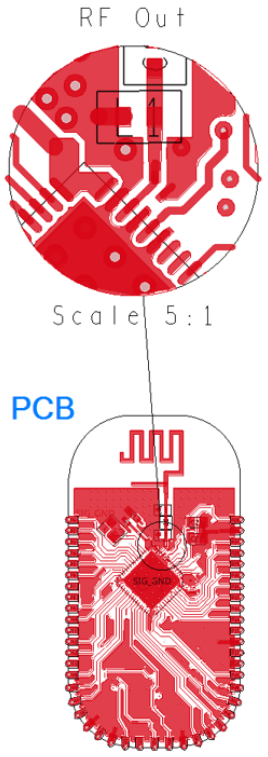


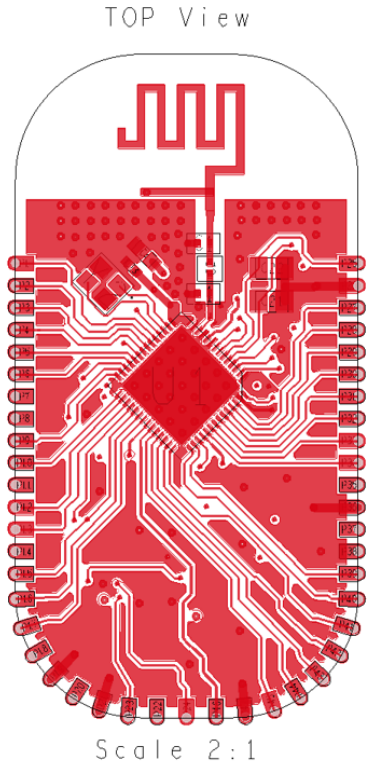


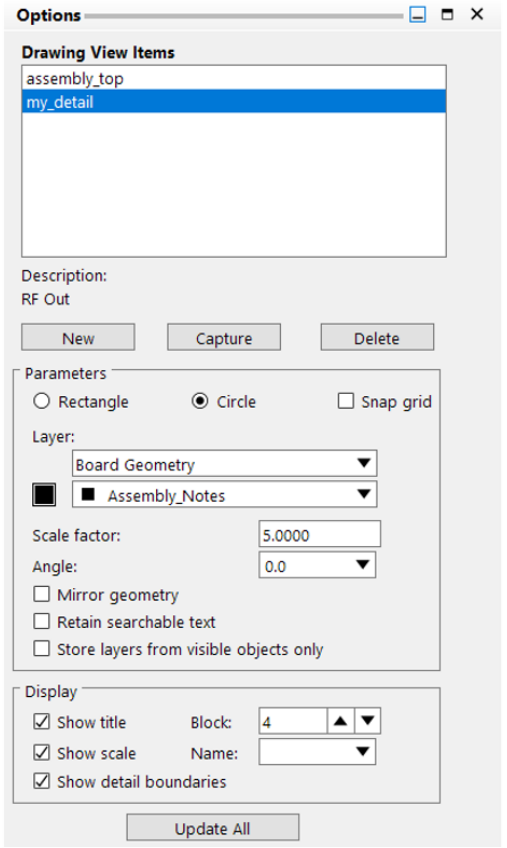


Drawing View Manager

- Facilitates creation of manufacturing drawings
- Features
  - Capture named drawing view items interactively
  - Clipping capabilities using rectangular or circular boundaries
  - Scale, mirror, rotate
  - Retain object colors
  - Automatic update
  - Template support

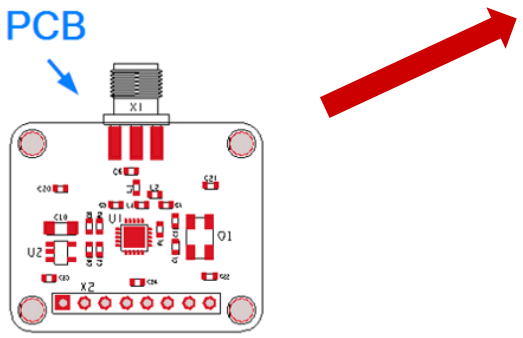


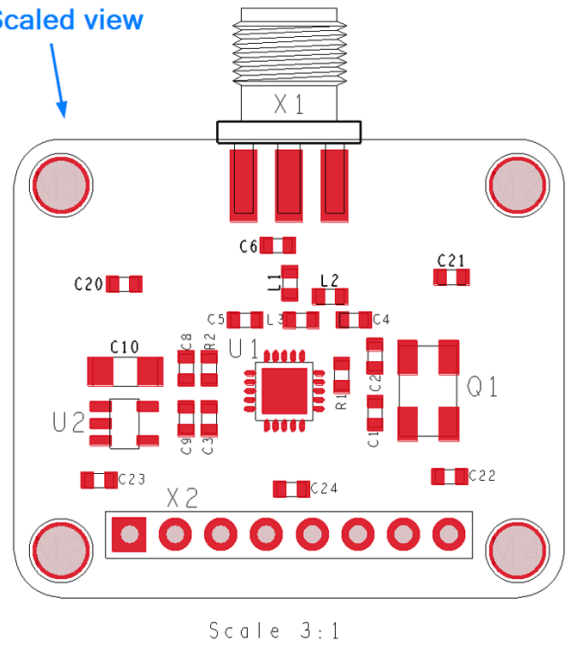


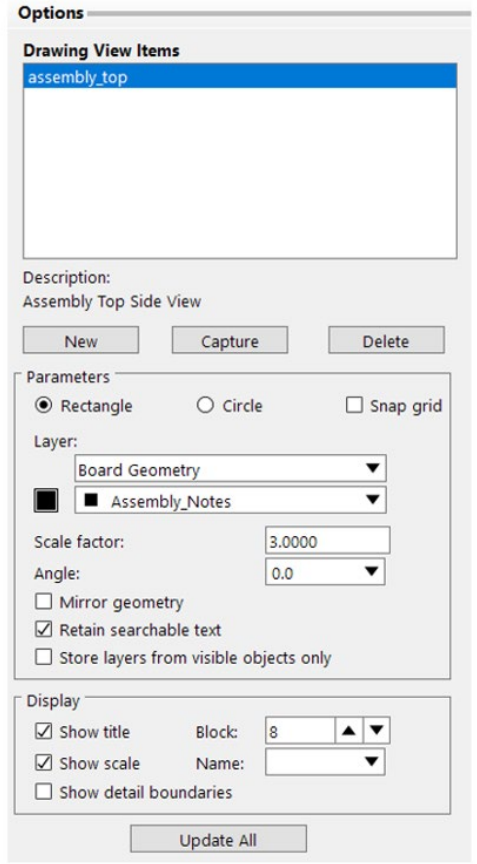


Drawing View Manager

- Simple use model
  - Press **New** and enter a name
  - Select item from the list
  - Press **Capture**
  - Adjust layer visibility and find filter …
  - Adjust mirror, scale, rotation …
  - Place item
  - Use **Update All** once PCB was modified

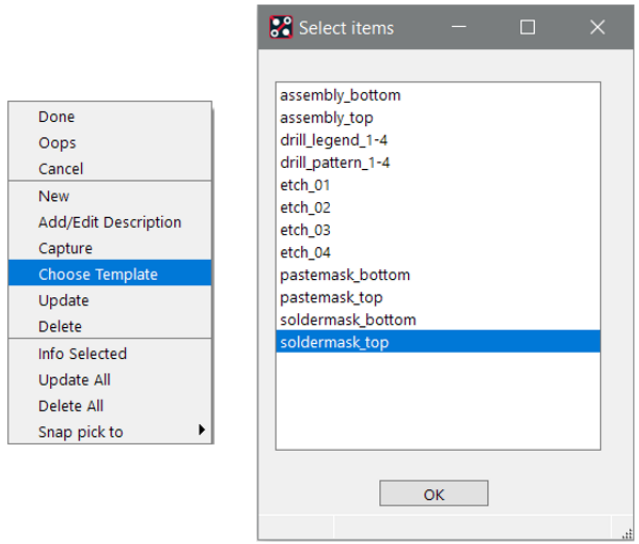


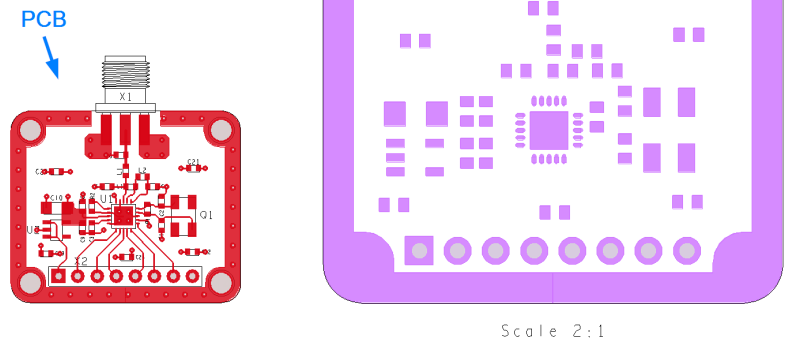




Drawing View Manager

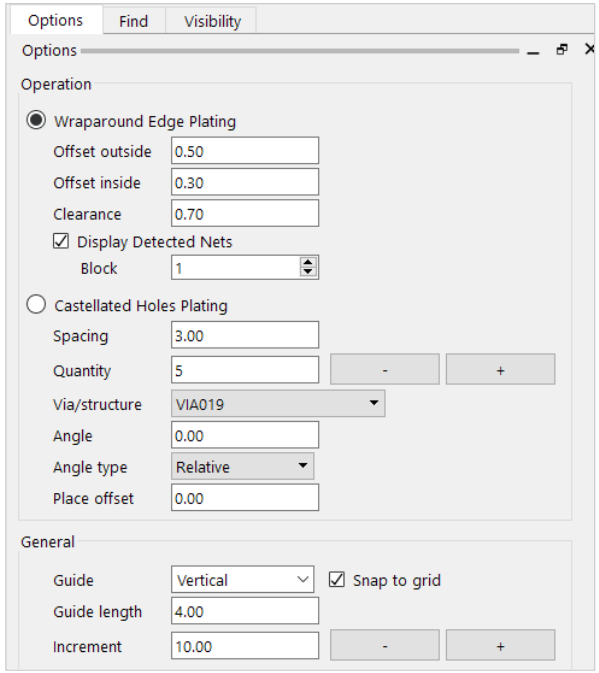
- Template support
  - Significantly shortens setup time
  - Eliminates the need to create drawing view items each time from scratch in a new project
  - Information about visible layers, objects, source area, destination layer, scaling etc. is already pre-defined
  - Default templates located in share/pcb/toolbox/config/drawingview
  - SITE and pcbenv customizable
- Use model
  - **RMB – Choose Template** and select an item
  - If necessary adjust scale etc.
  - Place item

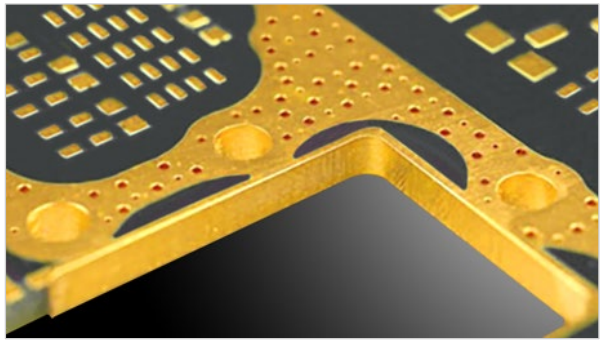


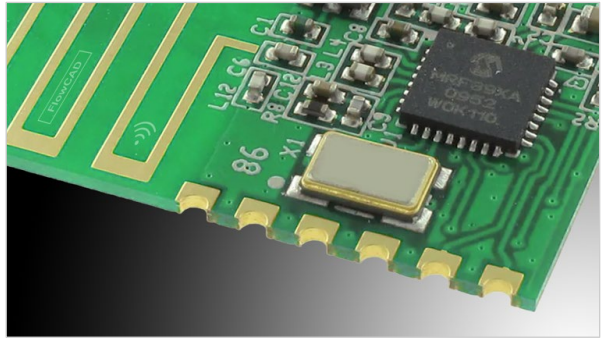


Edge Plating

- Edge plating is a plated conductive material on the edge of a PCB where in normal instances, only dielectric material is exposed
- This plated conductive material may be used for many functions
  - Improve current carrying across multiple layer of a PCB
  - Edge connection protection
  - Board to case grounding
  - EMC signal integrity
  - Heat management
- Two forms of Edge Plating
  - Wraparound (Side) Plating
  - Castellated Holes

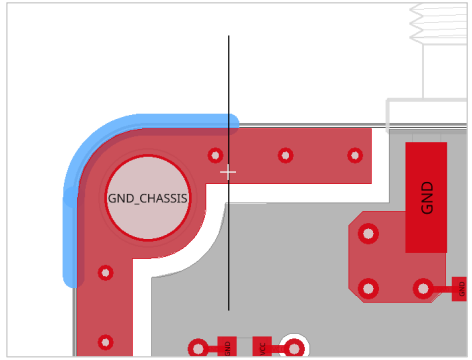


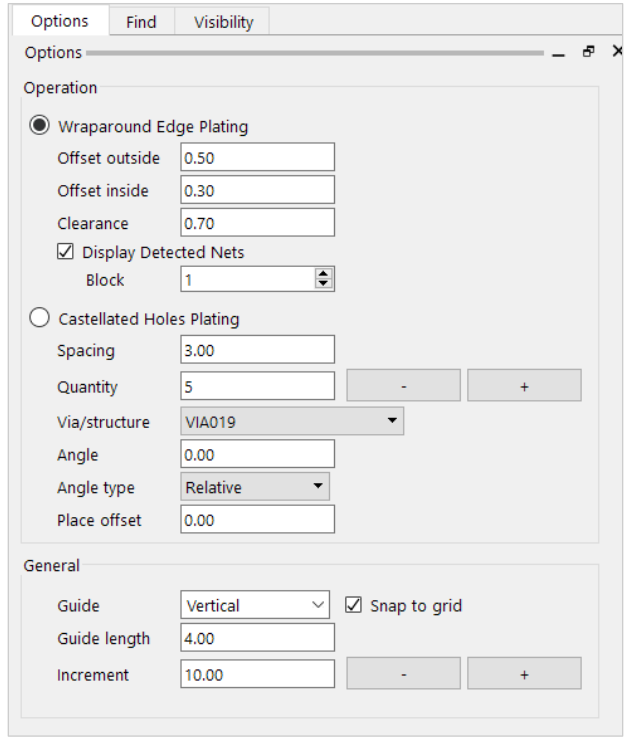


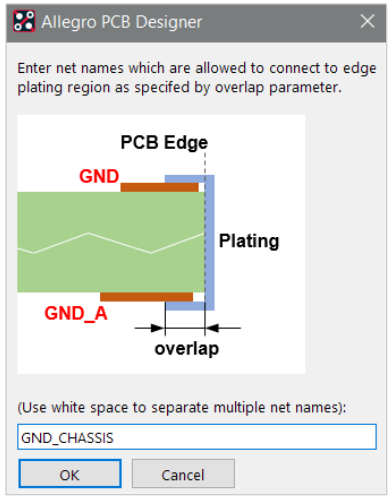


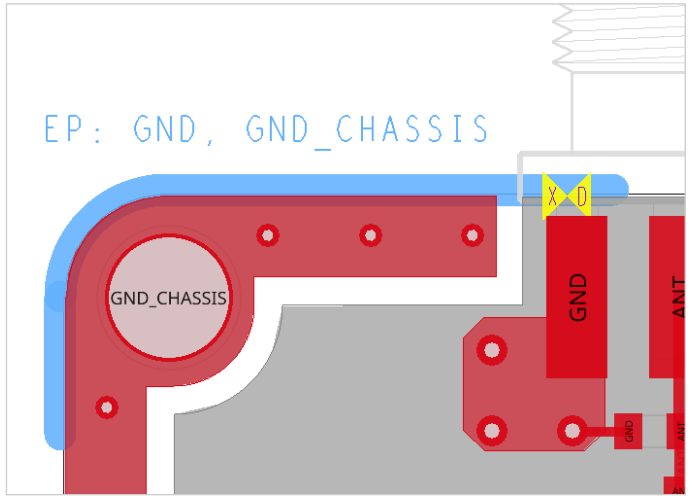
Edge Plating: Wraparound (Side)

- Define plating sections interactively
- Net assignment
- Connectivity Check
- DRC Clearance Check
- Net Short support



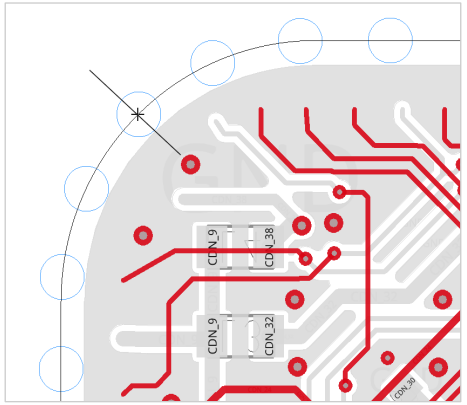


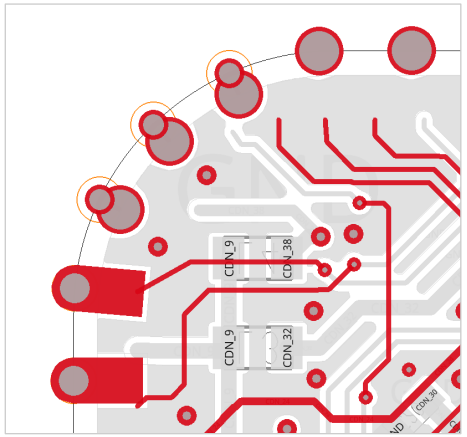


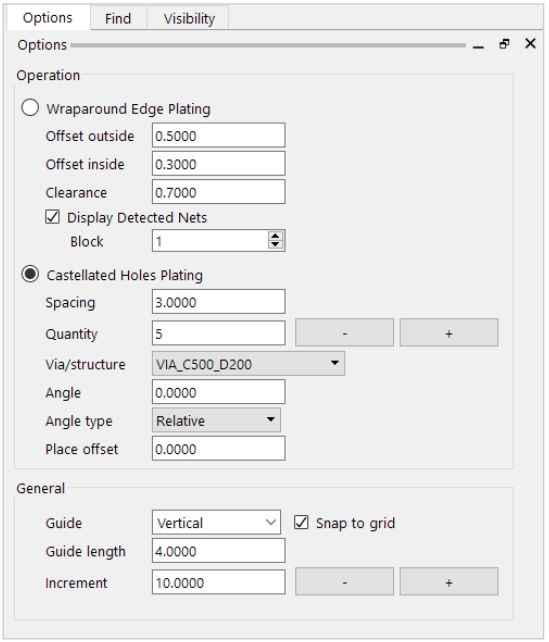


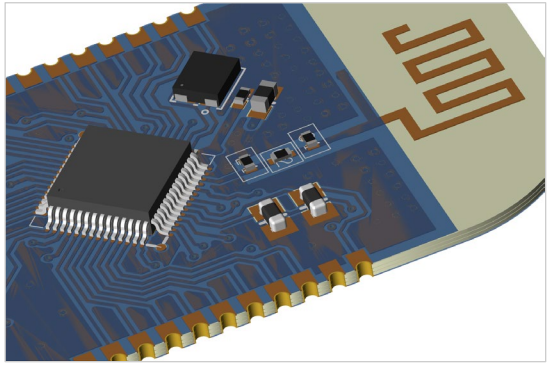
Edge Plating: Castellated Holes

- Define locations interactively along outline supporting
  - Spacing
  - Quantity
- Objects supported
  - Vias
  - Via structures
  - Symbols
  - Electrical components
- Placement parameters
  - Alignment with outline (relative, absolute)
  - Offset from outline



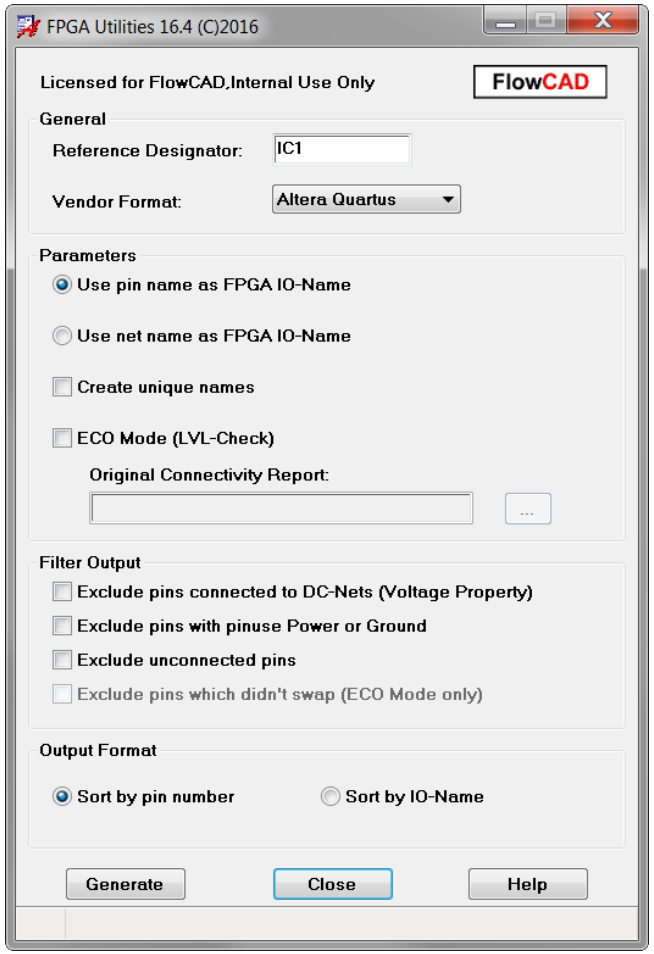






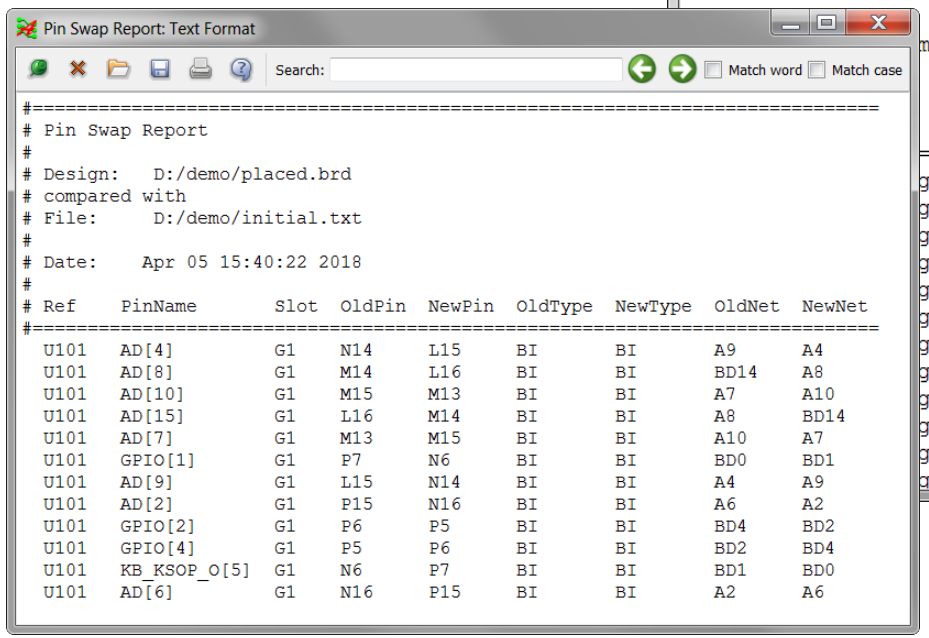
FPGA Utilities

- Check and report any pin swapping which has been done in a PCB layout
- Export pin constraints to csv and vendor specific formats
  - Altera, Xilinx, Actel, Lattice
- Works in both flows
  - Allegro Design Entry HDL
  - OrCAD Capture
- Various options

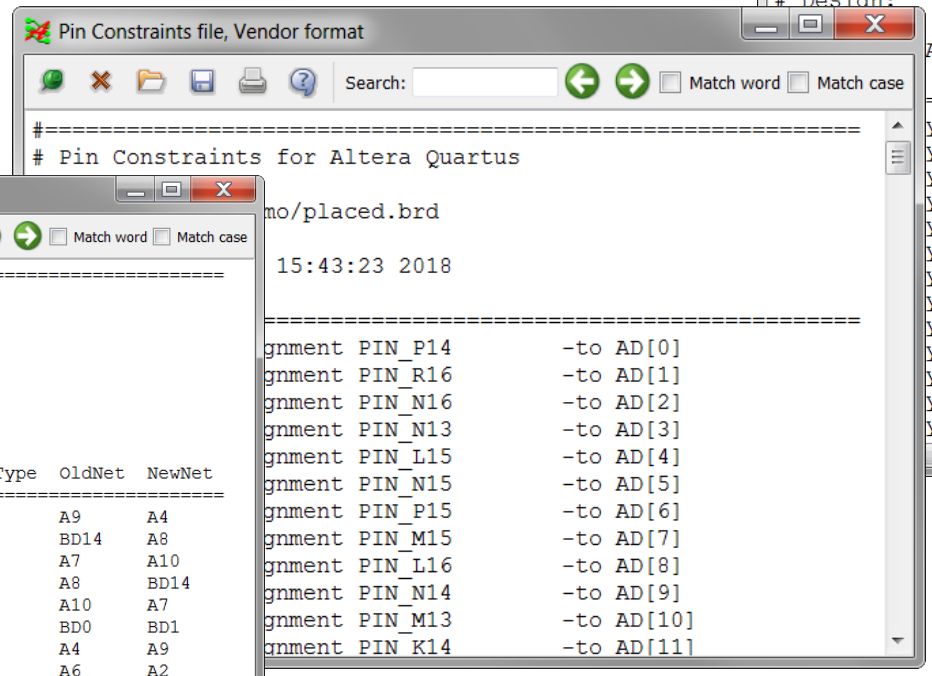


FPGA Utilities

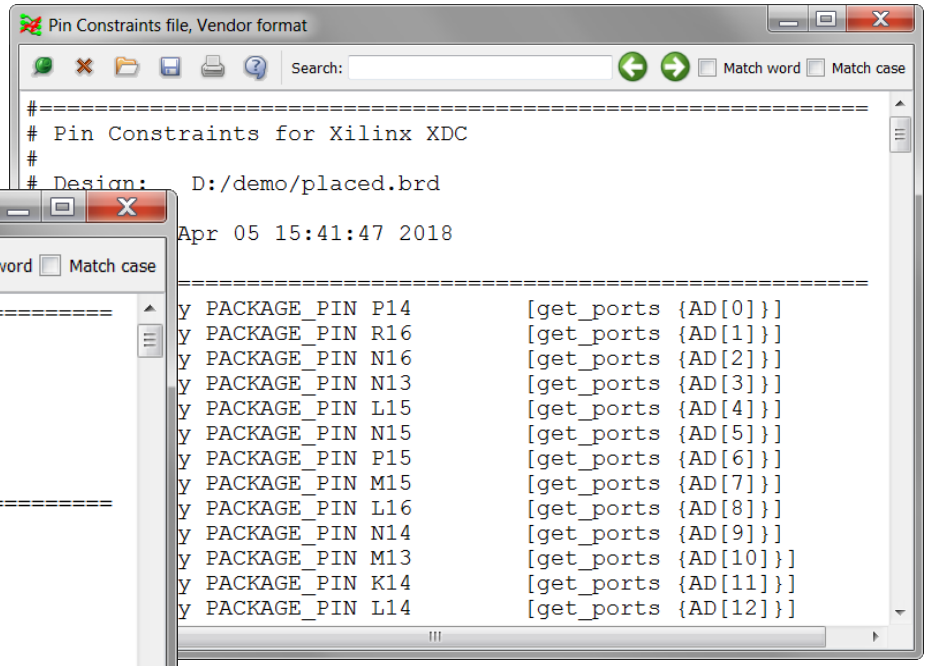
Differences Report



Altera Quartus

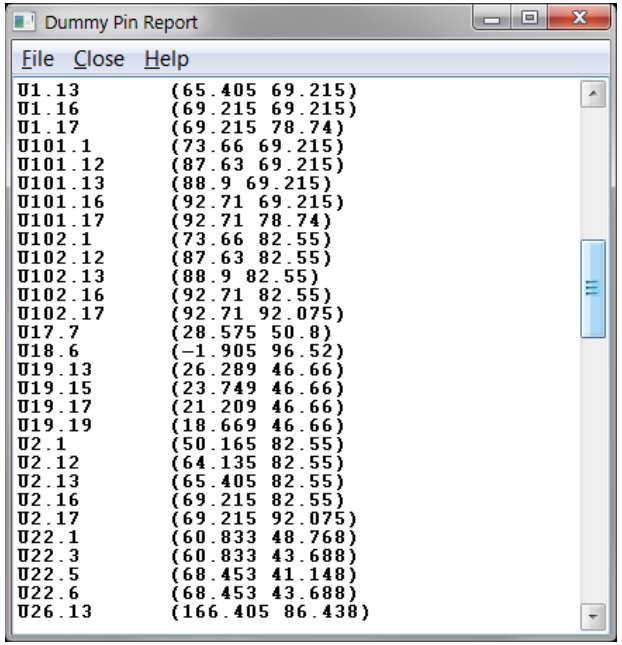


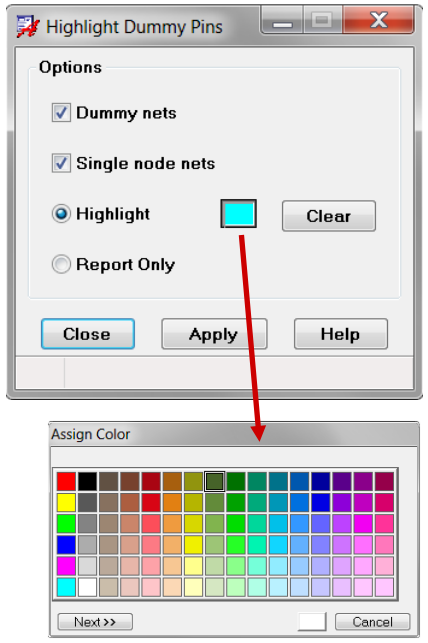
Xilinx XDC

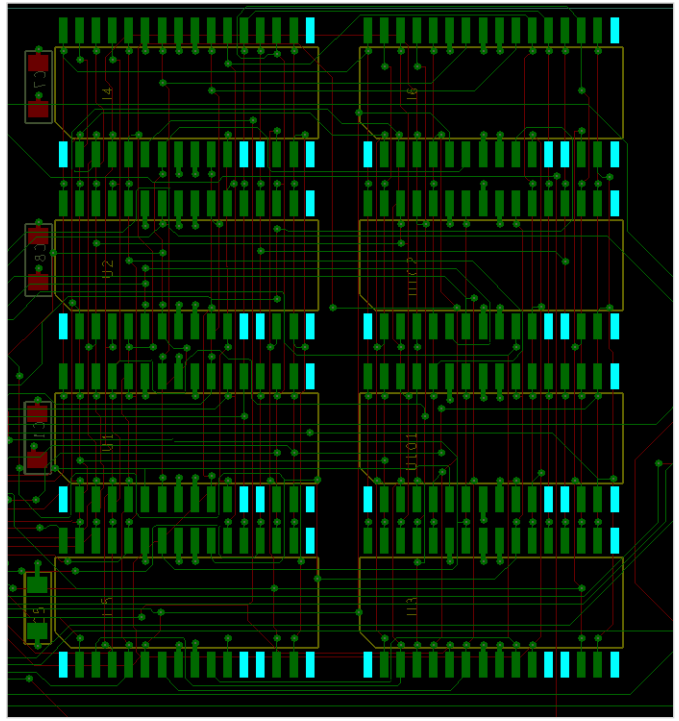


Highlight Dummy Pins

- Assigns a color to all pins in a design which are not connected to any net
- Including report and cross probe functionality
- Useful for review purposes

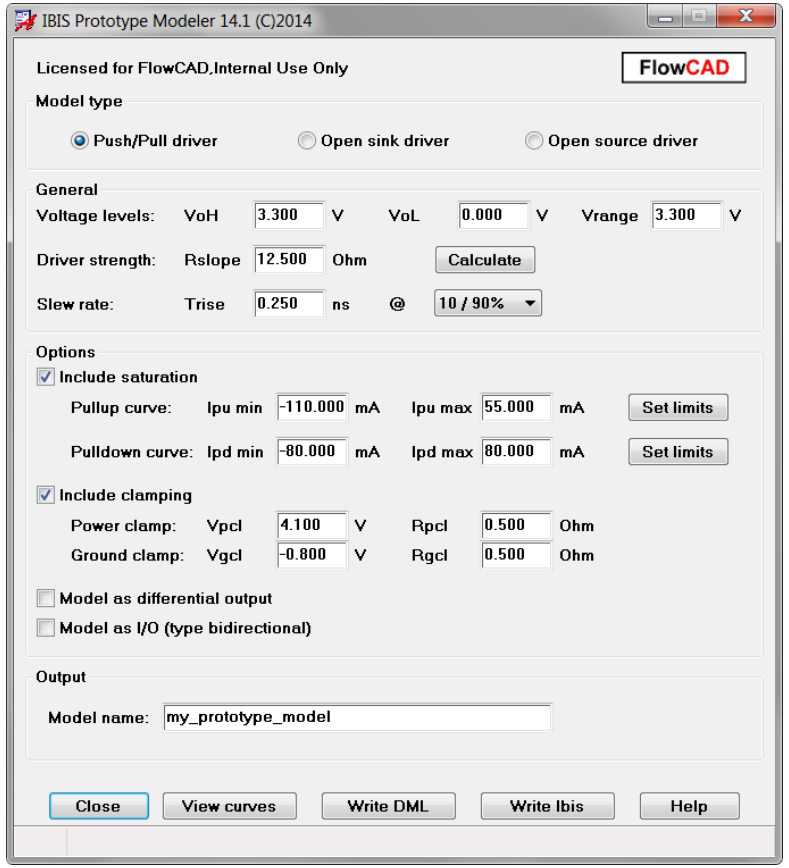




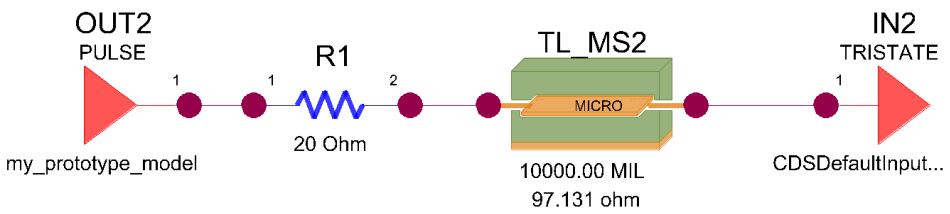


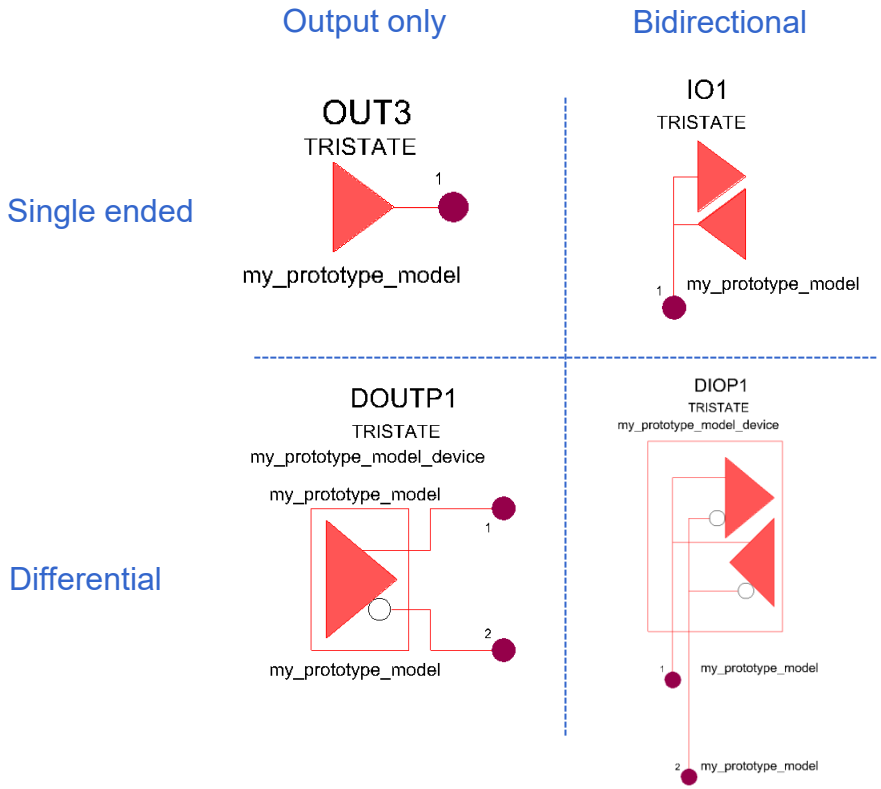
IBIS Prototype Modeler

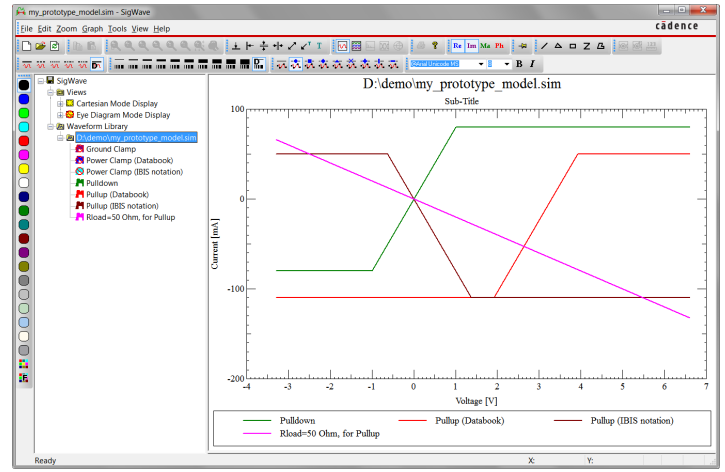
- Creates scalable IBIS models for early stage signal integrity analysis
- Features include
  - Ability to create Push / Pull, Open-Sink and Open-Source buffers
  - Adjustable voltage levels
  - Adjustable internal resistance including a calculator
  - Adjustable slew rate dV / dt
  - Ability to include saturation and clamping effects
  - Support for single-ended as well as differential outputs
  - Support for output only and bidirectional models
  - Ability to view curves in Sigwave
  - Generate DML models as well as native IBIS models



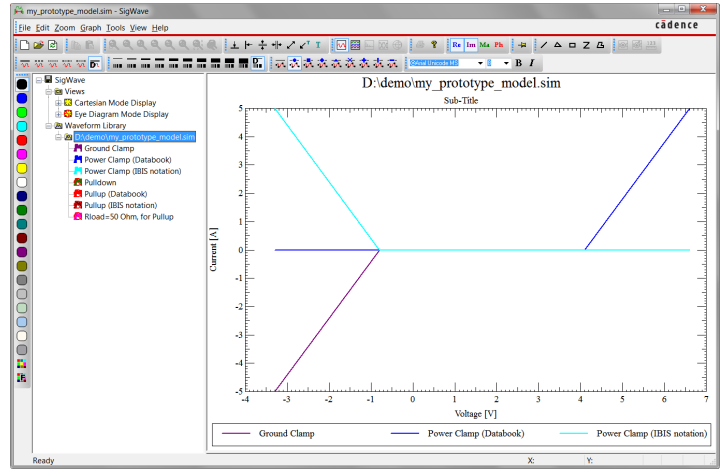
IBIS Prototype Modeler







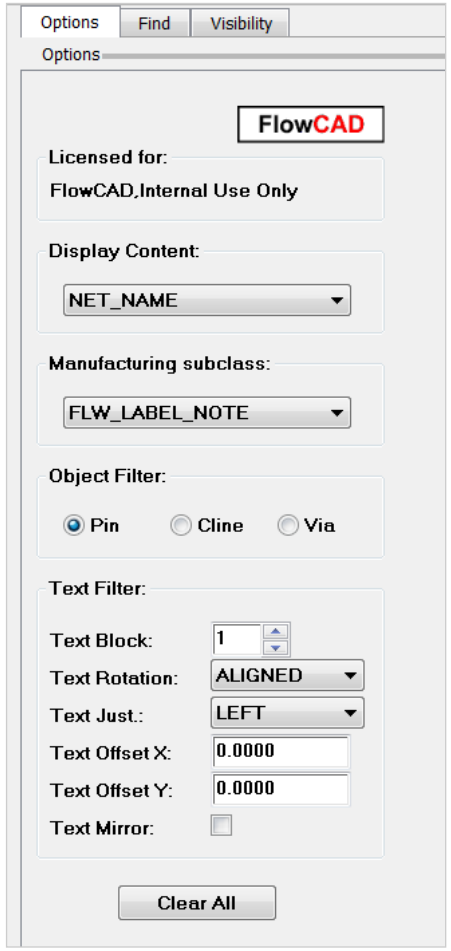
Pullup, Pulldown and Rload curves



Power, Ground clamp

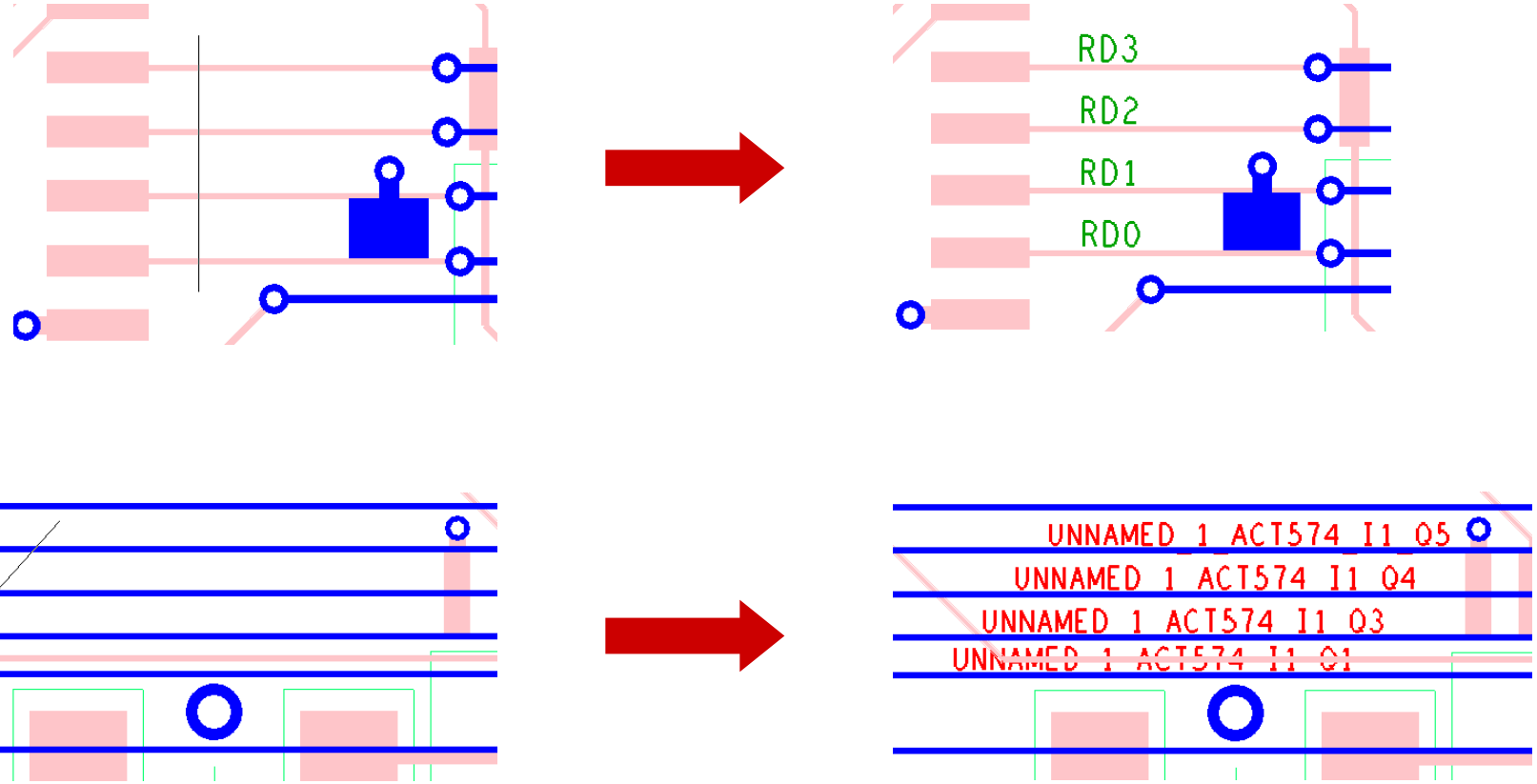
Label Generator

- Creates signal name and pin labels for documentation purposes
- Selectable label content (e.g. signal same + pin number)
- Individual label origin (e.g. pin, or via origin, but also cursor intersecting cline)
- Aligned text rotation mode (text angle value follow cursor gesture)
- Supports three different object types (pin, via, cline)
- User defined text size, justification and rotation



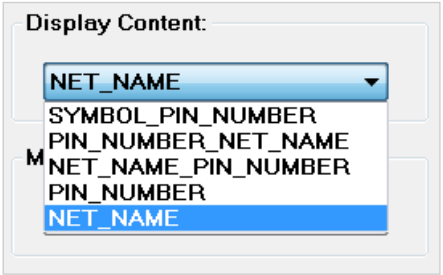
Label Generator

Procedure



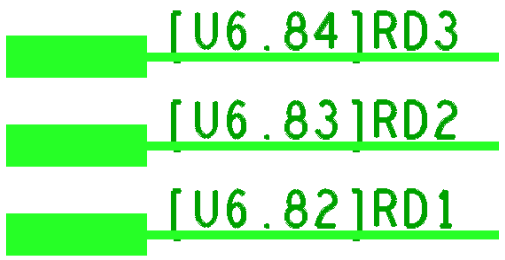
Label Generator

Label Content

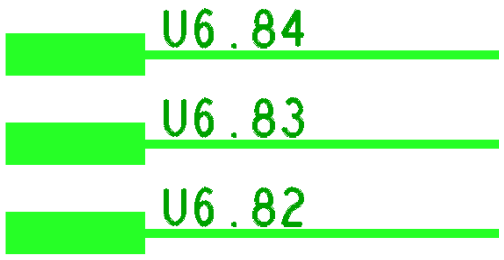


NET_NAME

PIN_NUMBER_NET_NAME

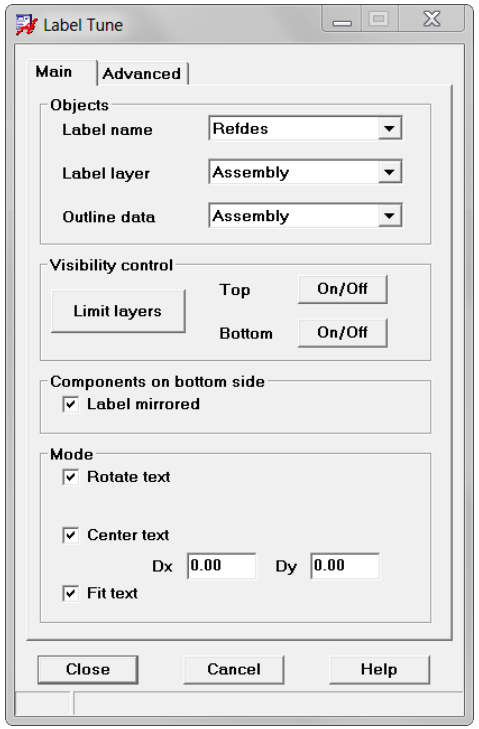


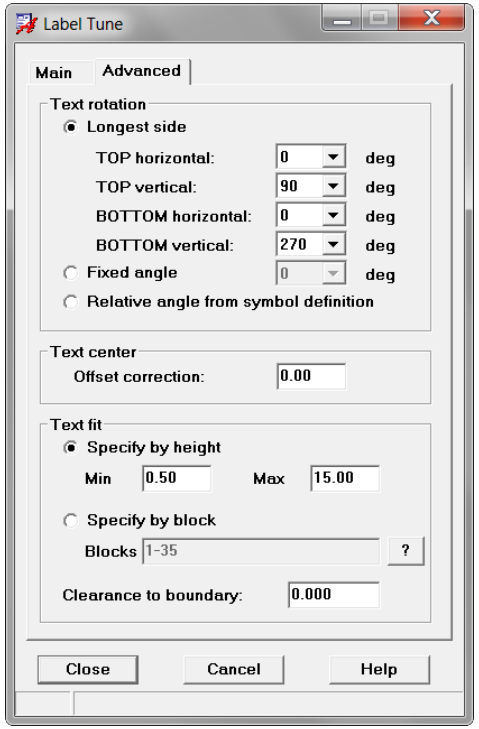
PIN_NUMBER



Label Tune

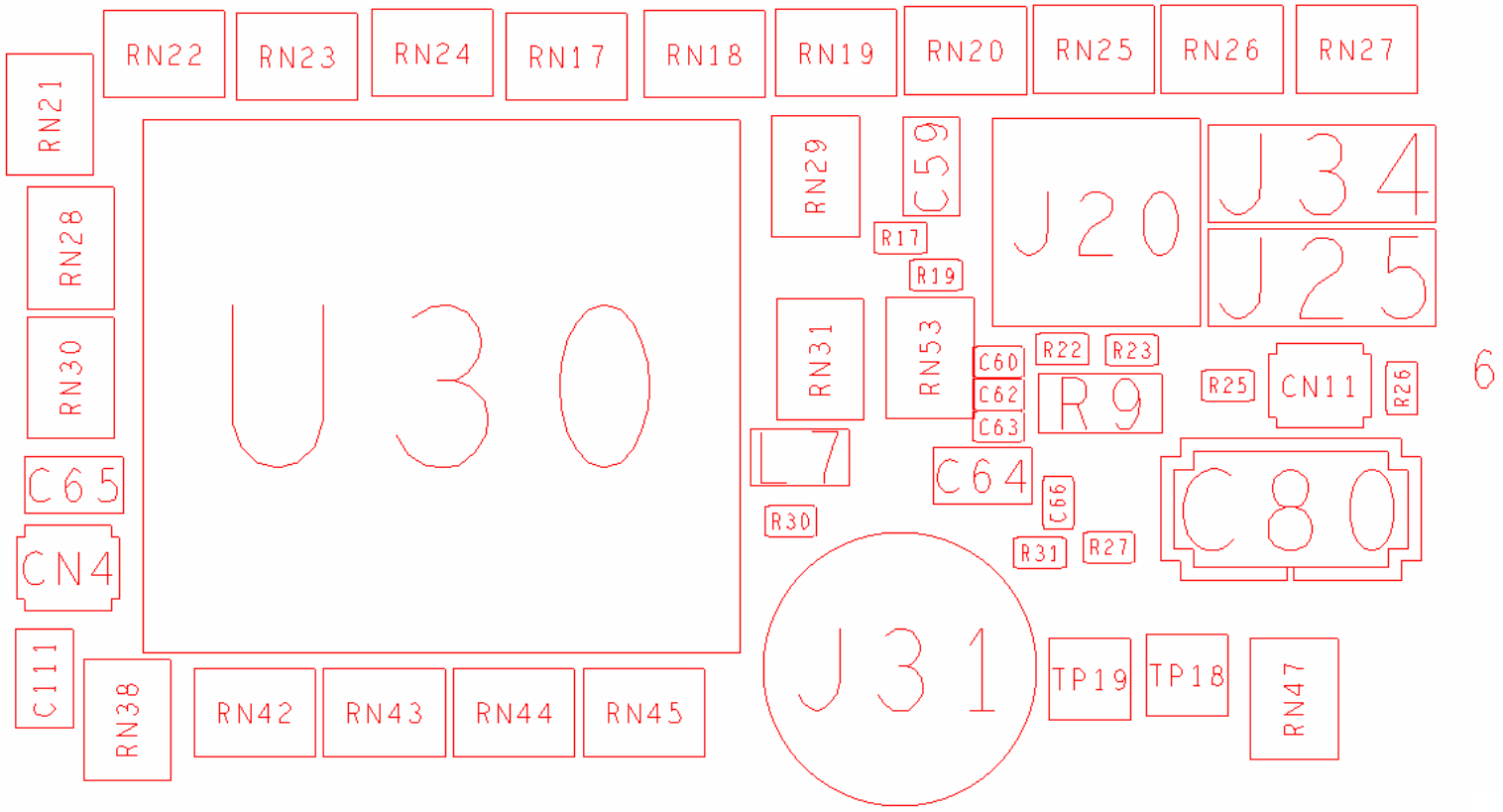
- **Adjusting component labels automatically**
  - Better readability
  - Saves a lot of time when creating assembly drawings
- **Features**
  - Label can be chosen (e.g. Refdes, Value, Part Number, …)
  - Automatic rotate, center, fit
  - Automatic mirroring
  - Visibility control
  - Various options
    - Max block size, max height
    - Boundary clearance





Label Tune

Typical situation in PCB Editor

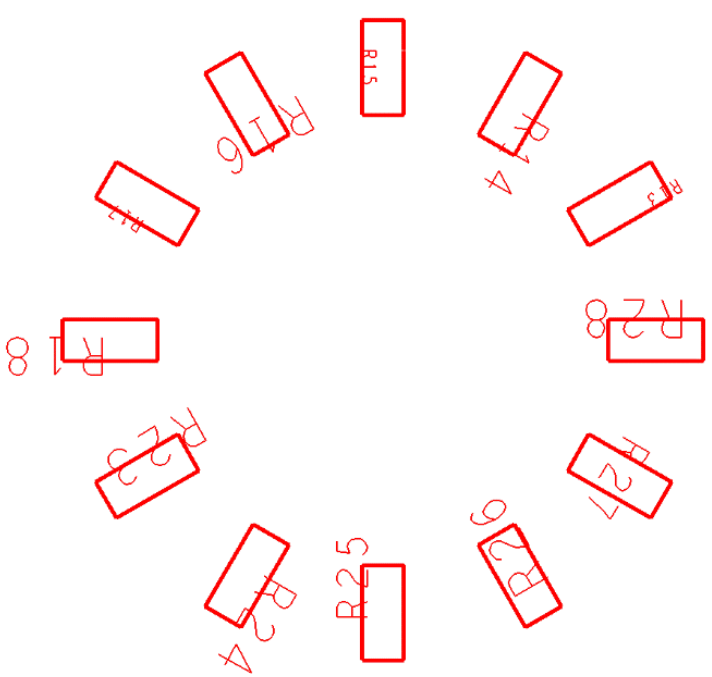


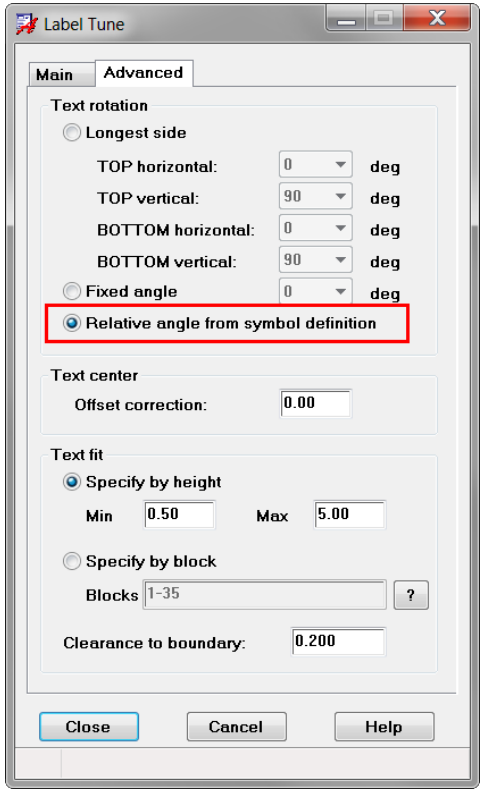
Animation

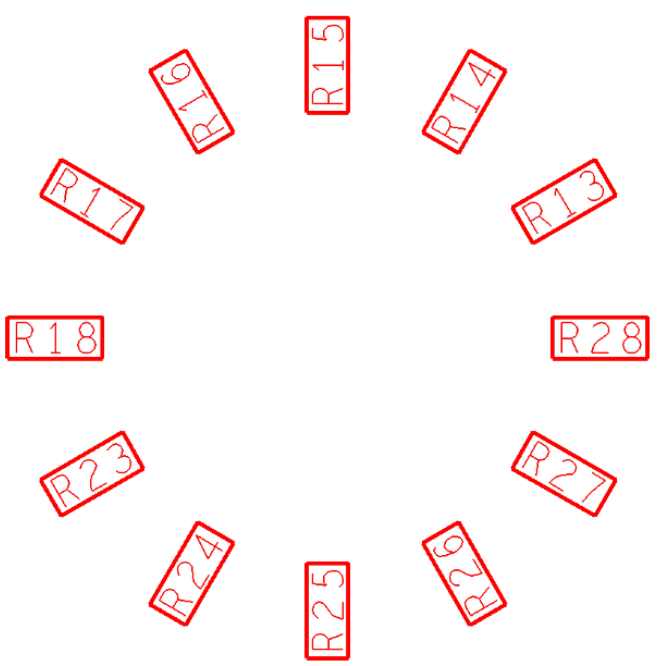
Result after running Label Tune

Label Tune

Another example

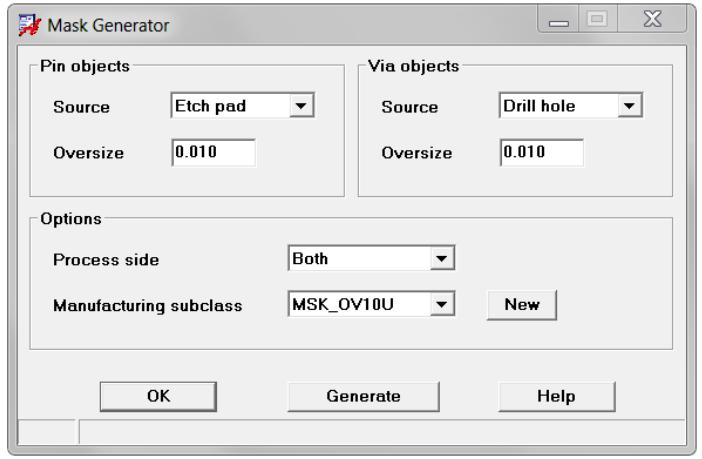


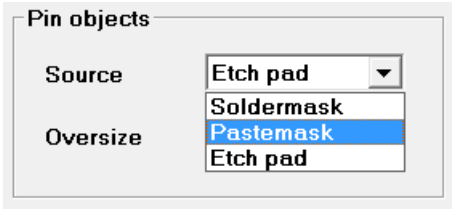


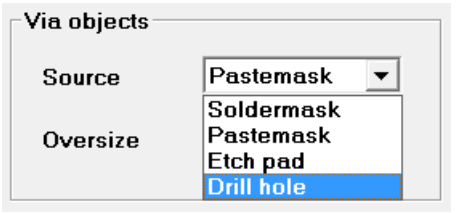


Mask Generator

- In some cases customers may want to oversize mask data (soldermask, pastemask) due to manufacturing requirements
- Data will be generated on manufacturing subclass. The original padstacks won't be touched
- Input parameters
  - Source data ("What to oversize") can be specified separately for vias and pins
  - Oversize values (positive and negative)
  - Side to process
  - Manufacturing subclass where data will be written to



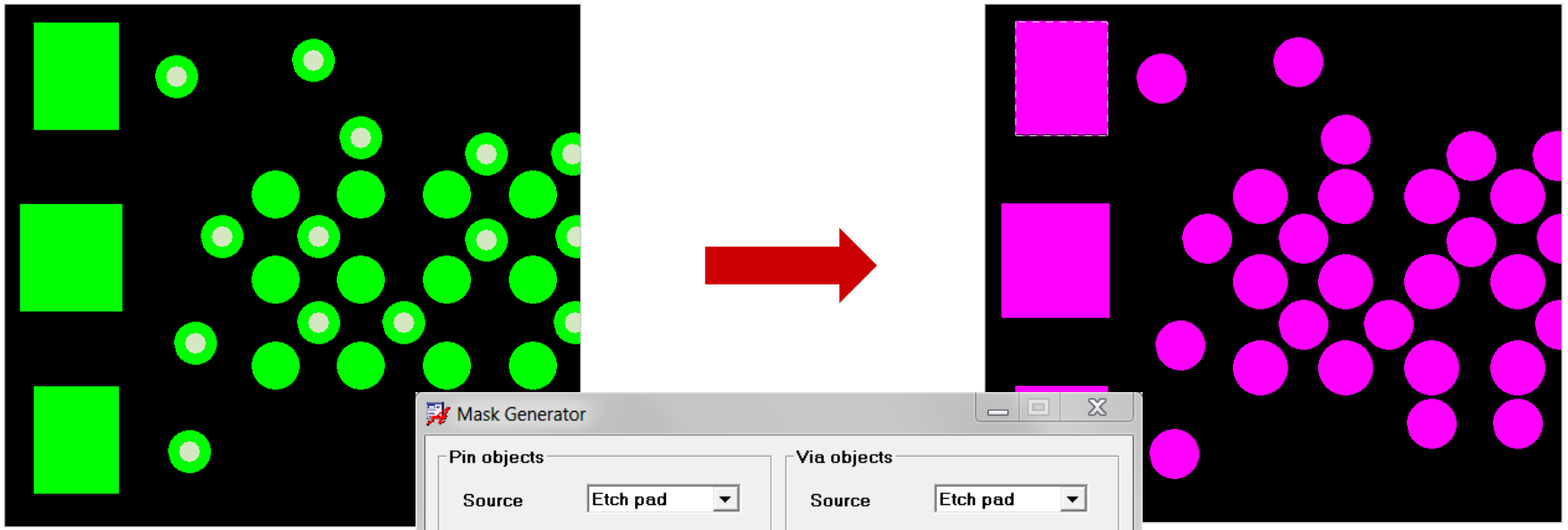


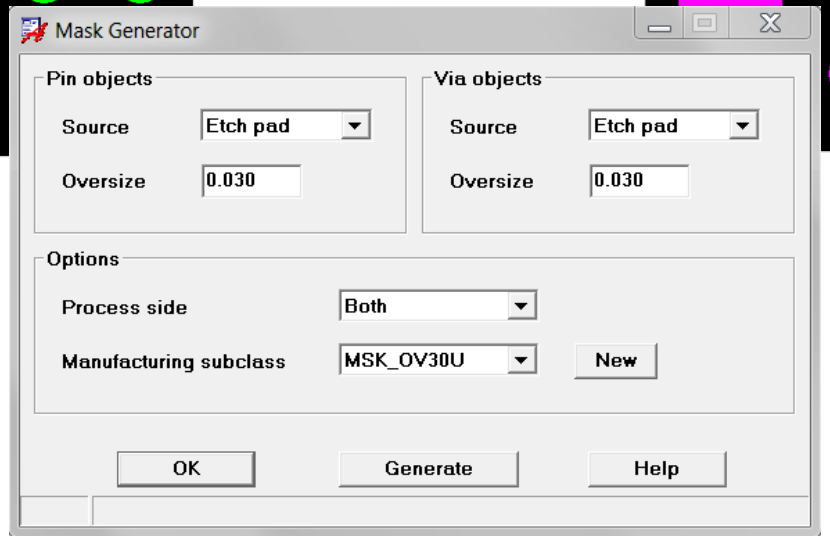


Mask Generator

Pins and vias on TOP

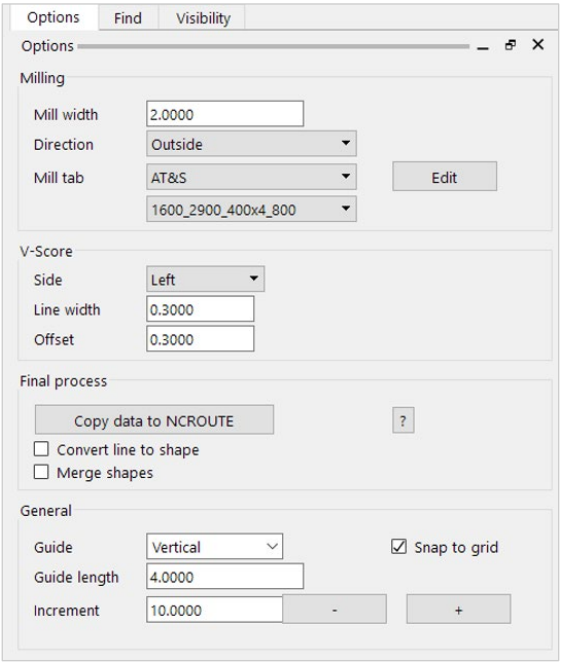
Manufacturing subclass MSK_OV30U_TOP



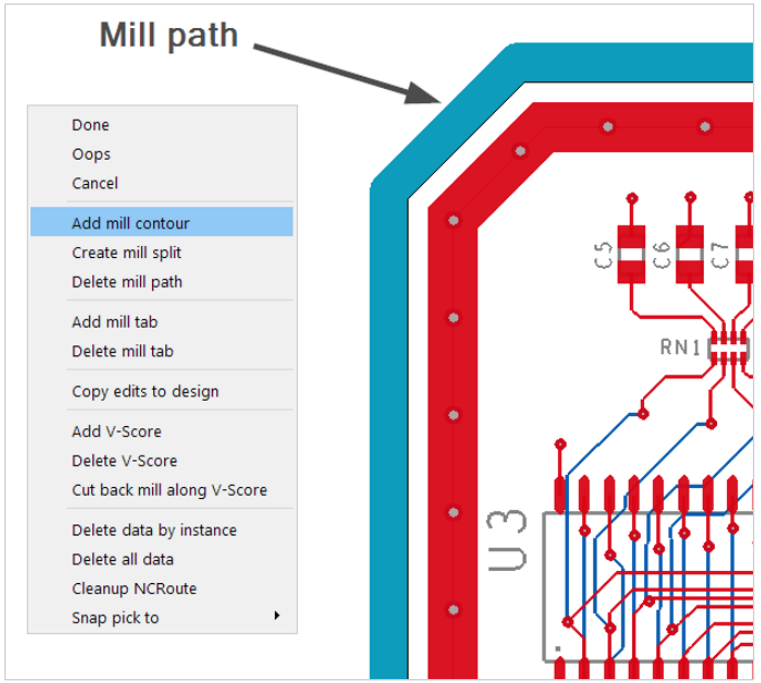


NC Panel Route

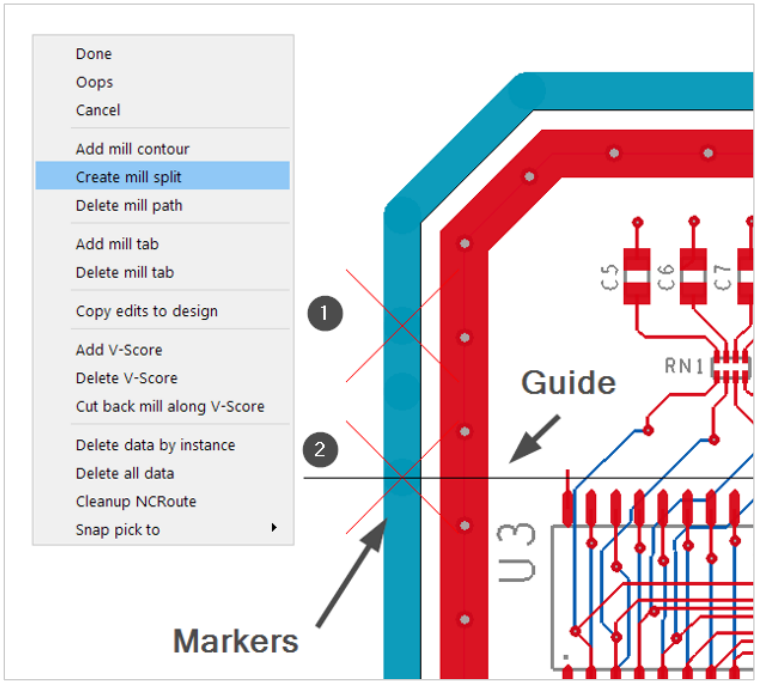
- Toolset supporting various techniques for PCBs in a panel to be easily separated after they are manufactured and assembled
- Mill tab panels
  - Add mill contour
  - Split & Cut mill
  - Add mill tabs with or without perforation drills
- V-Score panels



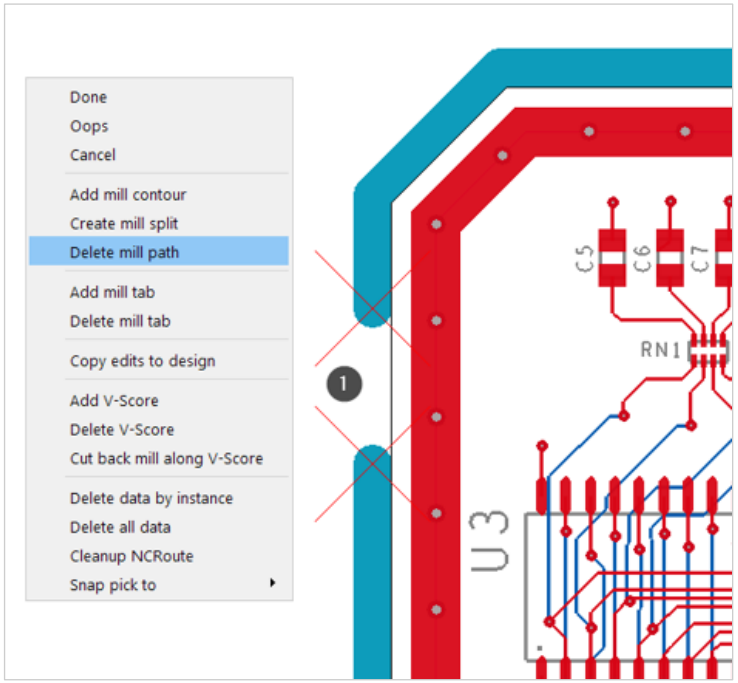
NC Panel Route



Add mill contour along the edge of the board



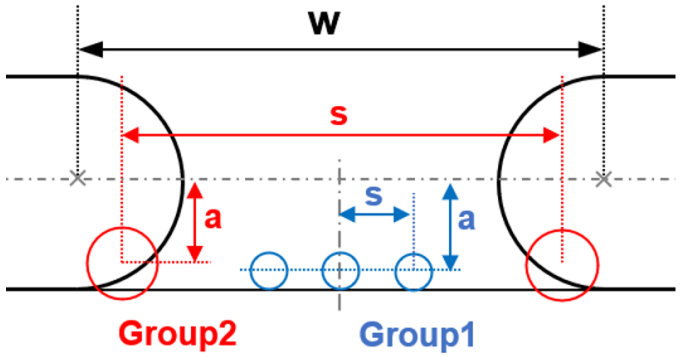
Create splits interactively

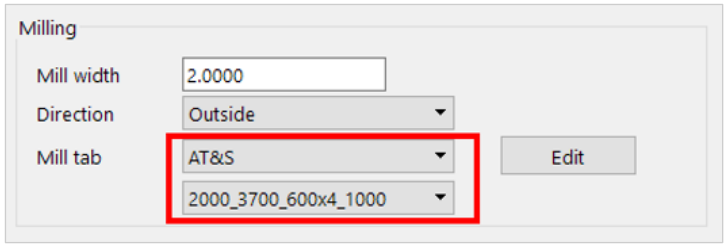


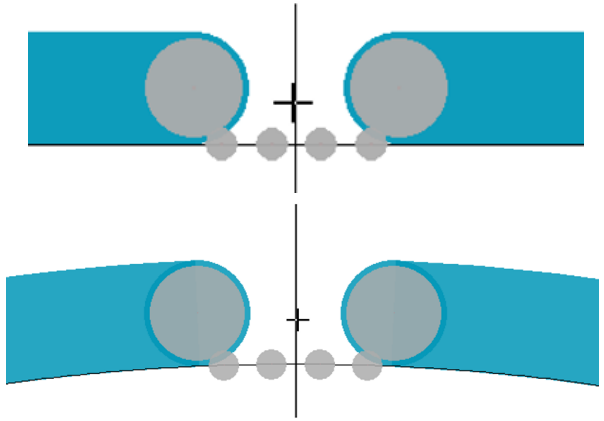
Delete splits

NC Panel Route

- Mill tabs can be specified with respect to
  - Tab size
  - Number of holes, diameter spacing and offset
- Application provides libraries from PCB fabricators
  - AT&S
  - Fineline
  - Alba PCB Group / Q-print electronic
- Interactive placement
  - Can be placed on any contour

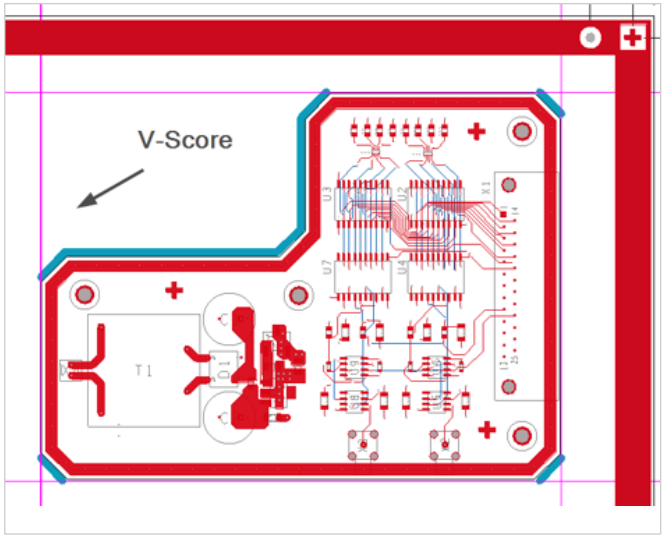


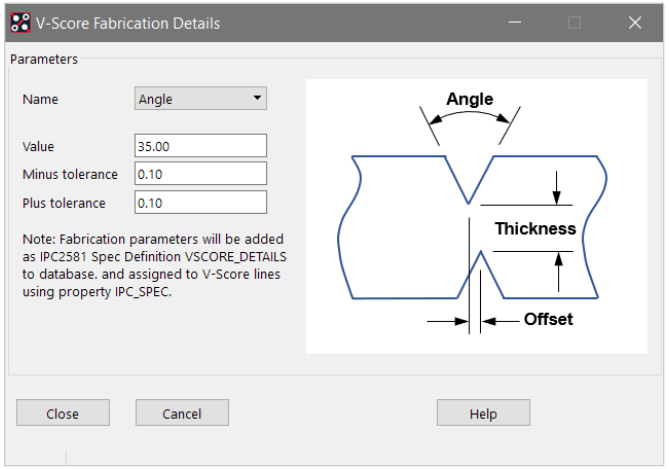




NC Panel Route

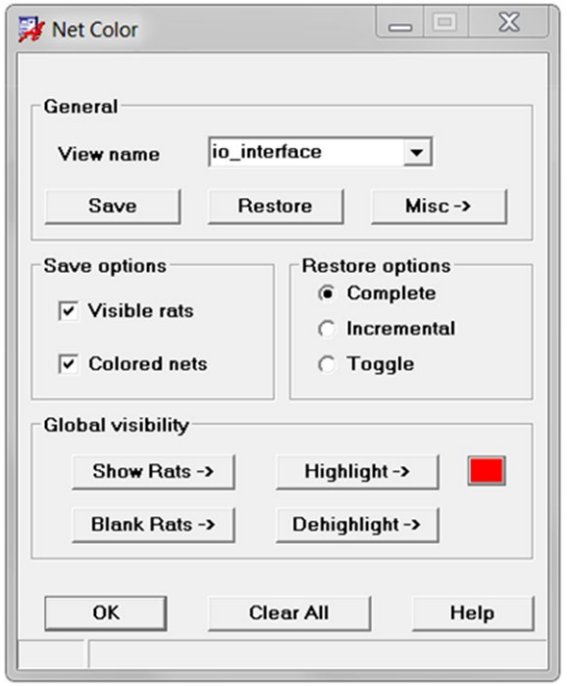
- V-Score lines can be defined in horizontal or vertical directions by selection an appropriate side of the board
- Existing milling can be cut back
- V-Score fabrication details can be specified which creates an IPC-2581 Spec Definition entry in the database

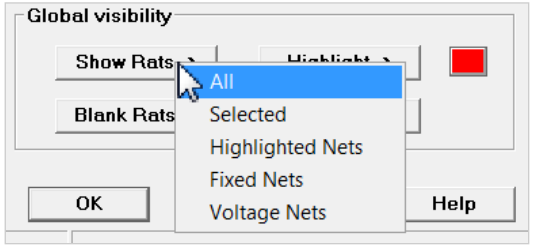


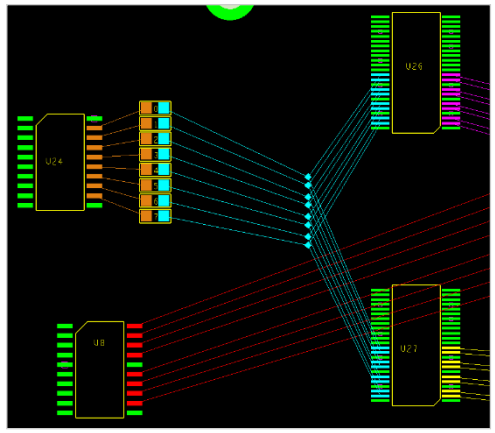


Net Color View

- Allows saving and restoring net color and rat visibility settings
- Useful for floor planning and route feasibility studies
- Global visibility commands
  - Useful hands-on for configuring a view (display / blank rats and assign net colors)
  - Find By Name support
  - No need for jumping and travelling to standard commands from **PCB Editor**

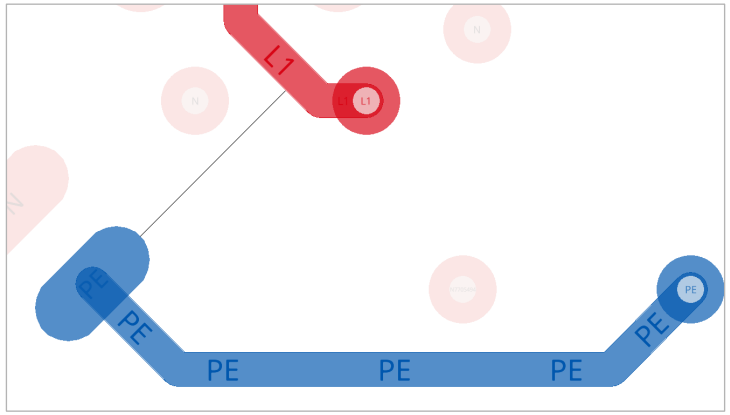


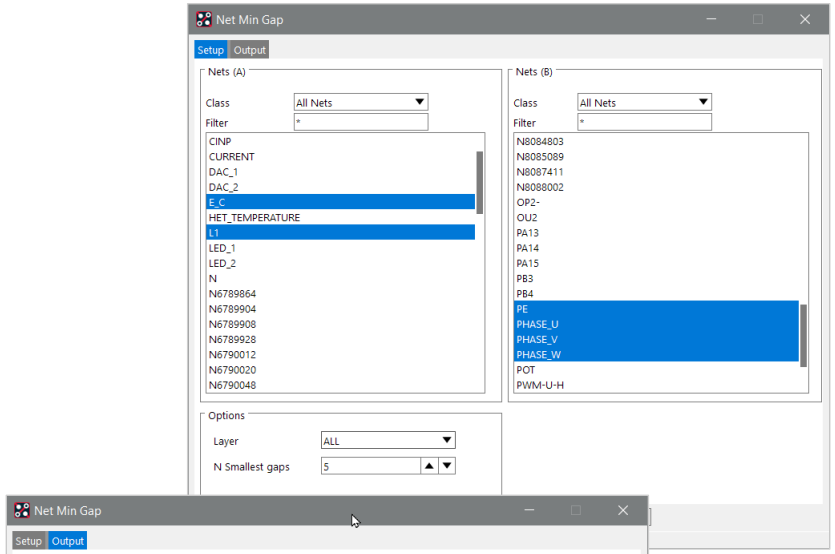


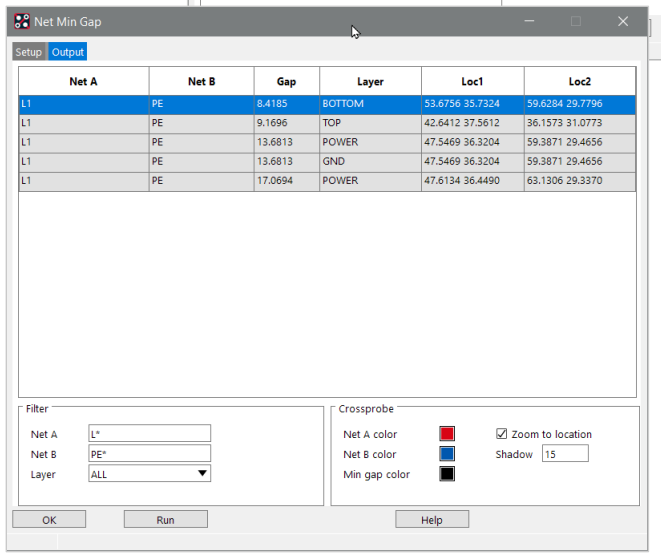


Net Min Gap

- Measures the smallest gap between two nets without adjusting DRC spacing rules
- Features
  - Multiple nets selection
  - Filter by spacing class including wildcard
  - Restrict measurements to certain layers
  - N smallest gaps (e.g. **Report 3 smallest values for a given net-net combination**)
  - Output tab with cross probing
  - Export results to CSV

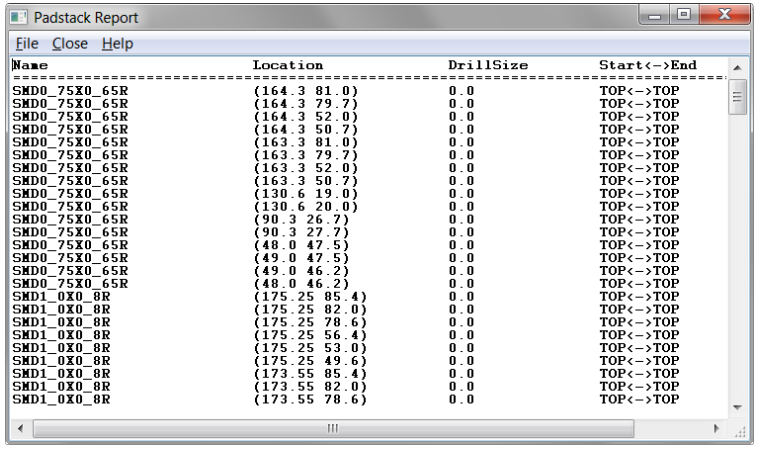


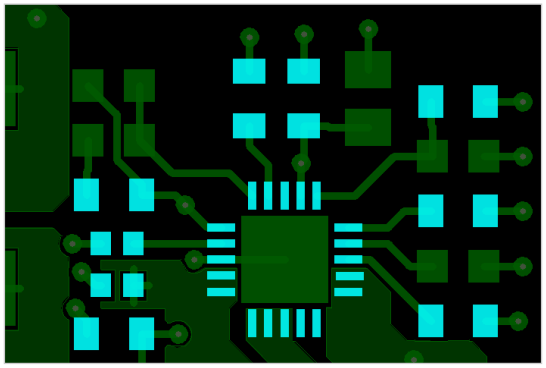


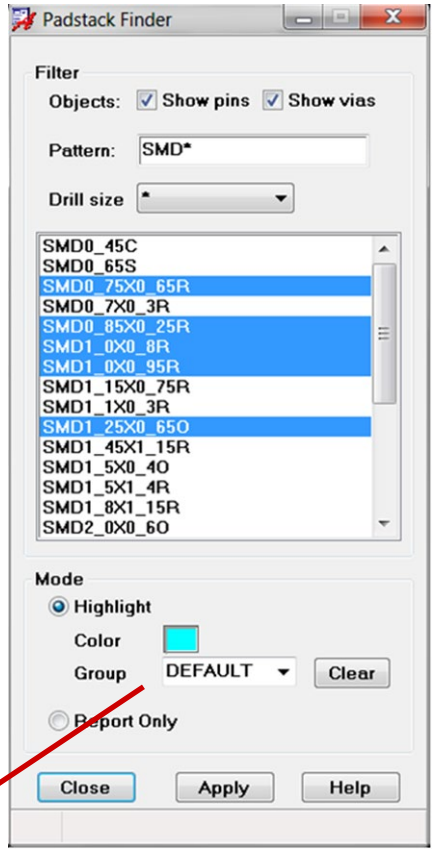


Padstack Finder

- Enables users to search and navigate for padstacks in the current design
  - Filter capabilities
    - Distinguish between pins and vias
    - Padstack name
    - Drill size
    - Wildcard support
  - Highlight and cross probe
  - Color by group

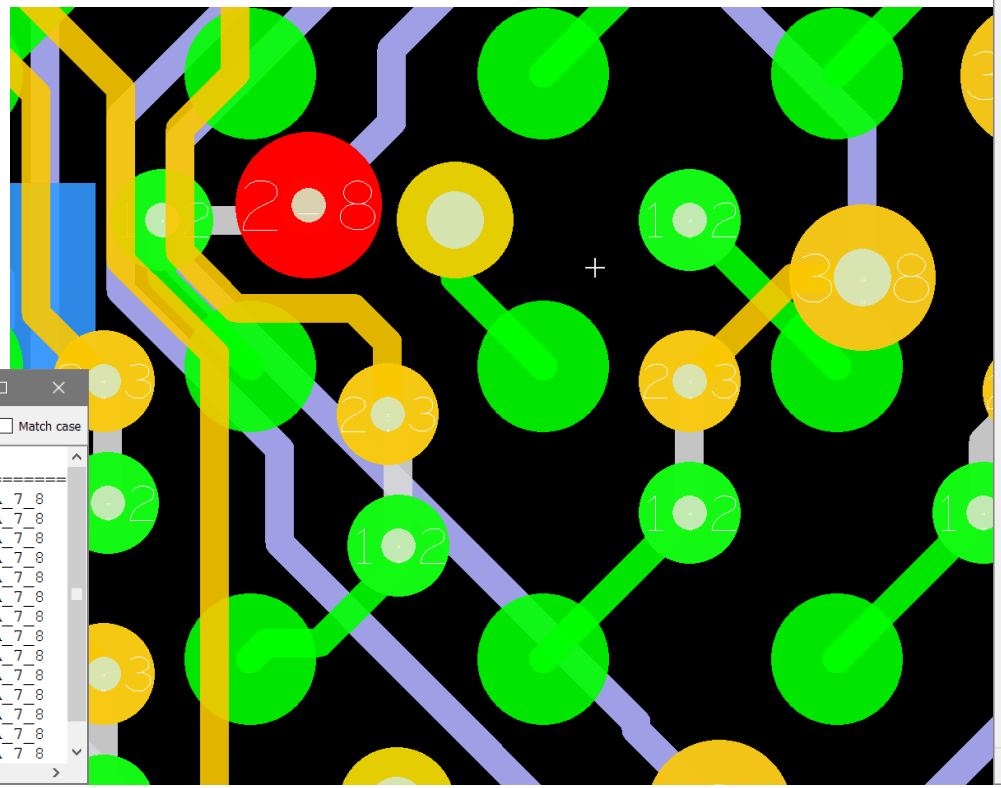


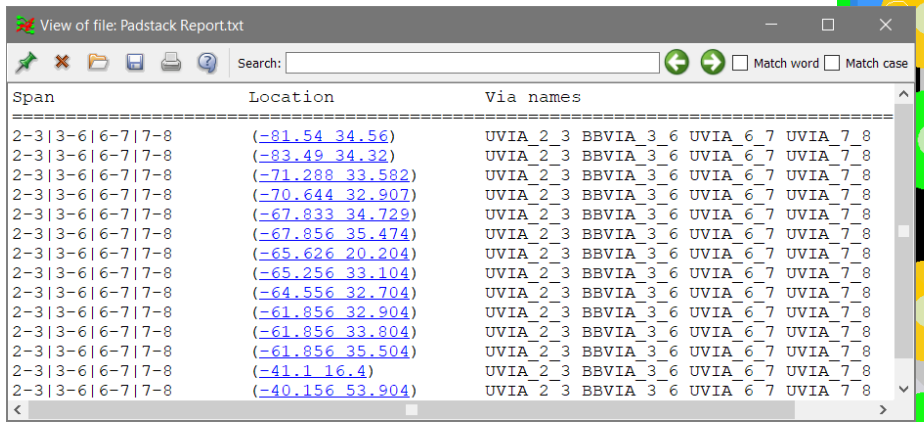


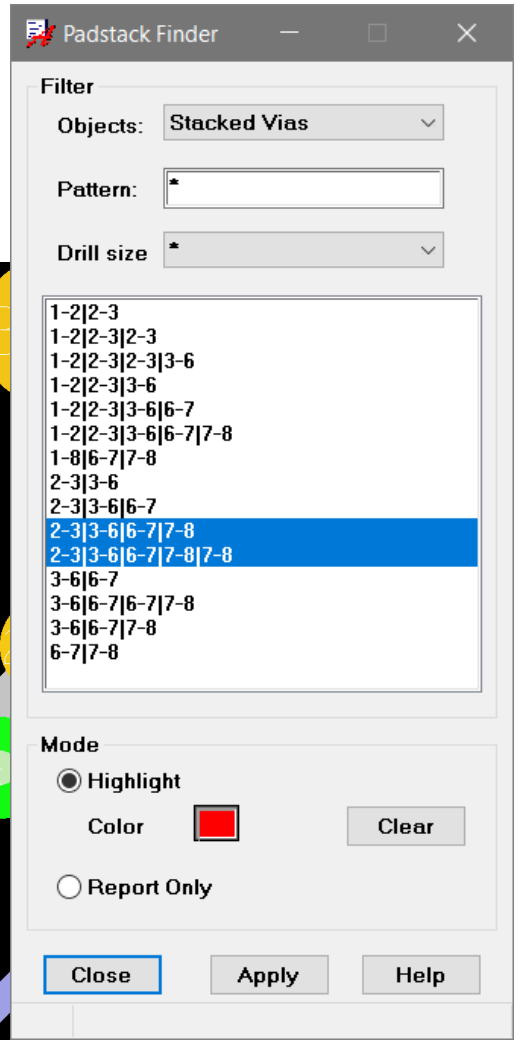


Padstack Finder

- Now supporting Vias Stacks
  - Display label formed by individual drill spans
  - Highlight and cross probe

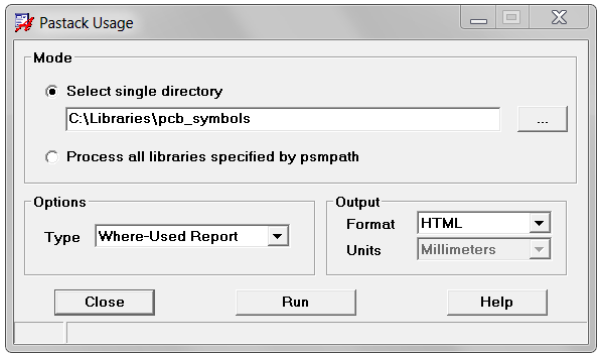


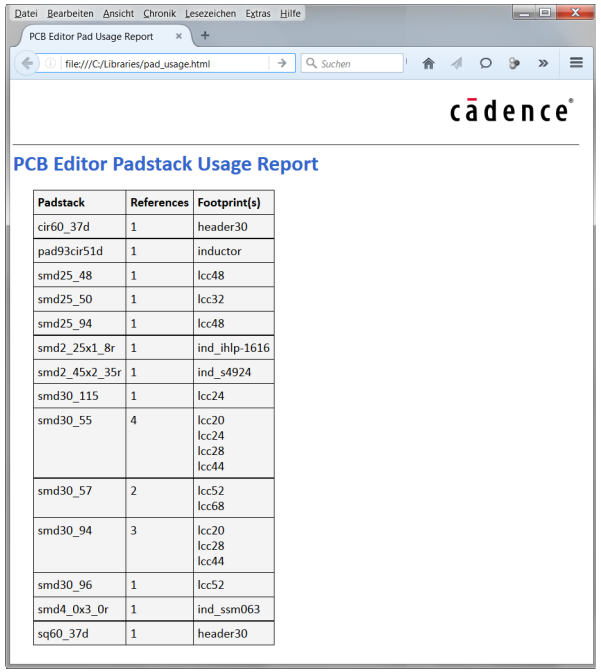




Padstack Usage

- Generate padstack reports by extracting data from PCB Editor symbol libraries (*.dra). Different reports are available:
- Report types
  - Where-Used
    Lists all footprints that use a given padstack
  - Padstack Standard
    Lists the padstack definitions for a given footprint
  - Padstack Detailed
    Lists detailed information for a given footprint. This information includes number of pins, vias and mechanical pins, pin numbers, xy coordinates, etc.
- Report format
  - HTML
  - Excel
  - Text

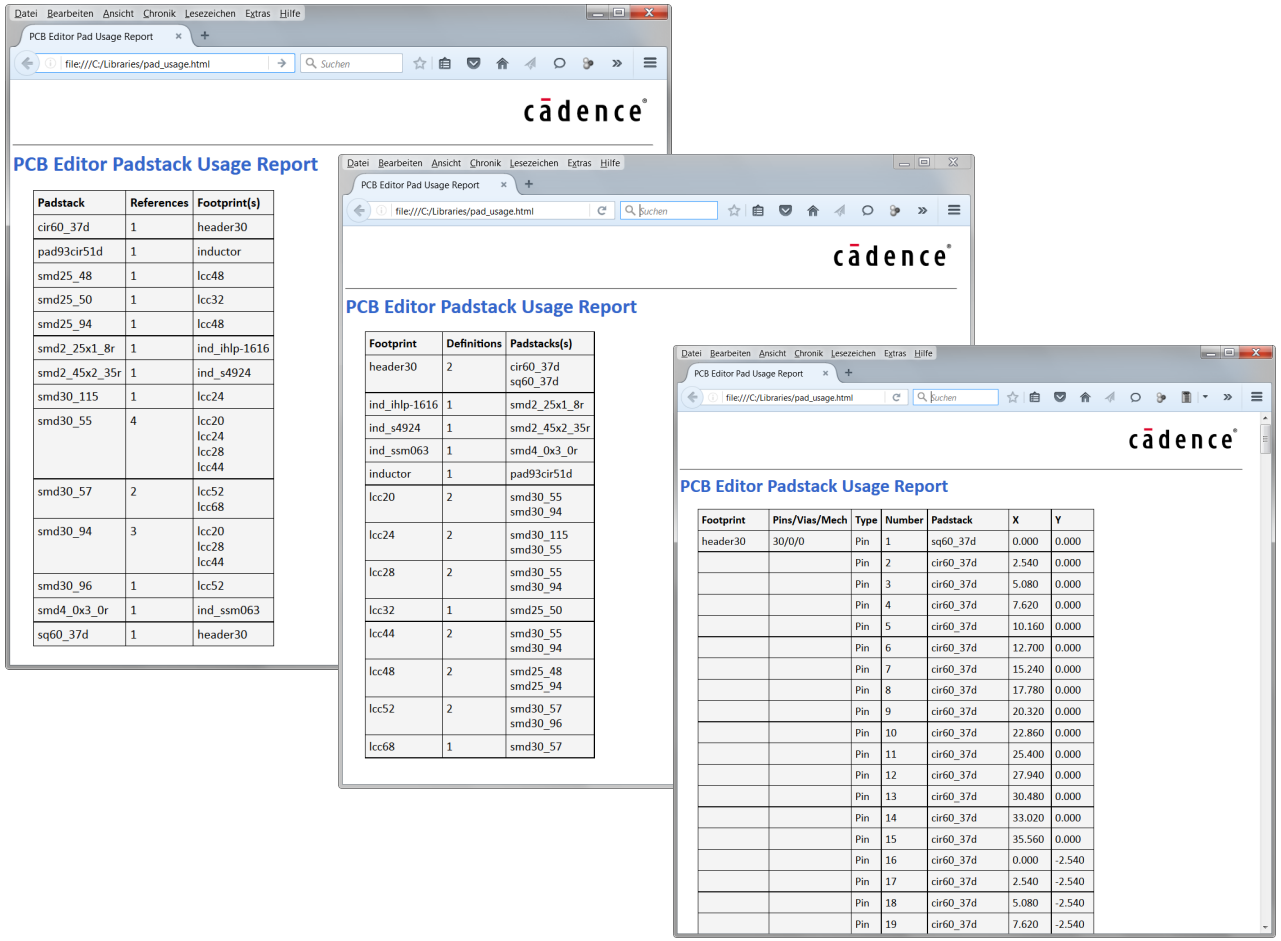




Padstack	References	Footprint(s)
cir60_37d	1	header30
pad93cir51d	1	inductor
smd25_48	1	lcc48
smd25_50	1	lcc32
smd25_94	1	lcc48
smd2_25x1_8r	1	ind_ihlp-1616
smd2_45x2_35r	1	ind_s4924
smd30_115	1	lcc24
smd30_55	4	lcc20 lcc24 lcc28 lcc44
smd30_57	2	lcc52 lcc68
smd30_94	3	lcc20 lcc28 lcc44
smd30_96	1	lcc52
smd4_0x3_0r	1	ind_ssm063
sq60_37d	1	header30

Padstack Usage

Report examples



PCB Editor Padstack Usage Report

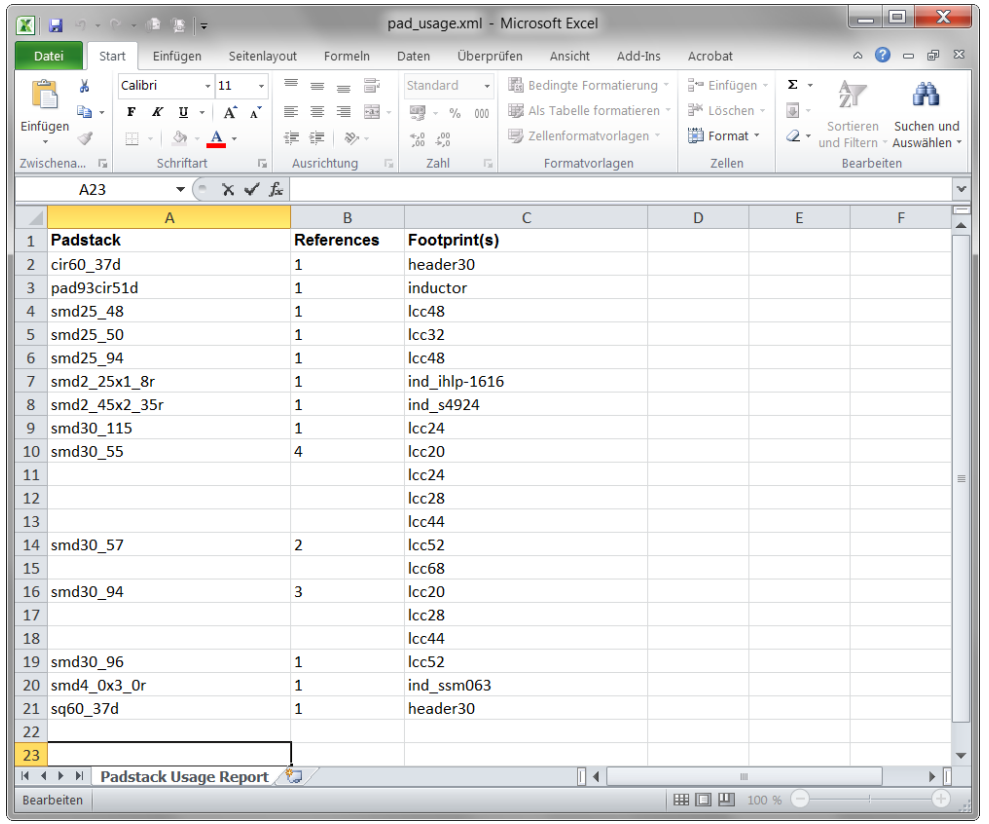
Padstack	References	Footprint(s)
cir60_37d	1	header30
pad93cir51d	1	inductor
smd25_48	1	lcc48
smd25_50	1	lcc32
smd25_94	1	lcc48
smd2_25x1_8r	1	ind_ihlp-1616
smd2_45x2_35r	1	ind_s4924
smd30_115	1	lcc24
smd30_55	4	lcc20 lcc24 lcc28 lcc44
smd30_57	2	lcc52 lcc68
smd30_94	3	lcc20 lcc28 lcc44
smd30_96	1	lcc52
smd4_0x3_0r	1	ind_ssm063
sq60_37d	1	header30

PCB Editor Padstack Usage Report

Footprint	Definitions	Padstacks(s)
header30	2	cir60_37d sq60_37d
ind_ihlp-1616	1	smd2_25x1_8r
ind_s4924	1	smd2_45x2_35r
ind_ssm063	1	smd4_0x3_0r
inductor	1	pad93cir51d
lcc20	2	smd30_55 smd30_94
lcc24	2	smd30_115 smd30_55
lcc28	2	smd30_55 smd30_94
lcc32	1	smd25_50
lcc44	2	smd30_55 smd30_94
lcc48	2	smd25_48 smd25_94
lcc52	2	smd30_57 smd30_96
lcc68	1	smd30_57

PCB Editor Padstack Usage Report

Footprint	Pins/Vias/Mech	Type	Number	Padstack	X	Y
header30	30/0/0	Pin	1	sq60_37d	0.000	0.000
		Pin	2	cir60_37d	2.540	0.000
		Pin	3	cir60_37d	5.080	0.000
		Pin	4	cir60_37d	7.620	0.000
		Pin	5	cir60_37d	10.160	0.000
		Pin	6	cir60_37d	12.700	0.000
		Pin	7	cir60_37d	15.240	0.000
		Pin	8	cir60_37d	17.780	0.000
		Pin	9	cir60_37d	20.320	0.000
		Pin	10	cir60_37d	22.860	0.000
		Pin	11	cir60_37d	25.400	0.000
		Pin	12	cir60_37d	27.940	0.000
		Pin	13	cir60_37d	30.480	0.000
		Pin	14	cir60_37d	33.020	0.000
		Pin	15	cir60_37d	35.560	0.000
		Pin	16	cir60_37d	0.000	-2.540
		Pin	17	cir60_37d	2.540	-2.540
		Pin	18	cir60_37d	5.080	-2.540
		Pin	19	cir60_37d	7.620	-2.540

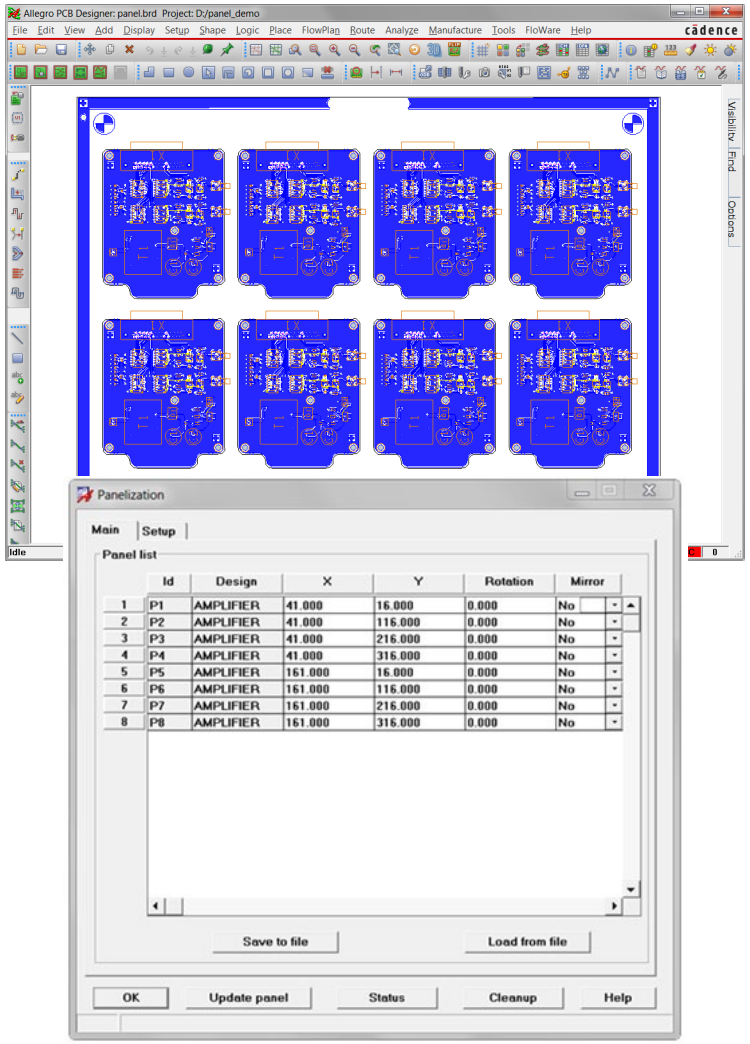


pad_usage.xml - Microsoft Excel

	A	B	C	D	E	F
1	Padstack	References	Footprint(s)			
2	cir60_37d	1	header30			
3	pad93cir51d	1	inductor			
4	smd25_48	1	lcc48			
5	smd25_50	1	lcc32			
6	smd25_94	1	lcc48			
7	smd2_25x1_8r	1	ind_ihlp-1616			
8	smd2_45x2_35r	1	ind_s4924			
9	smd30_115	1	lcc24			
10	smd30_55	4	lcc20			
11			lcc24			
12			lcc28			
13			lcc44			
14	smd30_57	2	lcc52			
15			lcc68			
16	smd30_94	3	lcc20			
17			lcc28			
18			lcc44			
19	smd30_96	1	lcc52			
20	smd4_0x3_0r	1	ind_ssm063			
21	sq60_37d	1	header30			
22						
23						

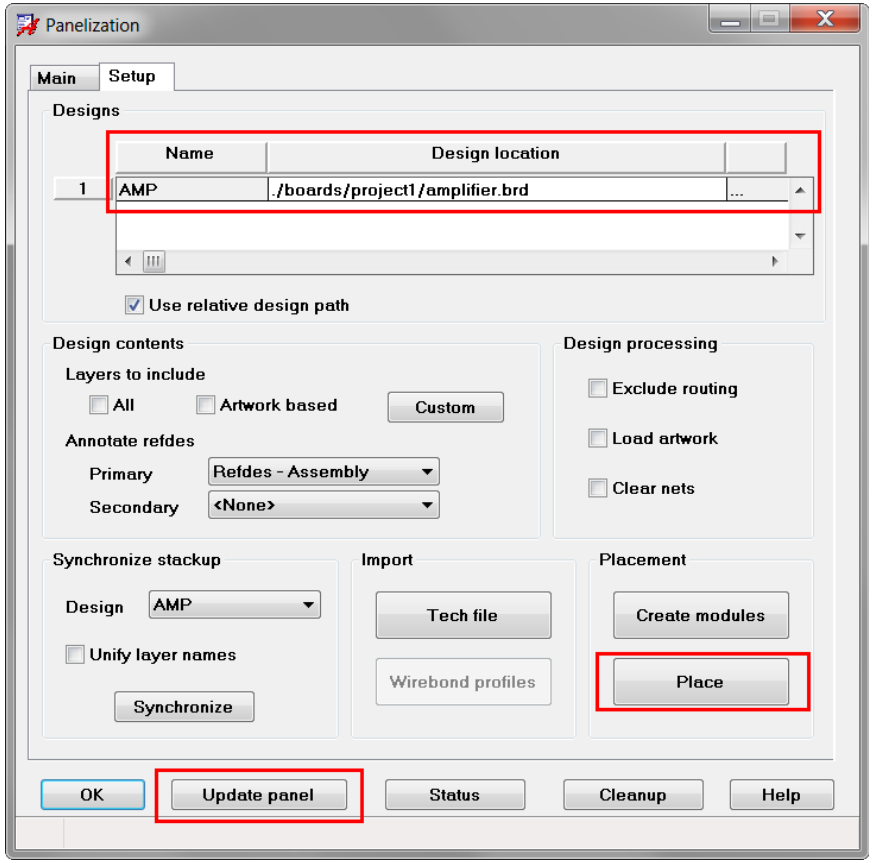
Panelization

- Simplifies panel documentation process
- Boards can be stepped individually or by array
- Boards can be rotated and / or mirrored individually
- Automatic update
- Automatic notification if boards have been modified
- Based on proven **mdd**-Technology **(Design Reuse, Place Replicate)**
- Supports standard panels as well as family panels
- Configuration stored in database



Panelization

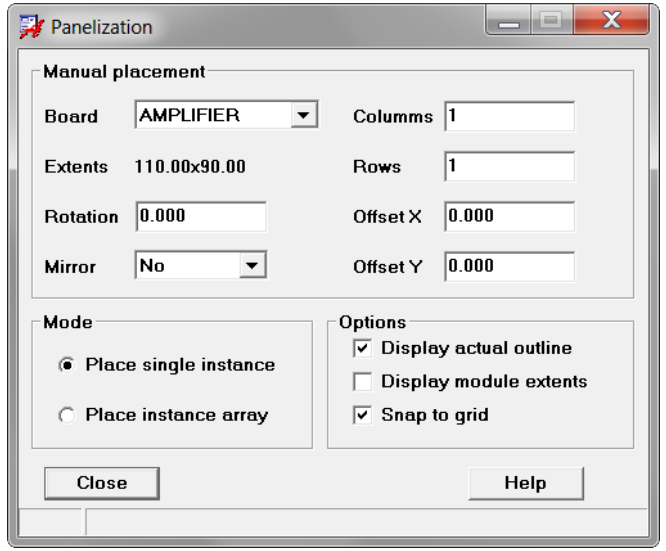
- **Setting up a new panel**
  - Open a new database or panel template
  - Launch **FloWare > Panelization**
  - Link your boards
  - Create modules
  - Place a single instance or an array of your board
  - Done
- **Updating an existing panel**
  (e.g. original layouts have been modified)
  - Open the panel database
  - Launch **FloWare > Panelization**
  - Choose Update panel
  - Done
  - Create manufacturing data as usual …

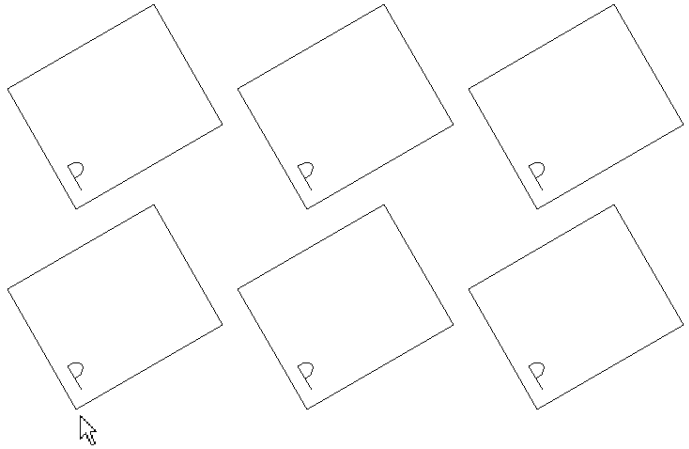


Panels – Made easy

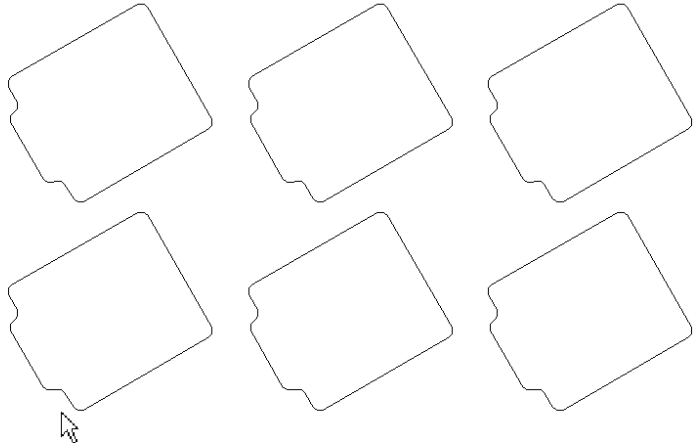
Panelization

- Interactive placement
  - Place single instances or array
  - Dynamic preview attached to cursor (board size, orientation, rotation, mirror)
  - Display design bounding box or actual outline
  - Snap to grid option





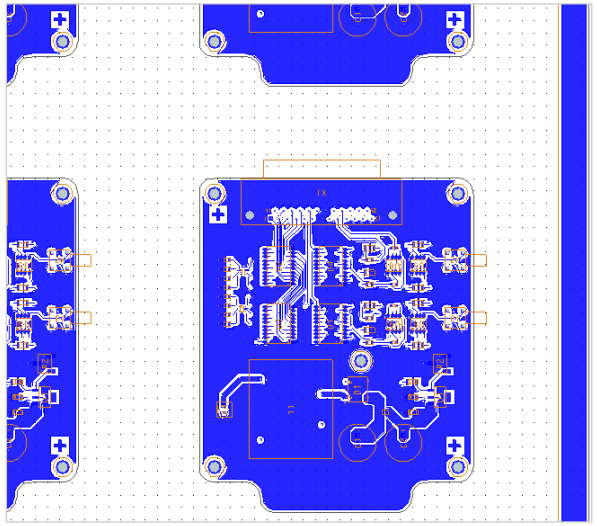
Display bounding box

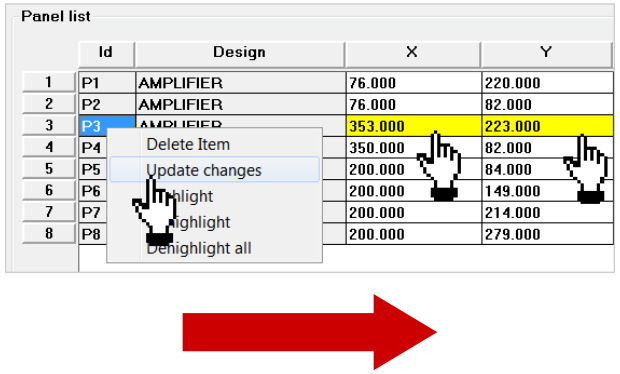


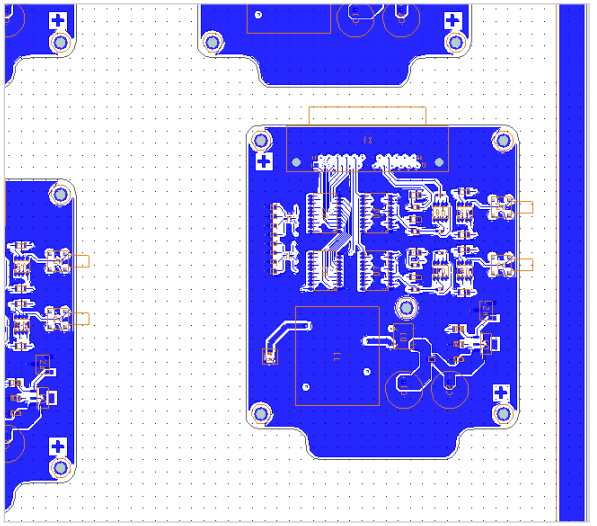
Display actual outline

Panelization

- Panel modifications
  - Change parameters (e.g. x, y) of instance to be changed
  - Fields become yellow
  - Choose context menu Update changes to confirm

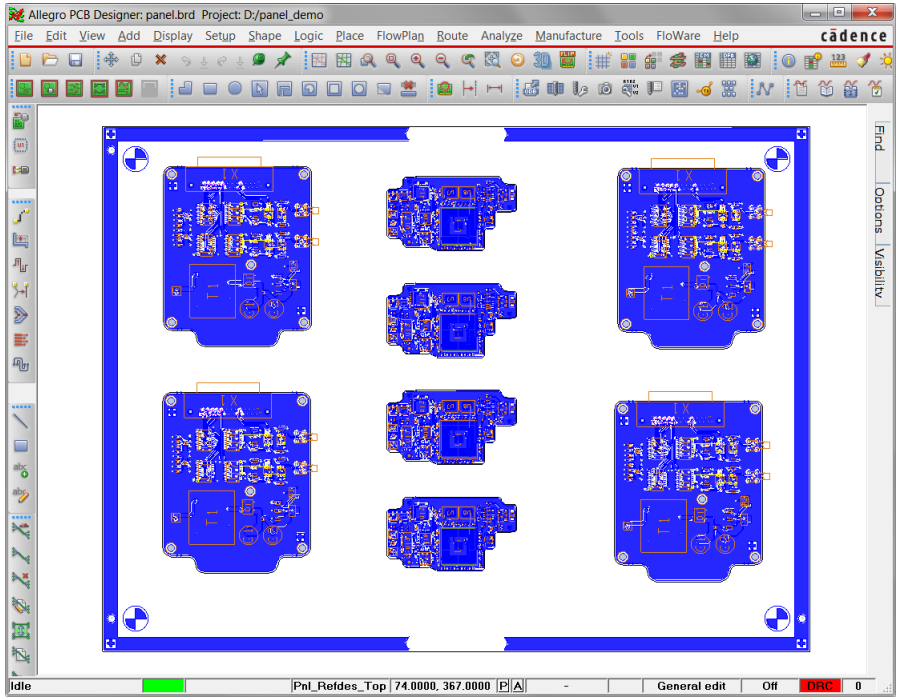


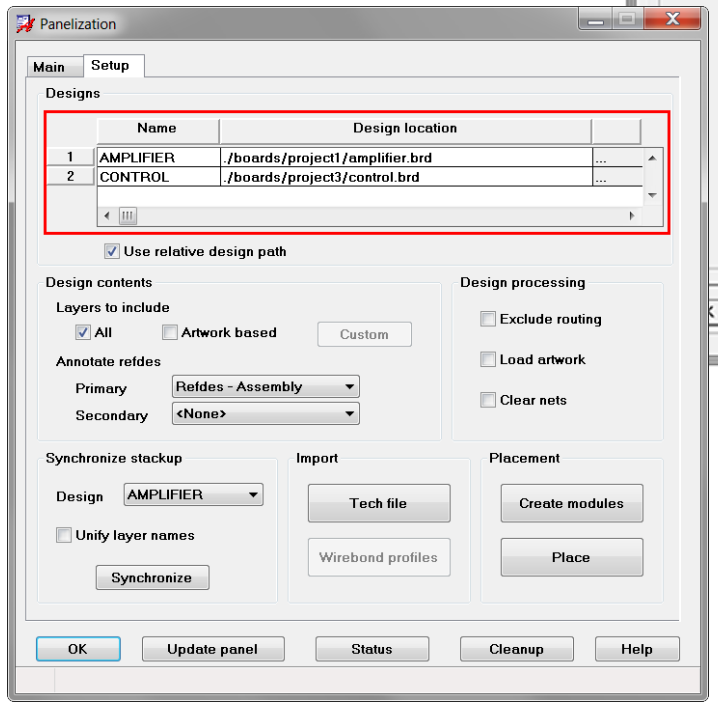


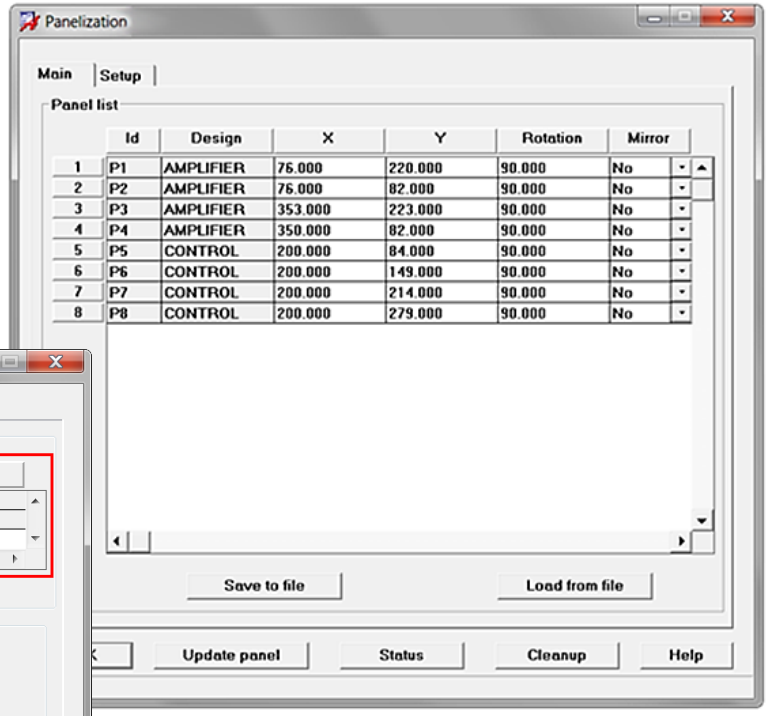


Panelization

- Family panels
  - Contain more than one board layout
  - Simply link the board databases
  - Make your placement

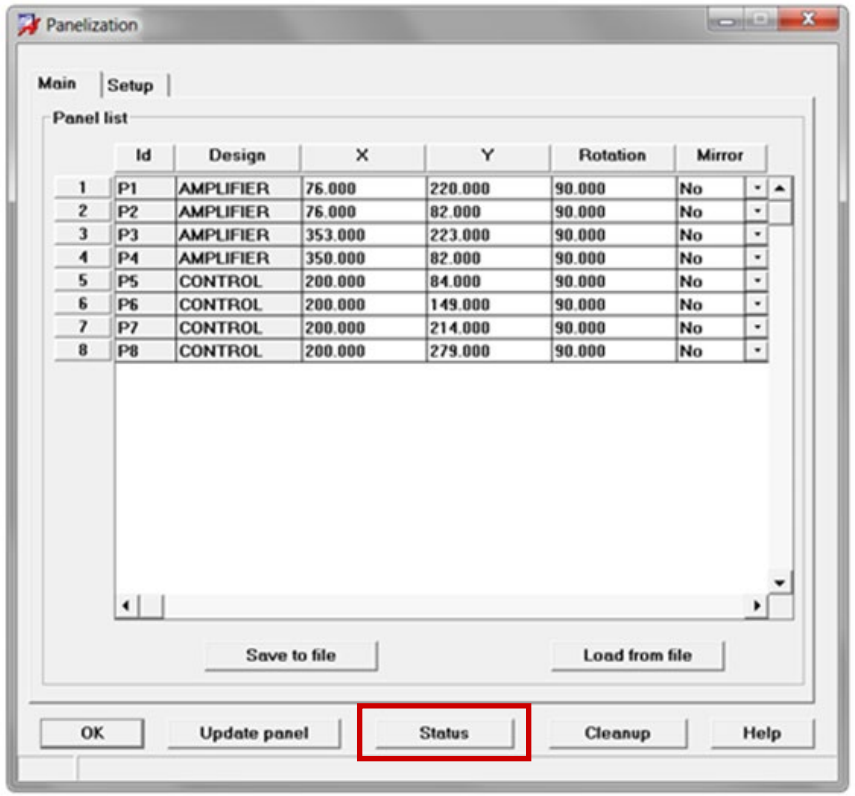


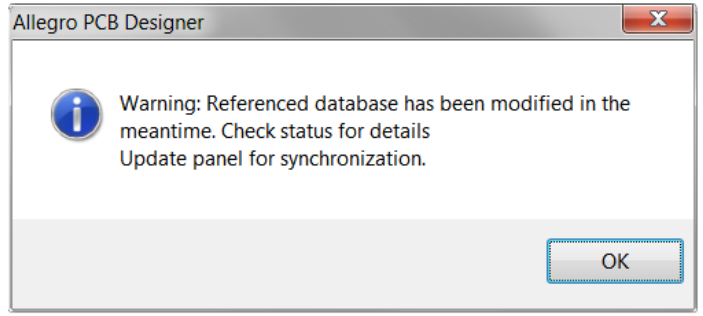


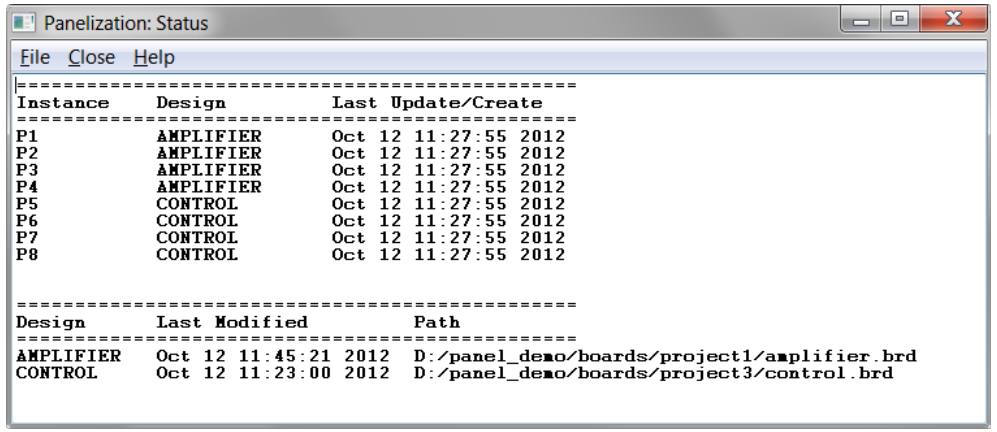


Panelization

- Panel status
  - Automatic notification when board databases have been modified
  - Status report gives details about time stamps

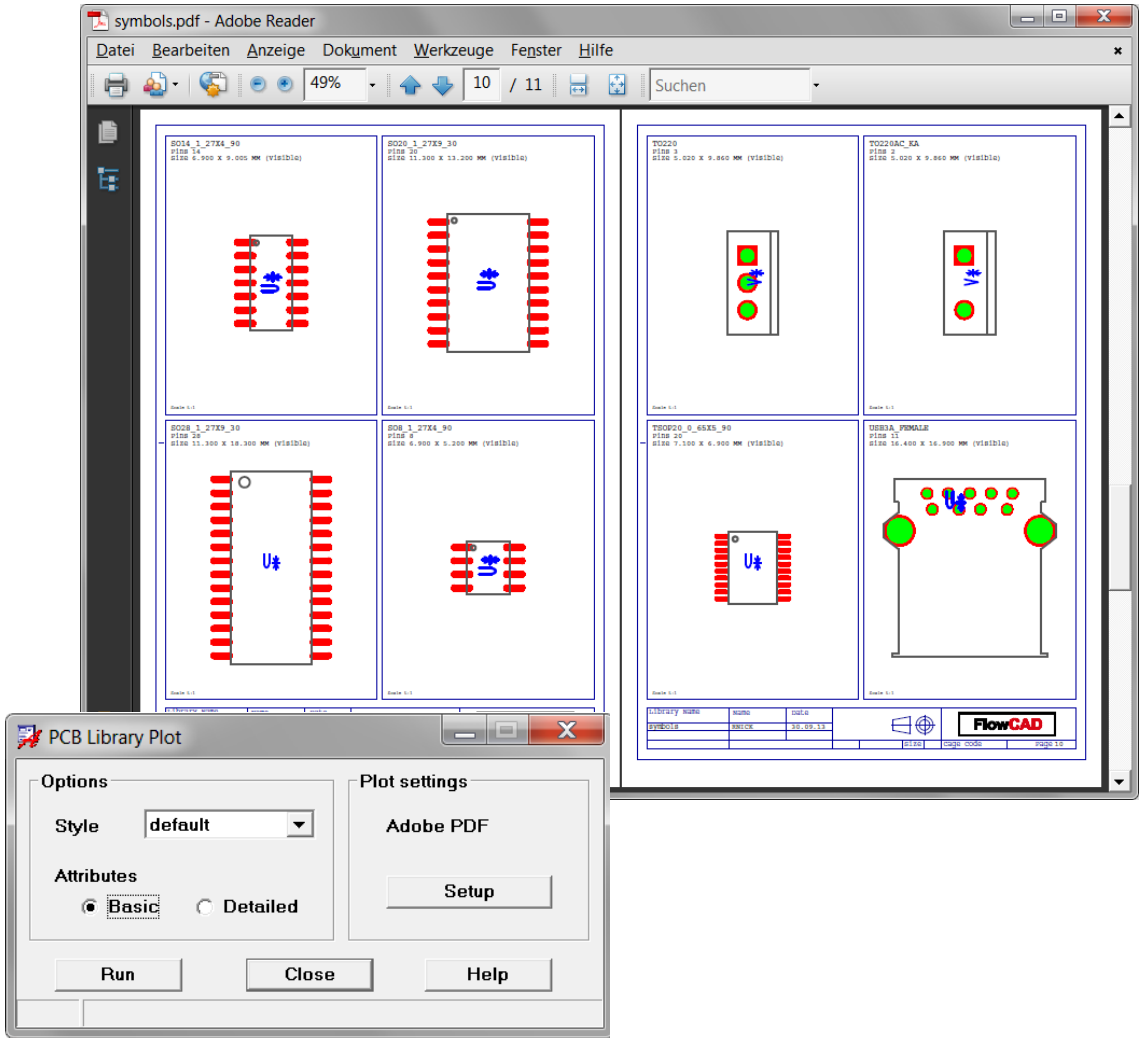






PCB Library Plot

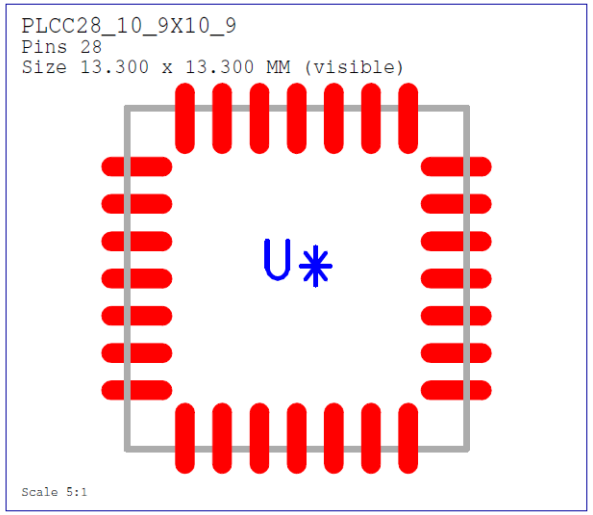
- Documentation of PCB footprints within a selected library
  - Includes graphical representation of footprint graphics
  - Graphics will be scaled into dedicated areas for better readability
  - Additional attributes (size, pitch, padstacks used etc.) are automatically extracted and written to the document
  - Frame templates are provided
  - Customizable contents and drawing styles including drill holes
  - One single PDF document for all footprints

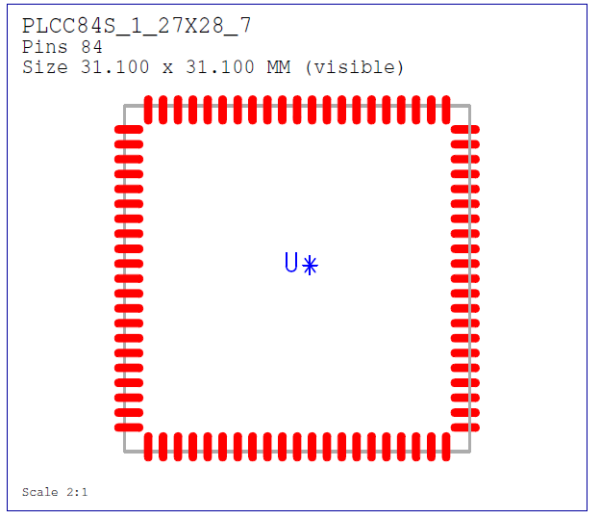


PCB Library Plot

Default Mode

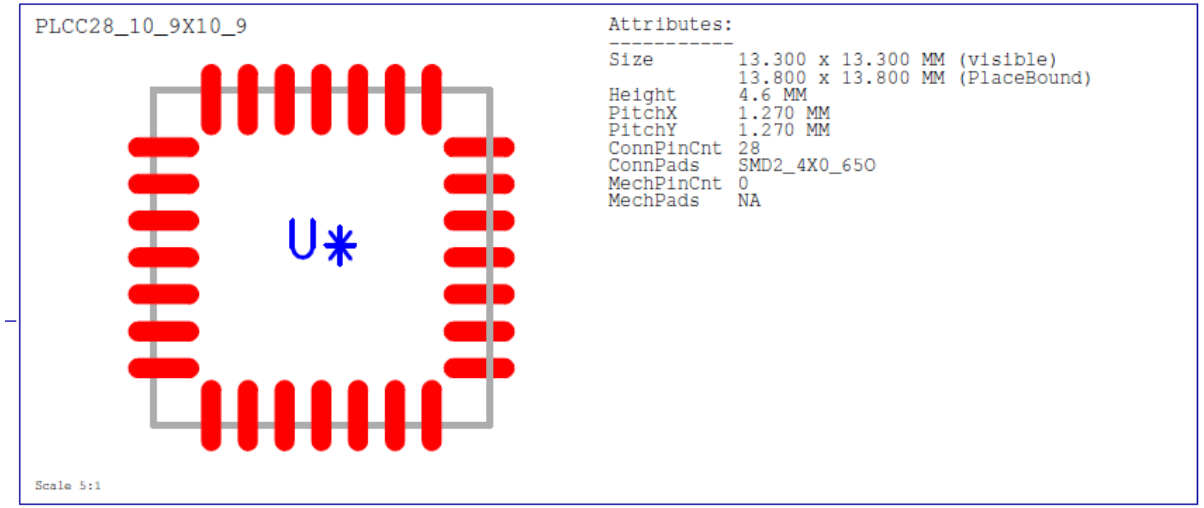
- Basic information
- More footprints per page





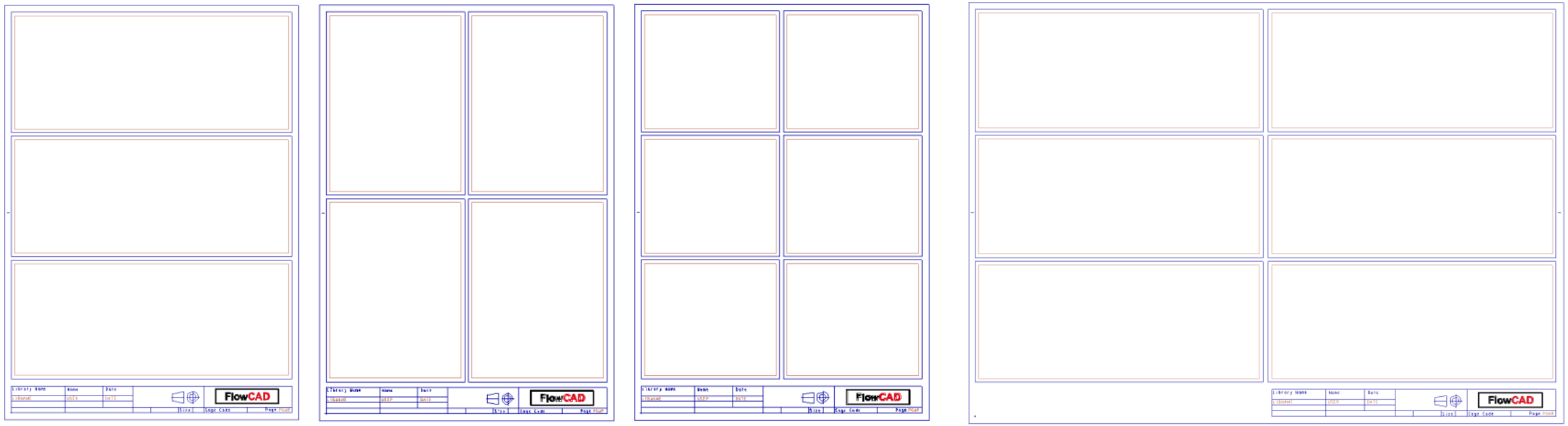
Detailed Mode

- Additional information
- Less footprints per page



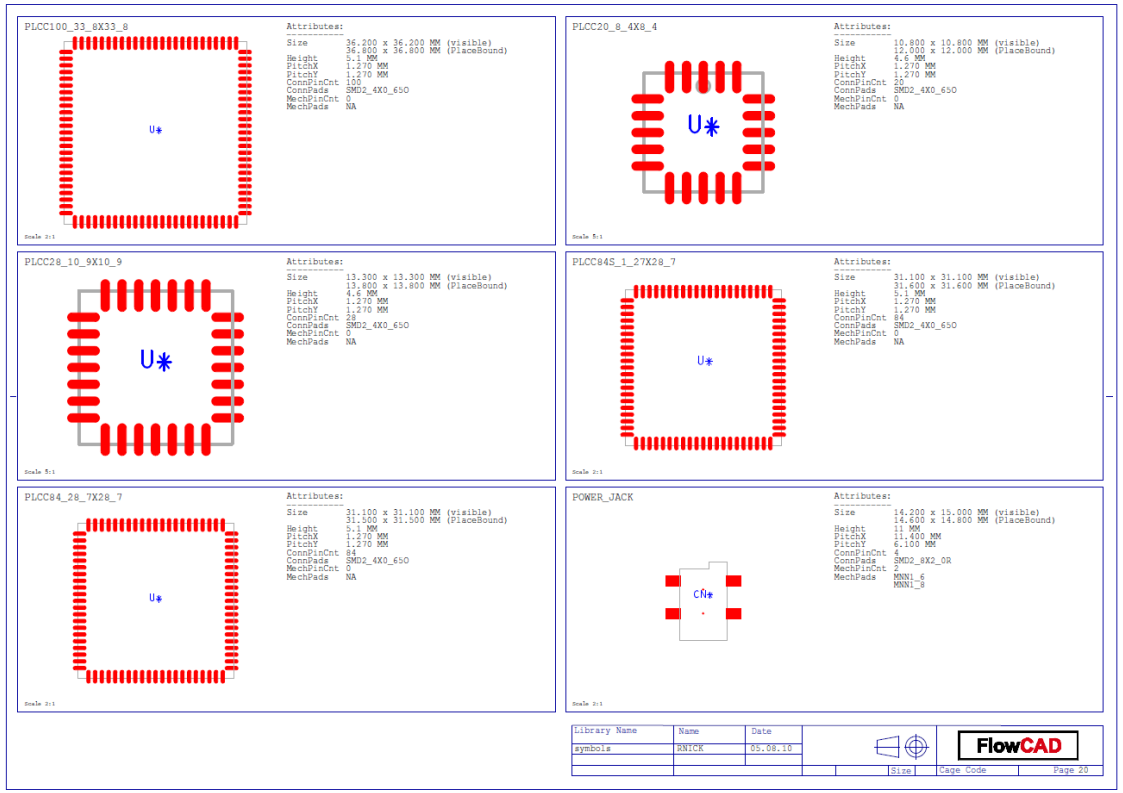
PCB Library Plot

- Templates
  - Define the areas to be used for plotting which correlates to the number of footprints per page
  - Metadata support for title blocks (page number, date, user, library name)
  - Default templates provided
  - Customer can define his own templates



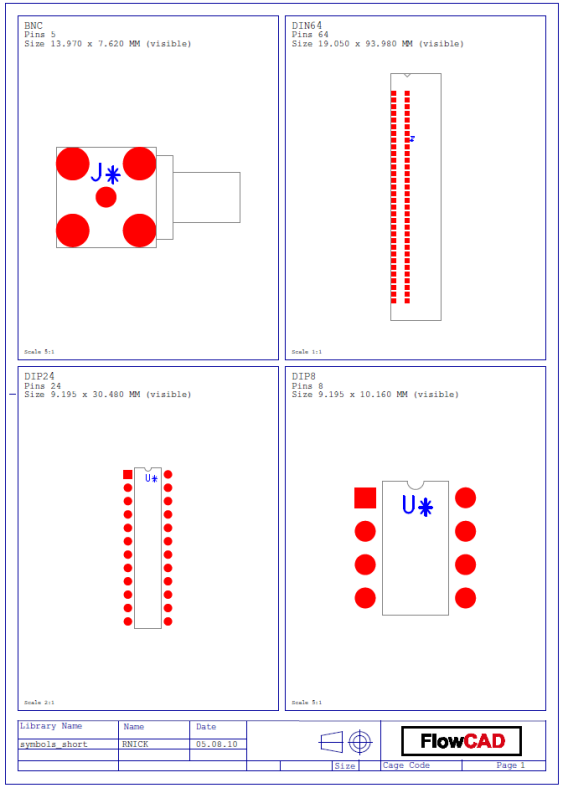
PCB Library Plot

Examples



6 footprints on A3

Detailed attributes

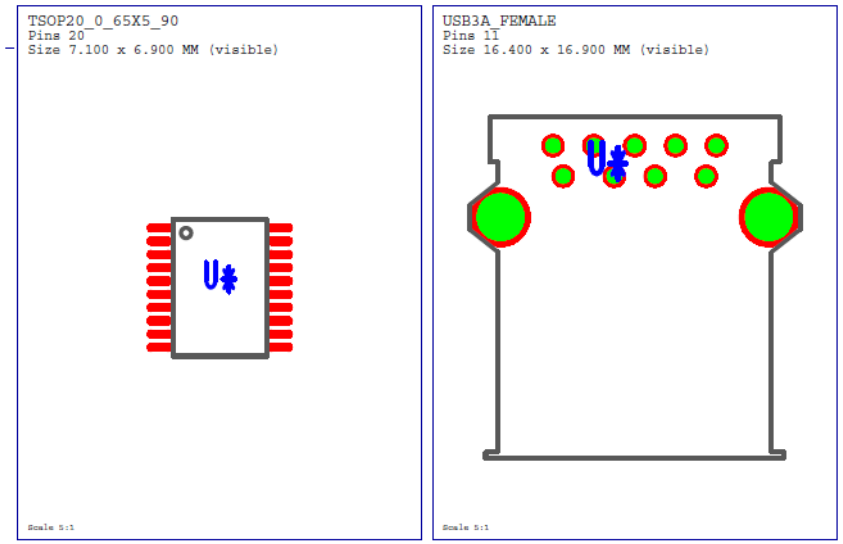


4 footprints on A4

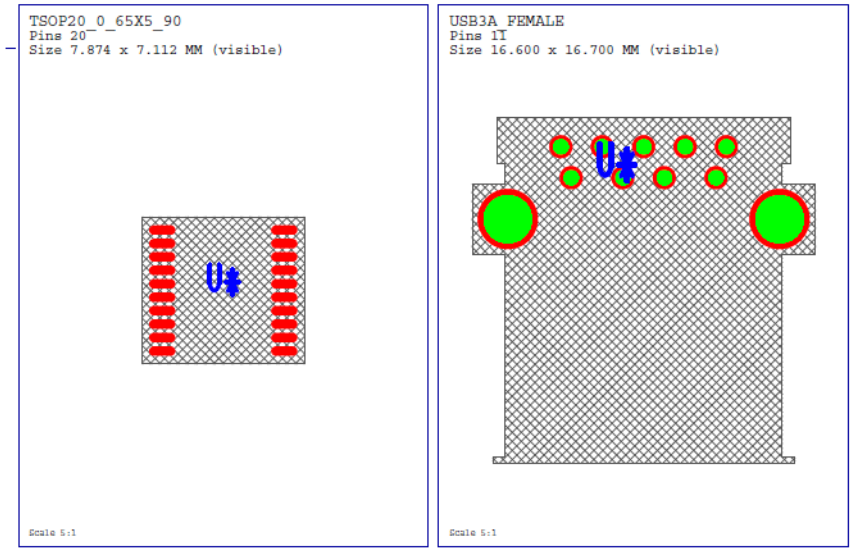
Basic attributes

PCB Library Plot

Customizable content including drill holes and various drawing styles



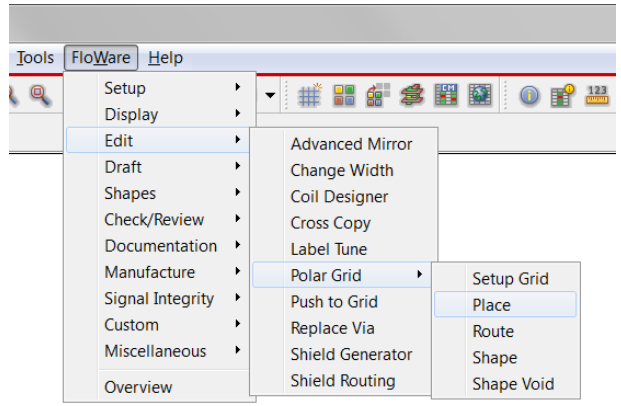
Assembly TOP including etch and drill holes

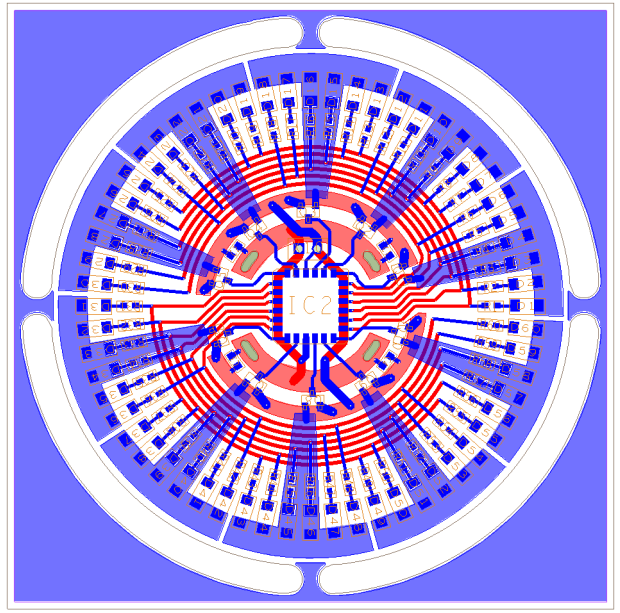


Placebound as hatch shape including etch and drill holes

Polar Grid Utilities

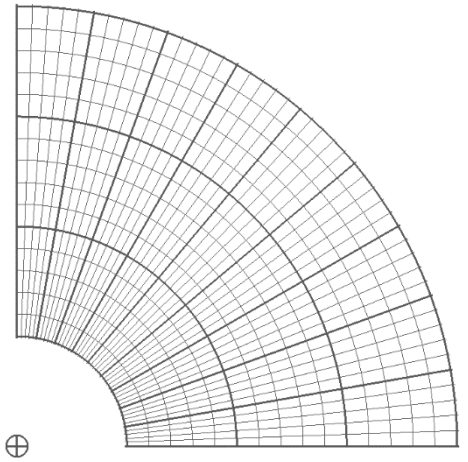
- Useful for boards where circular placement and routing is required
- Providing a set of functions
  - Defining and editing a polar grid
  - Polar placement
  - Polar routing
  - Polar shape editing including voids
- Snap control
  - Coarse and fine grid
  - System grid
- Polar grid can be also used in conjunction with standard PCB Editor commands using **RMB > Snap pick to > Intersection**

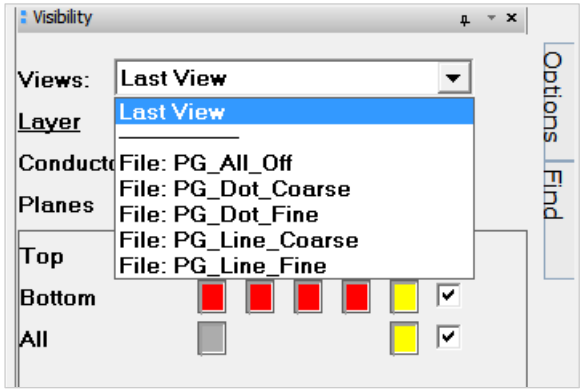


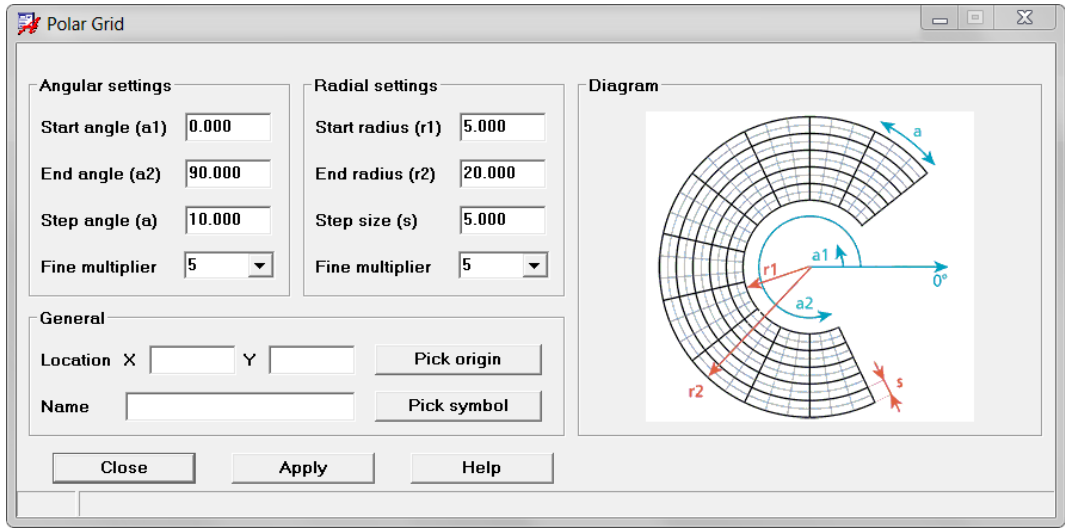


Polar Grid Utilities

- **Polar Grid Setup**
  - Define a new grid
  - Edit an existing grid
  - Fully parameterized
  - Coarse and fine grid settings
  - Line and dot style support
  - Stored as format symbol in database
  - Visibility control

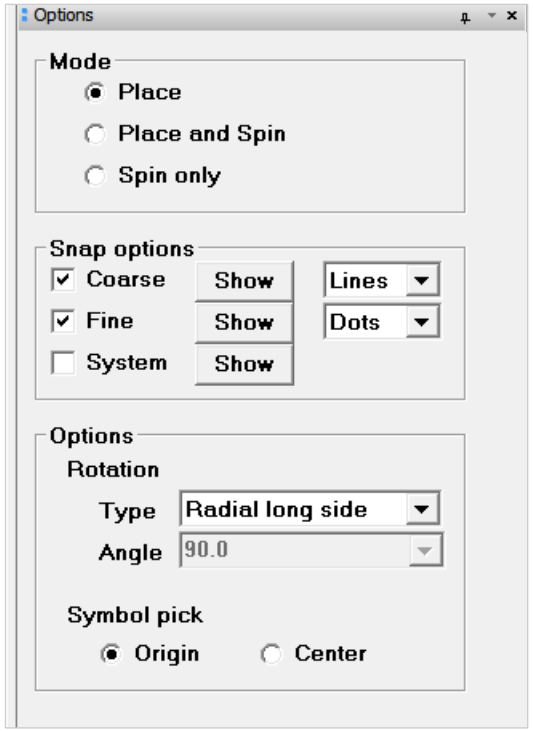




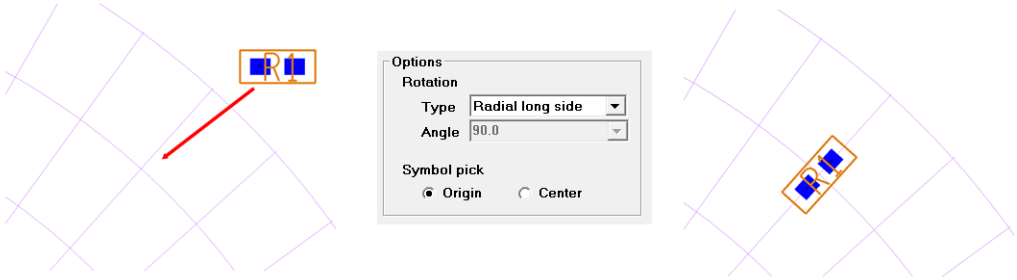


Polar Grid Utilities

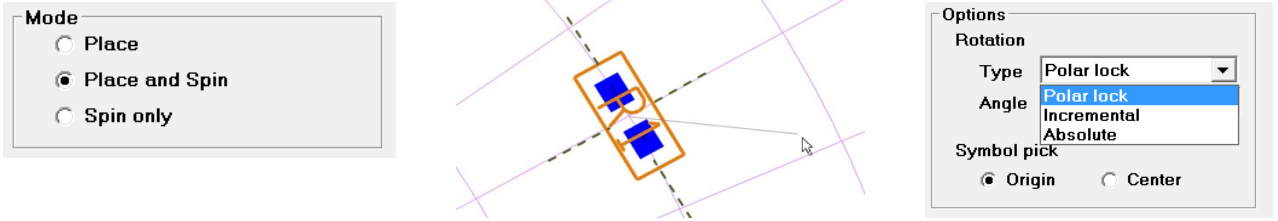
- **Polar placement**
  - Special mode for placing component in circular or radial fashion
  - Snap to fine or coarse grid
  - Various alignment and rotation capabilities
  - Spinning on polar grid basis (e.g. Polar lock)



Place mode

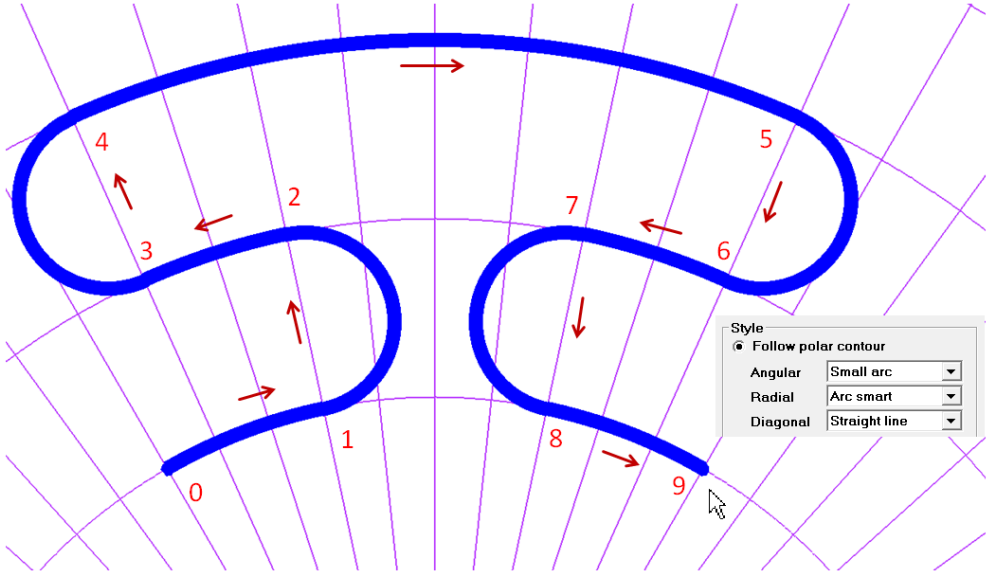


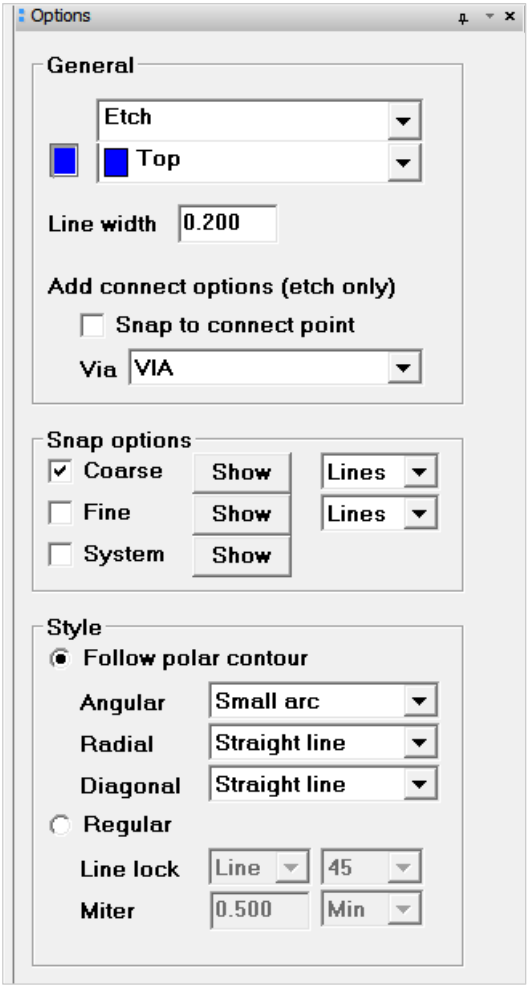
Place and Spin mode



Polar Grid Utilities

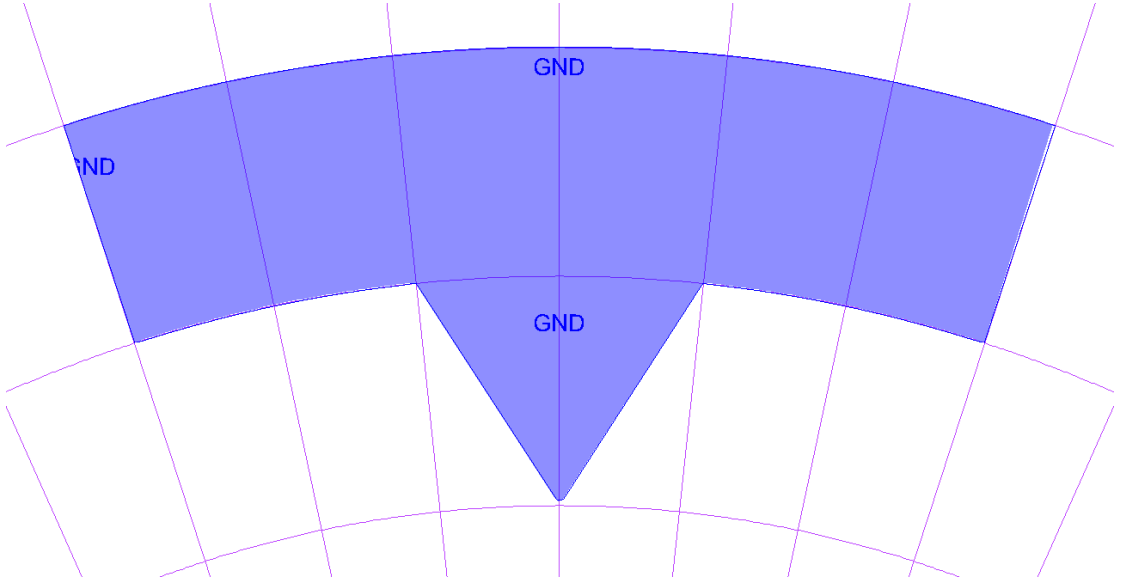
- **Polar routing**
  - Special mode for drafting or routing in a circular or radial fashion
  - Snap to fine or coarse grid
  - Ability to follow radial and angular contour
  - Alternate path options (e.g. **Arc smart**)

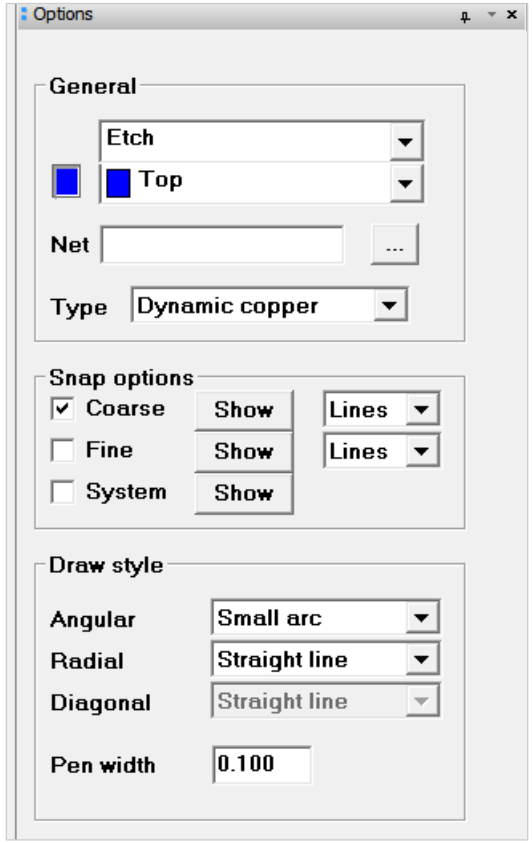




Polar Grid Utilities

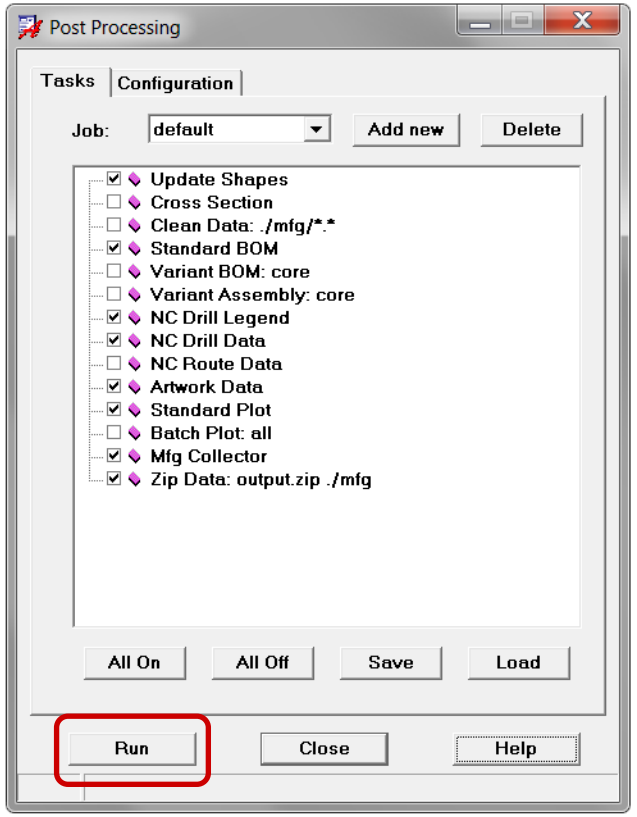
- **Polar shape and void editing**
  - Special mode for creating shapes and voids in a polar grid
  - Snap to fine or coarse grid
  - Ability to follow radial and angular contour
  - Alternate path options (e.g. **Arc smart**)





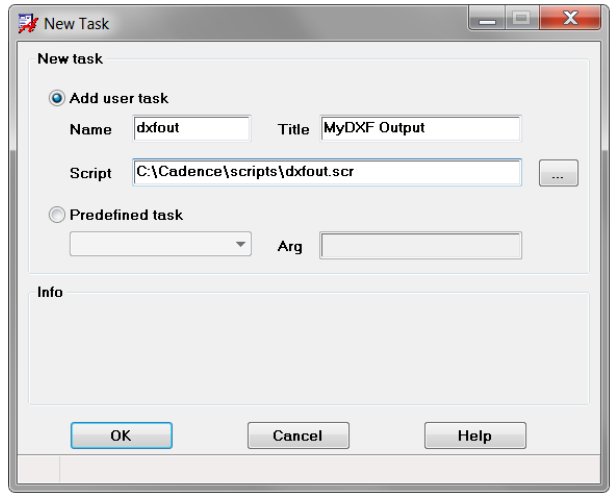
Post Processing

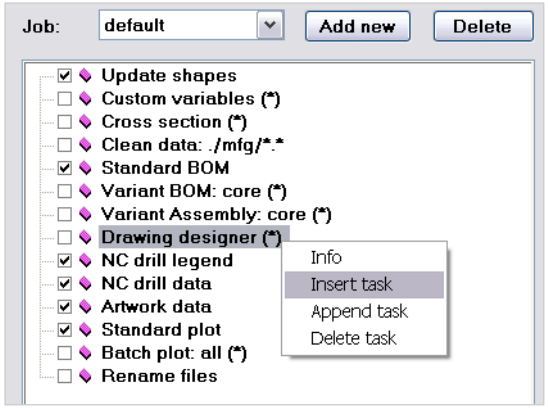
- Central cockpit from which manufacturing output can be configured and generated
- **Hit Button** solution many users are asking for
- Tasks can be enabled / disabled, added and removed individually
  - Standard functions from PCB Editor
  - Skill procedures (e.g. FloWare)
  - User defined scripts
- Jobs can be defined which contain a collection of tasks
- Configuration stored in database
- Import and Export capabilities for the purpose of standardization

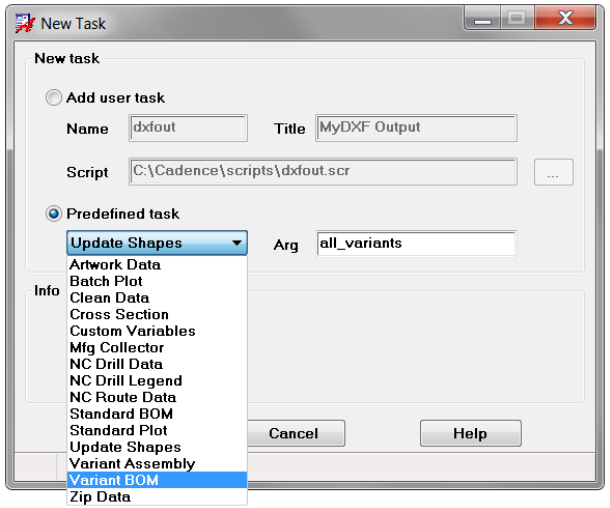


Post Processing

- Context menu provides task editing
  - Info
  - Tasks can be added (appended or inserted)
    - User tasks
    - Predefined tasks including arguments
  - Tasks can be removed if not needed at all

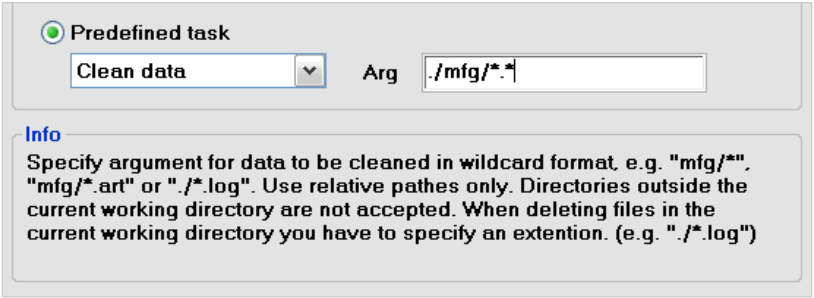


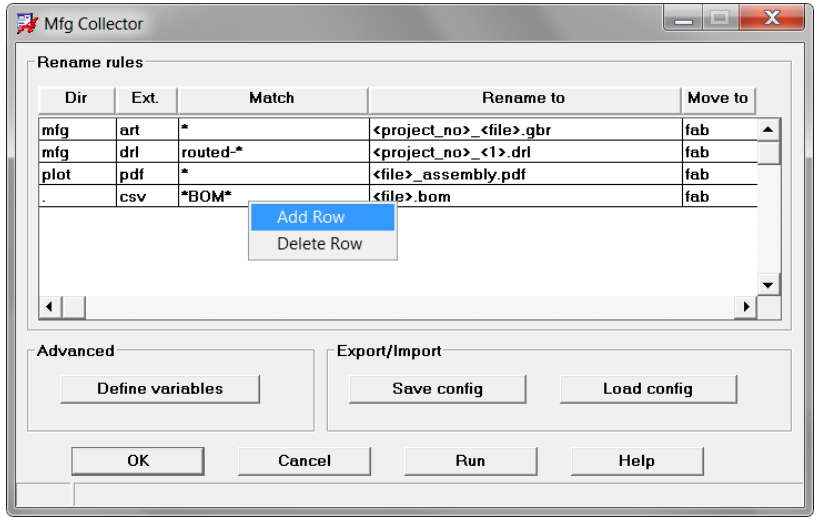




Post Processing

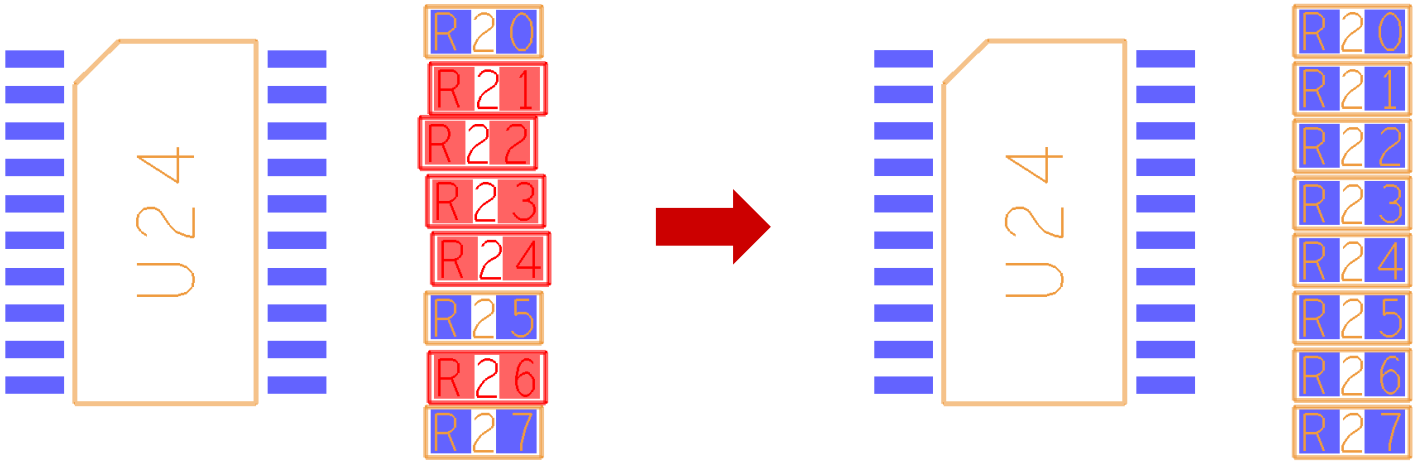
- Additional built-in functions
  - **Clean Data**
    Performs file delete operations based on arguments provided including wildcards
  - **Standard BOM**
    Generates standard BOM in text and csv format
  - **Standard Plot**
    Plots all artwork film control records into one PDF file artwork.pdf
  - **Rename Files**
    Provides powerful automated file renaming mechanism (wildcards, variables and pattern tags) for PLM purposes

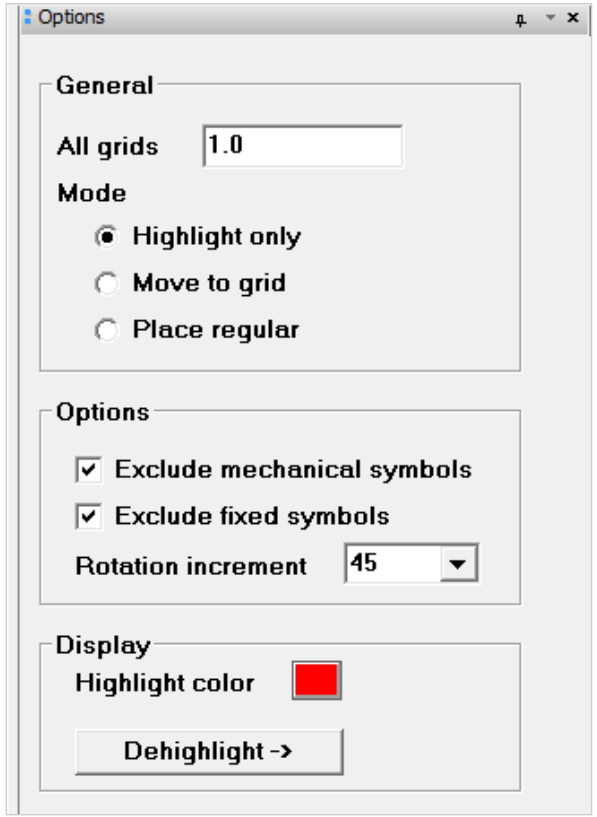




Push to Grid

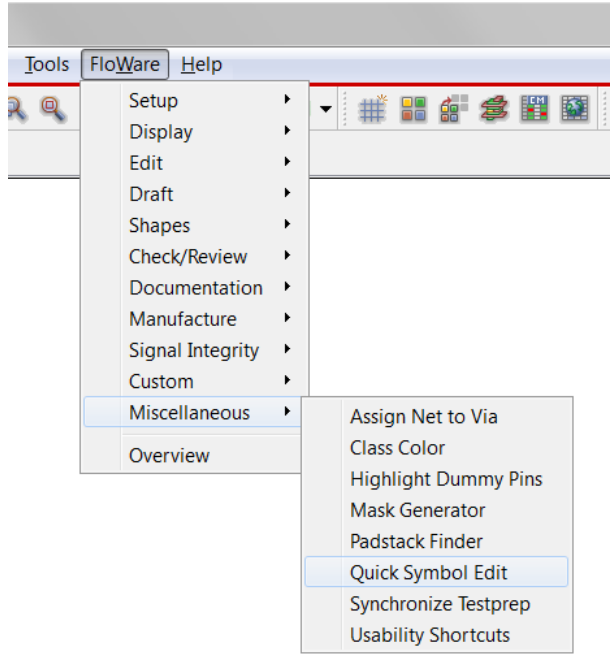
- Placement application featuring
  - Highlight off grid symbols
  - Option to move / push symbols to the nearest grid point
  - Regular placement mode for standard placement operations
    - Single and multiple selected symbols
    - Including mirror and spin support





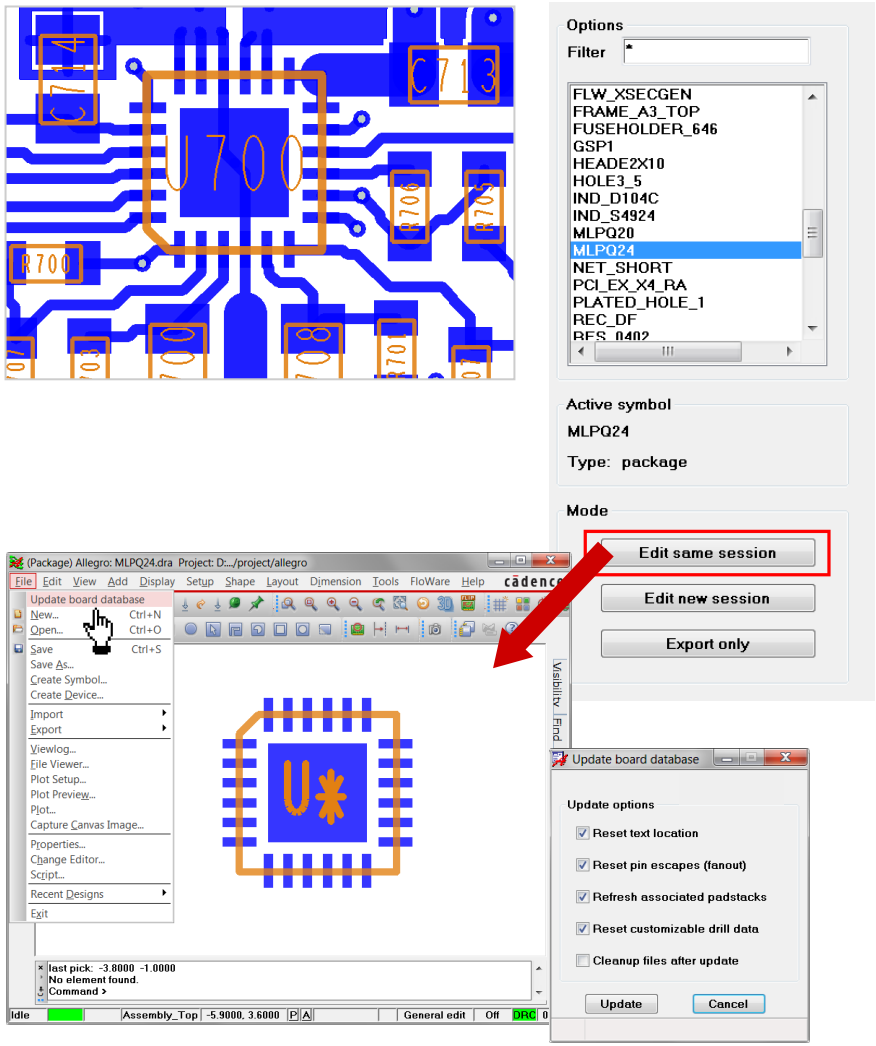
Quick Symbol Edit

- Opens symbol editor out of a layout database for viewing or editing purposes
- Three modes
  - **Edit same session**
    - Acts similar to **Tools > Modify Design Padstack** (next slide)
  - **Edit new session**
    - Launches a new session and open the symbol dra file
  - **Export only**
    - Only exports symbol data (dra, psm, pad, etc.) for the selected symbol to a specified directory



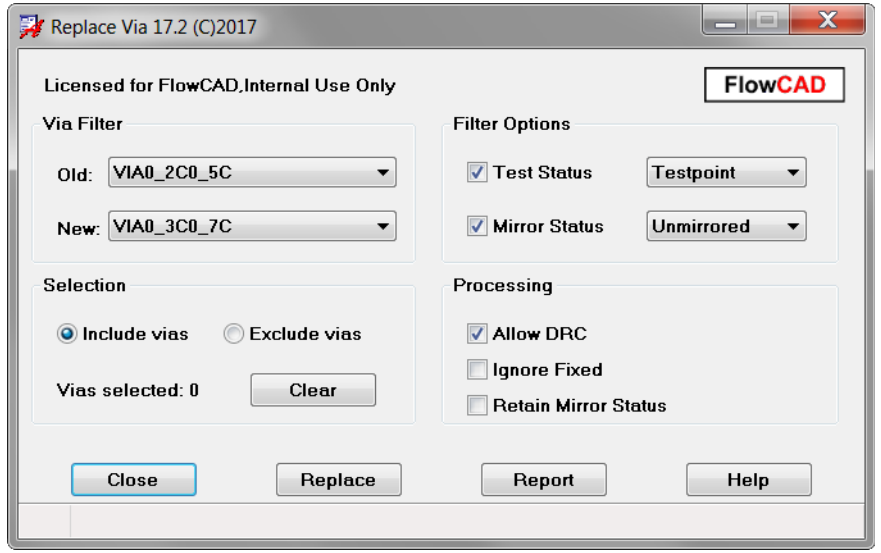
Quick Symbol Edit

- **Edit same session**
  - Seamless edit and update of a symbol definition in board context
  - Acts like Tools > Modify Design Padstack
  - Steps:
    1. Launch **Quick Symbol Edit** in layout context
    2. Select a symbol
    3. Current database closes, symbol dra file will be opened
    4. Make your modifications
    5. Finally choose **File > Update board database**
    6. Specify update settings
    7. The layout database from which the command was launched opens again and the footprints will be updated



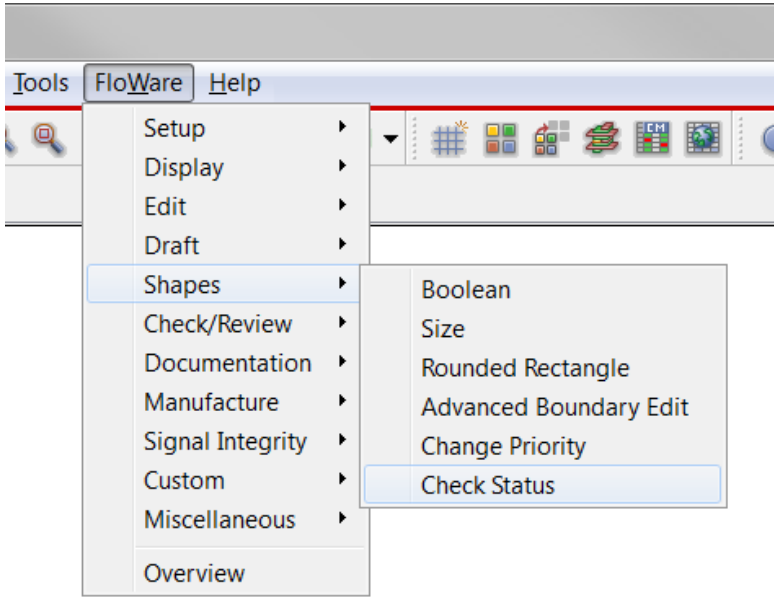
Replace Via

- More flexibility while replacing vias in the design
  - Specify padstack names
  - Restrict replacement to selection area
  - Include and exclude vias from the specified area through interactive commands
  - Additional filter options, e.g. distinguish between
    - Vias with or without testpoint status
    - Mirrored or unmirrored vias
  - Processing options
    - Allow DRC
    - Ignore Fixed
    - Retain Mirror Status



Shape Utilities

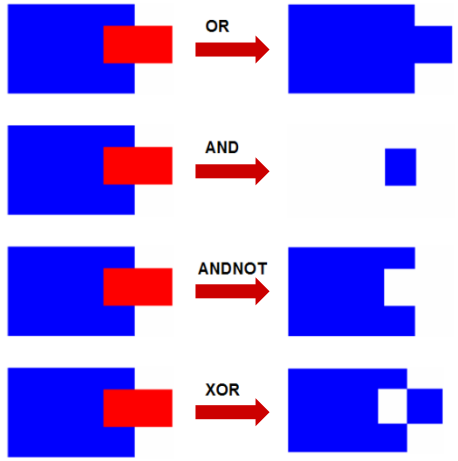
- Includes useful functions when editing shapes
  - Boolean operations
  - Size operations (Expand, Contract, Size)
  - Rectangular shapes with rounded corners
  - Advanced boundary edit functions
    - Stretch
    - Cut
    - Round off vertices
    - Change round off radius
    - Modify individual arc parameters
  - Modify shape priorities
  - Check status

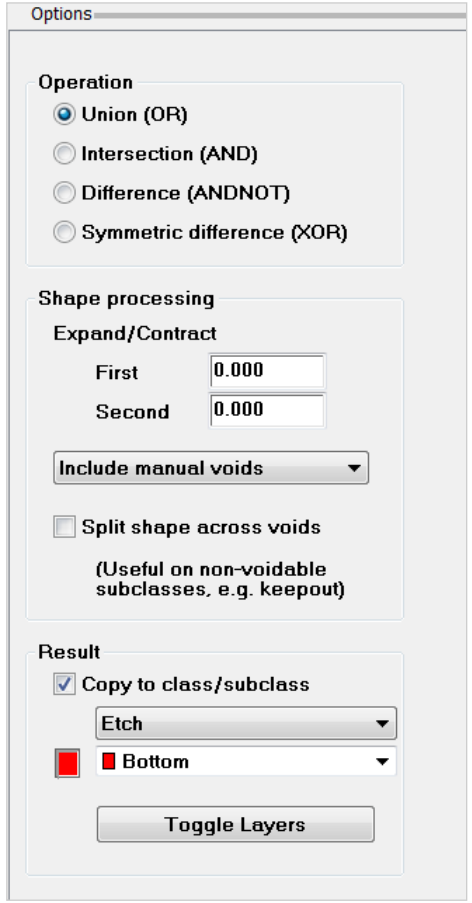


Shape Utilities – Boolean Operations

- Features
  - OR, AND, ANDNOT, XOR
  - Supports shape–shape operations as well as shape–line and shape–text operations
  - Shape attributes (shape type, fill style, net name etc.) are retained and applied to the resulting shape
  - Ability to split shapes across voids
  - Expand / contract capabilities
  - Useful for general editing and basic RF-applications

Basic operations



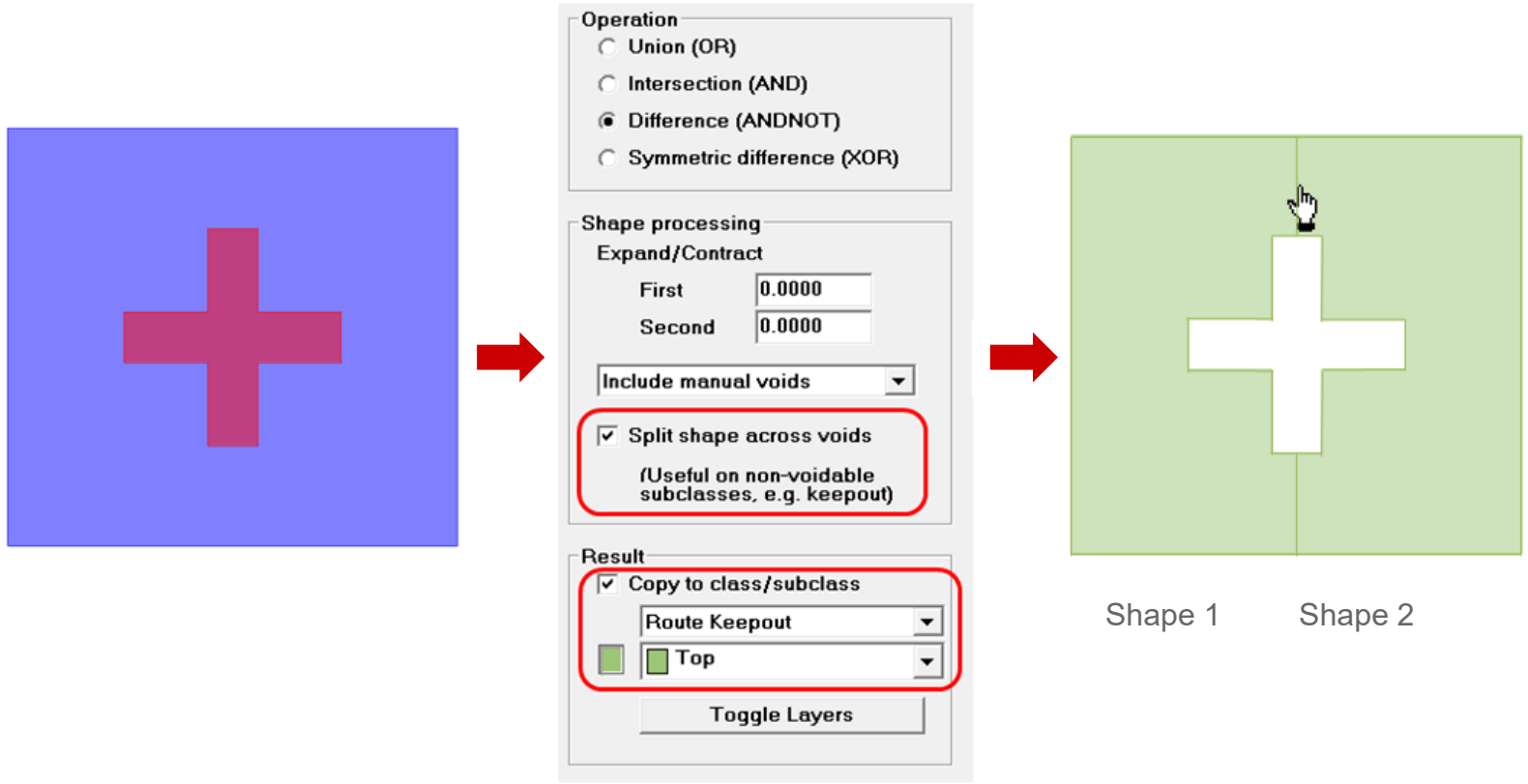


Etching negative texts into copper

Cutting a dynamic shape

Shape Utilities – Boolean Operations

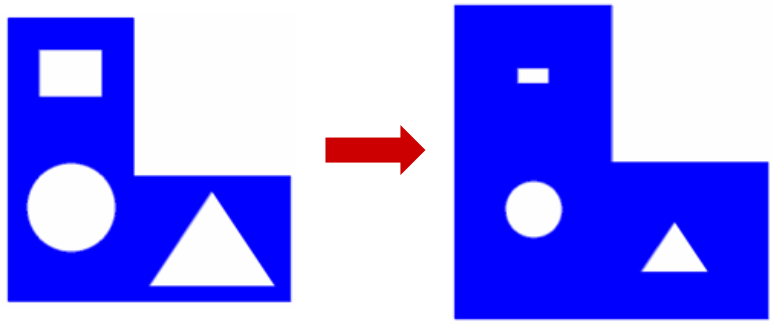
- Let's you also split shapes across voids
- Useful when working on non-voidable layers such as KEEPOUT, NO_PROBE etc.

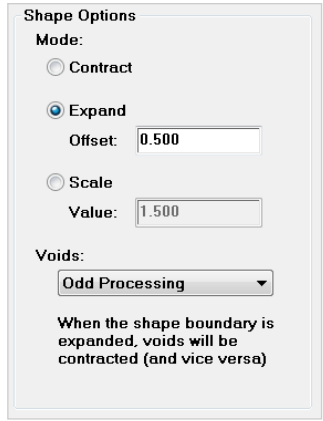


Shape Utilities – Size Operations

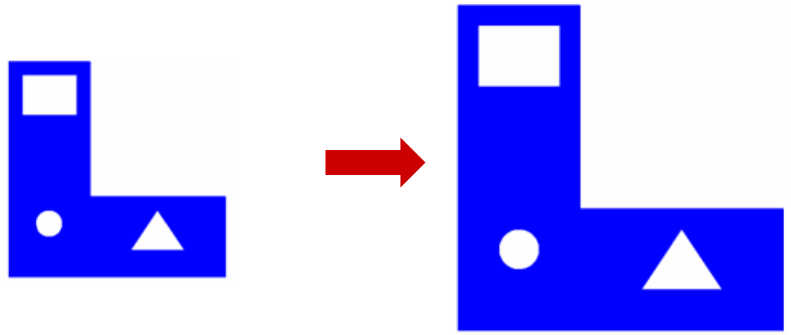
- Expand / Contract similar to **Edit > ZCopy** but directly acts on selected shape. No copies remain. Additional options for void handling

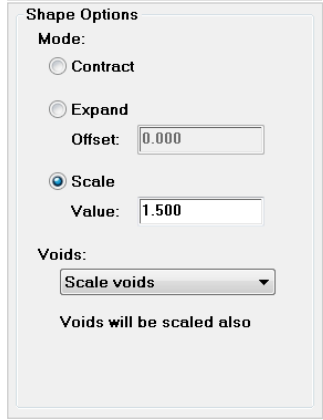
Expanding a shape

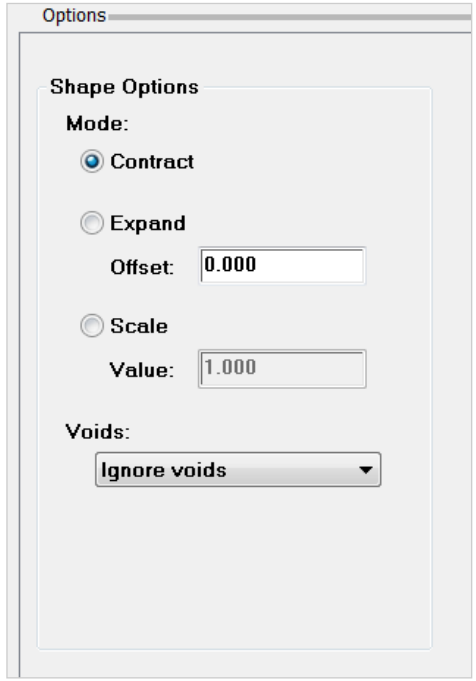




Scaling a shape



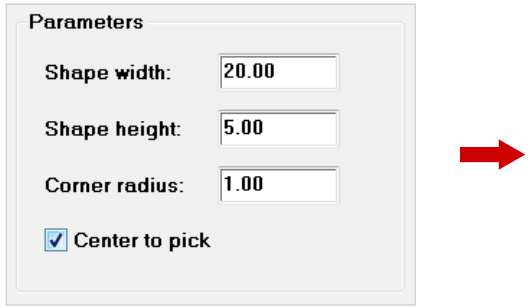




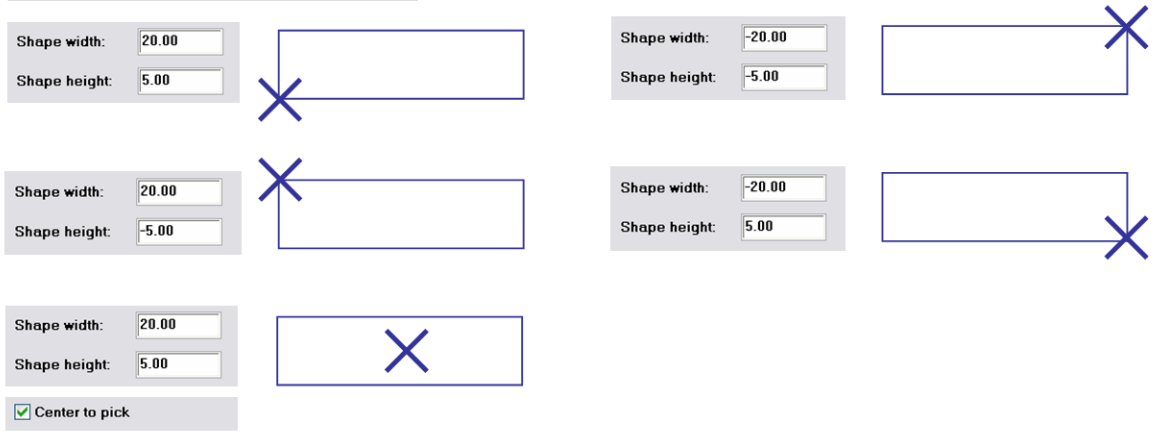
Shape Utilities – Rounded Rectangular Shapes

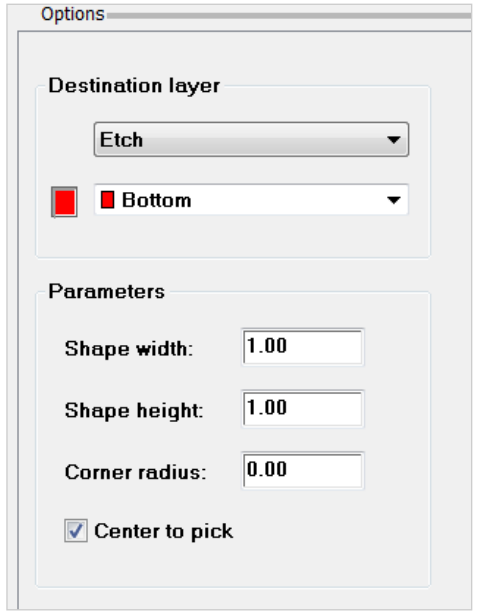
- Useful when defining pad shapes
- Size can be specified exactly
- Reference point can be chosen by using negative values for width and height

Basic operation



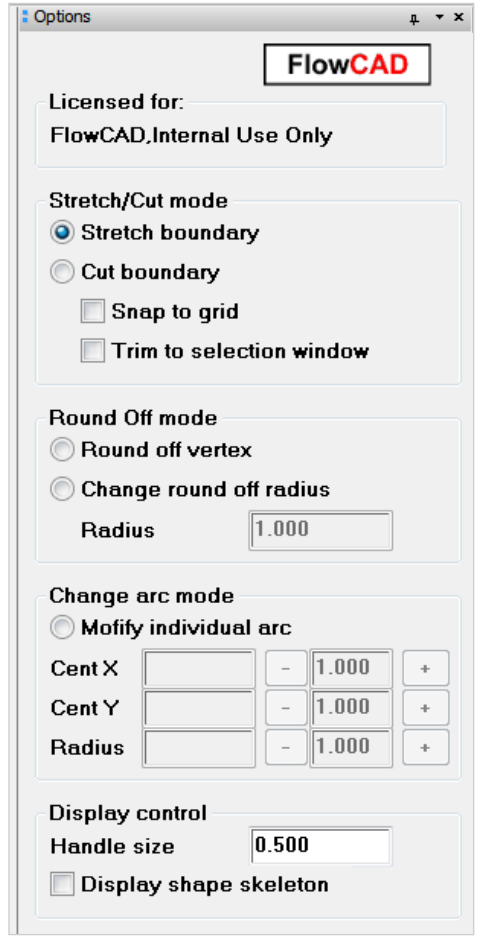
Specify shape origin





Shape Utilities – Advanced Boundary Edit

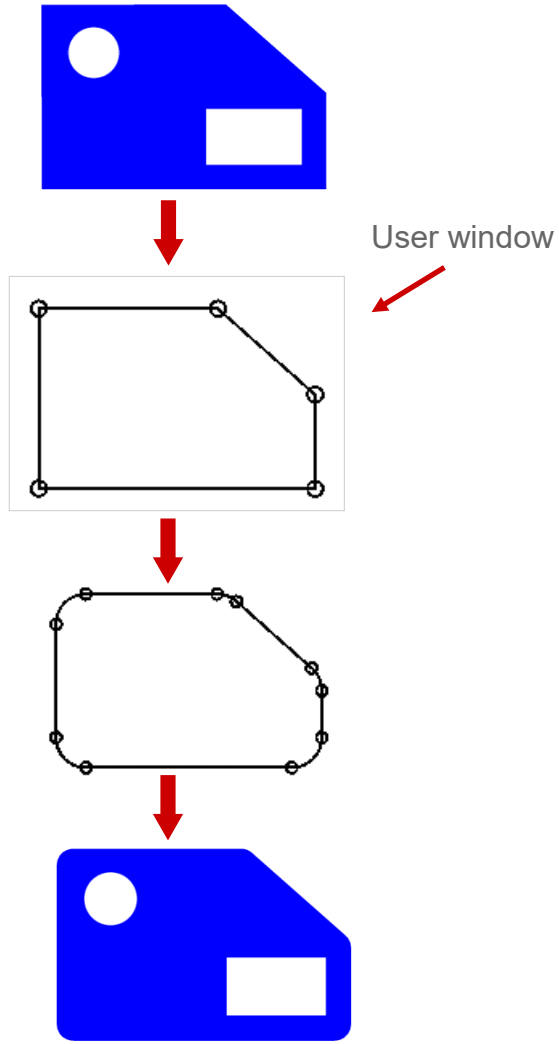
- Supports several modes
  - Stretching of shapes
  - Cutting of shapes
  - Rounding off vertices
  - Changing existing round off radius
  - Modifying individual arc segments of a shape
- All modes within one command
  - Including Oops support
- Additional features
  - Can also edit voids (Find Filter)
  - Supports single pick as well as window selection (several vertices)
  - Snap to grid, Trim to selection window
  - Display control (e.g. handle size)



Shape Utilities – Advanced Boundary Edit

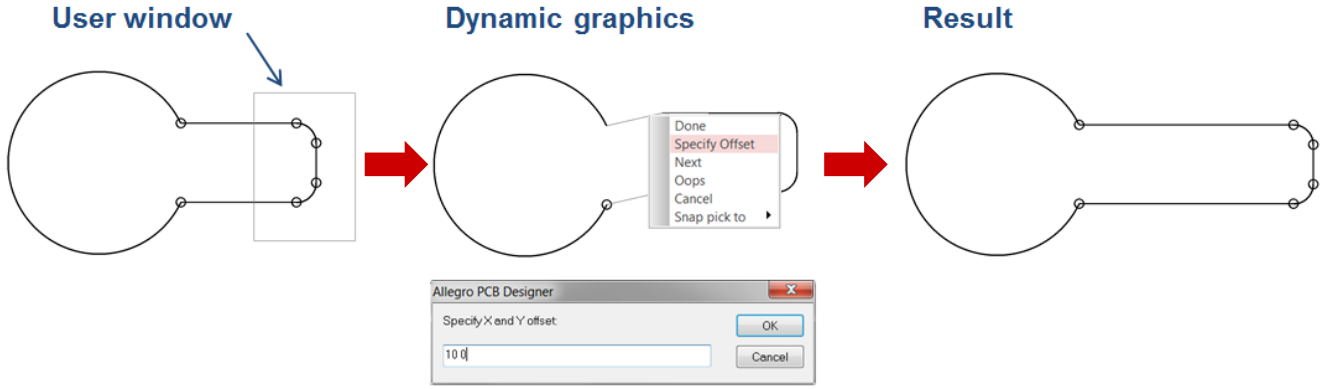
- Use model
  1. Select the shape or void to be modified
  2. Select an action, e.g. **Round off vertex**

  3. Pick a vertex or drag a window to select the vertices
  4. Switch to other modes if necessary and continue
  5. RMB > Done

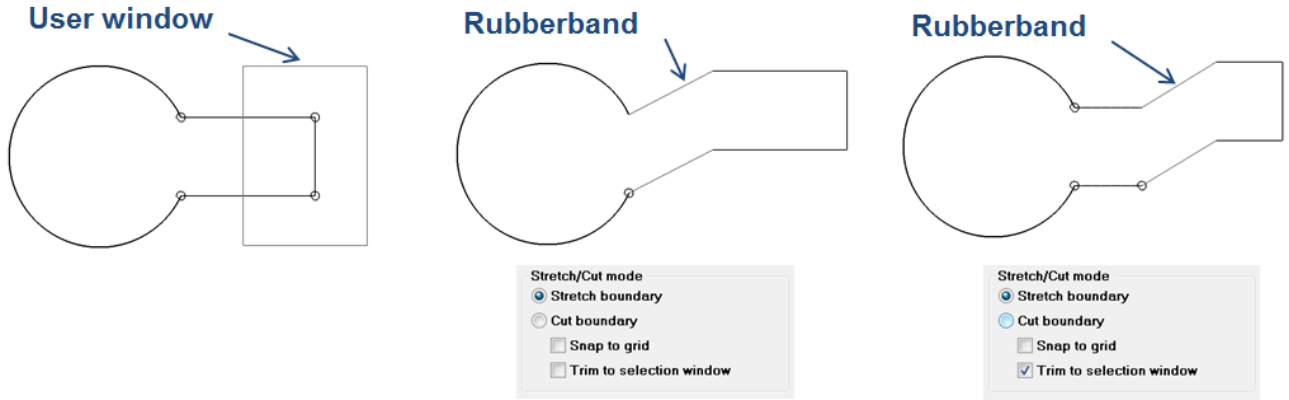


Shape Utilities – Advanced Boundary Edit

- Stretching of shapes
  - Specify offset if accurate stretch distance is needed

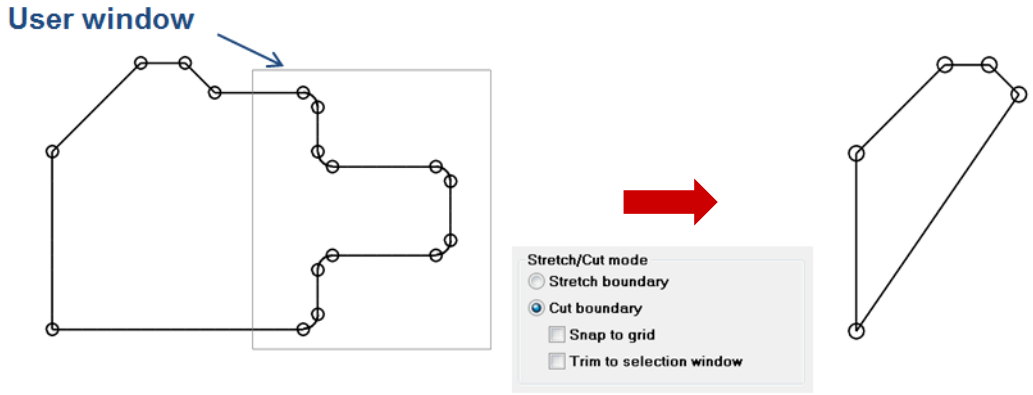


  - Trim to selection window let's you control stretch point origin

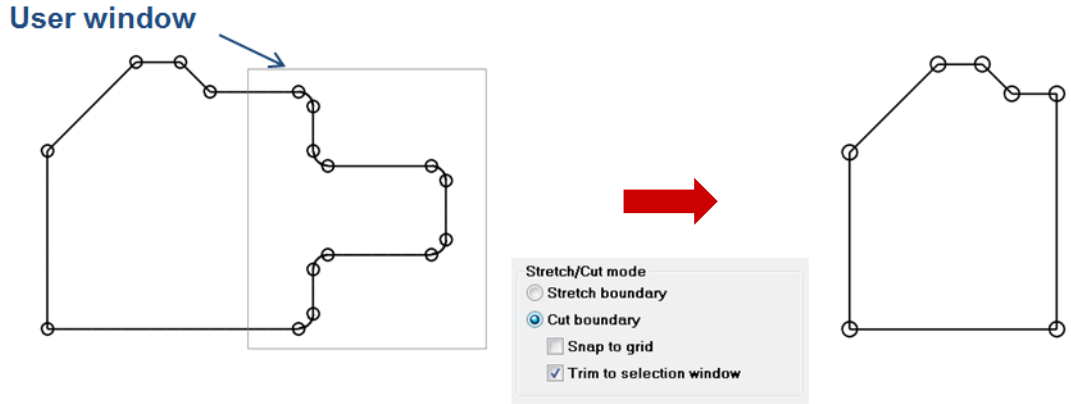


Shape Utilities – Advanced Boundary Edit

- Cutting of shapes
  - Adjacent segments of selected vertices will be deleted

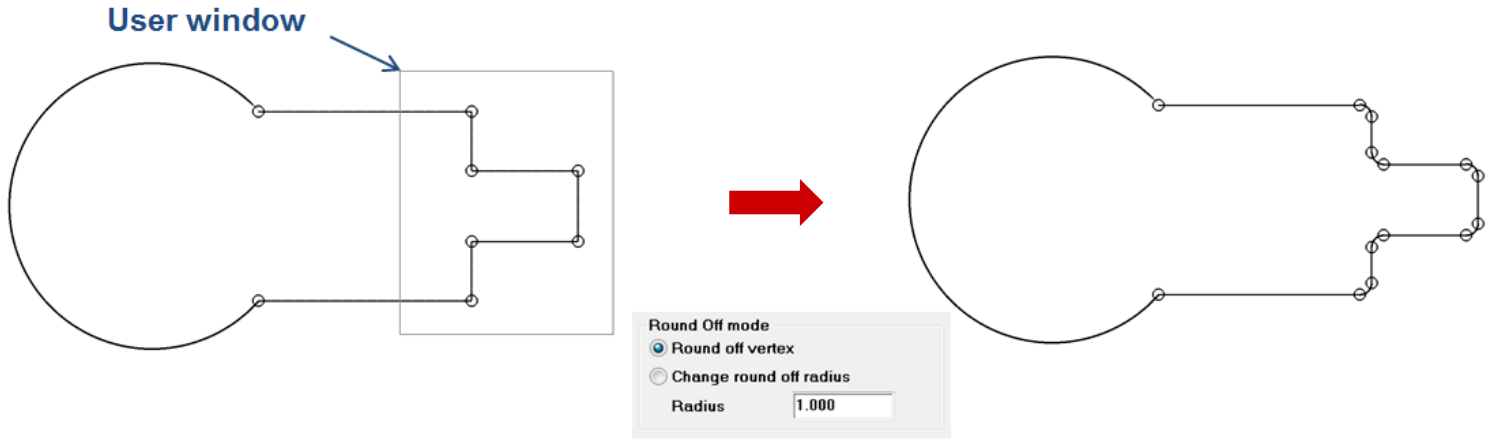


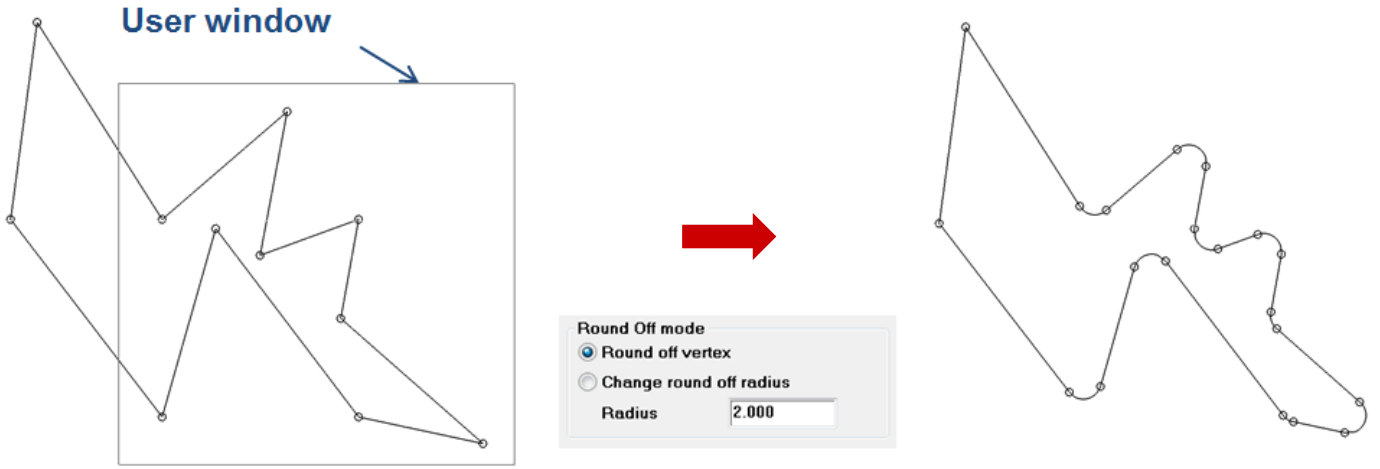
  - Trim to selection window simply cuts at the window boundary



Shape Utilities – Advanced Boundary Edit

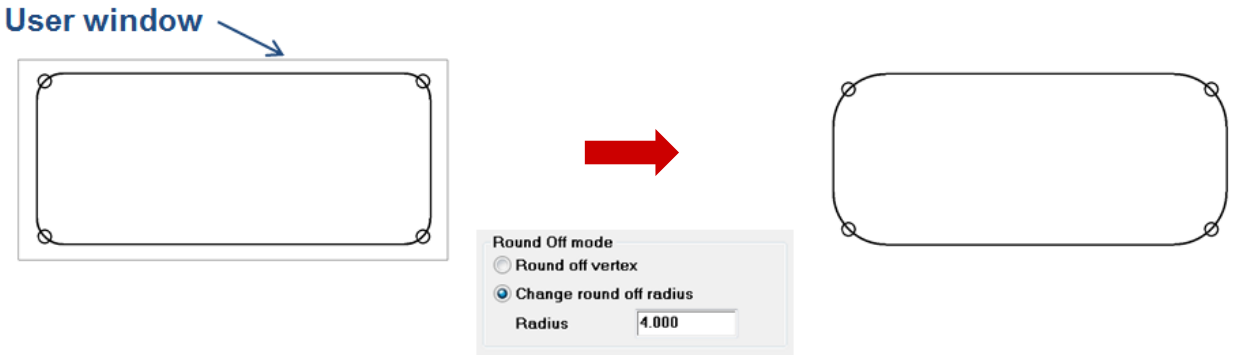
- Round off vertex



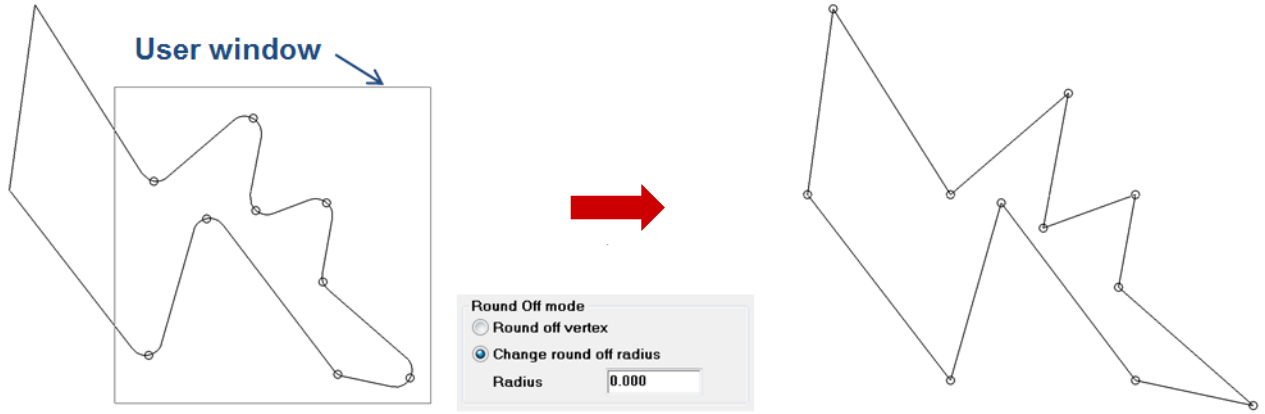


Shape Utilities – Advanced Boundary Edit

- Change round off radius
  - Let's you change existing rounded off corners

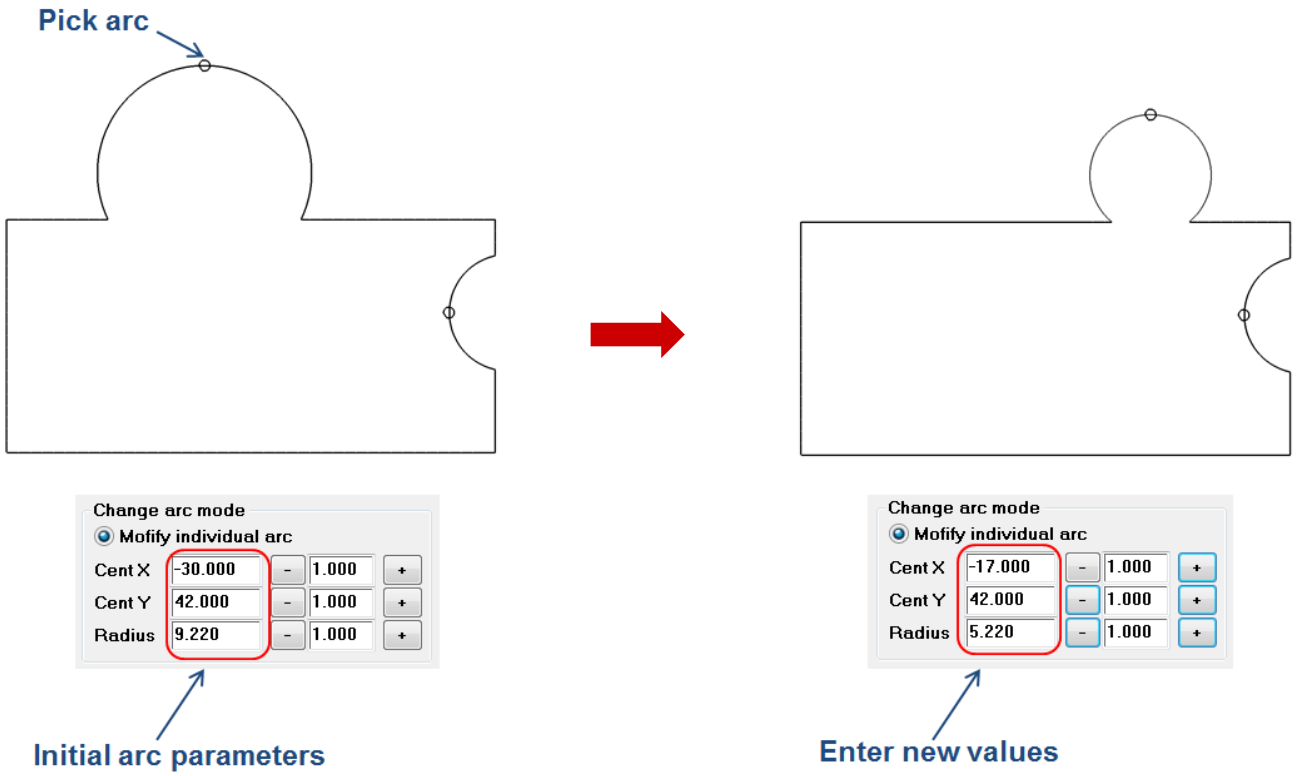


  - Can also restore original vertices by specifying a radius of 0.0



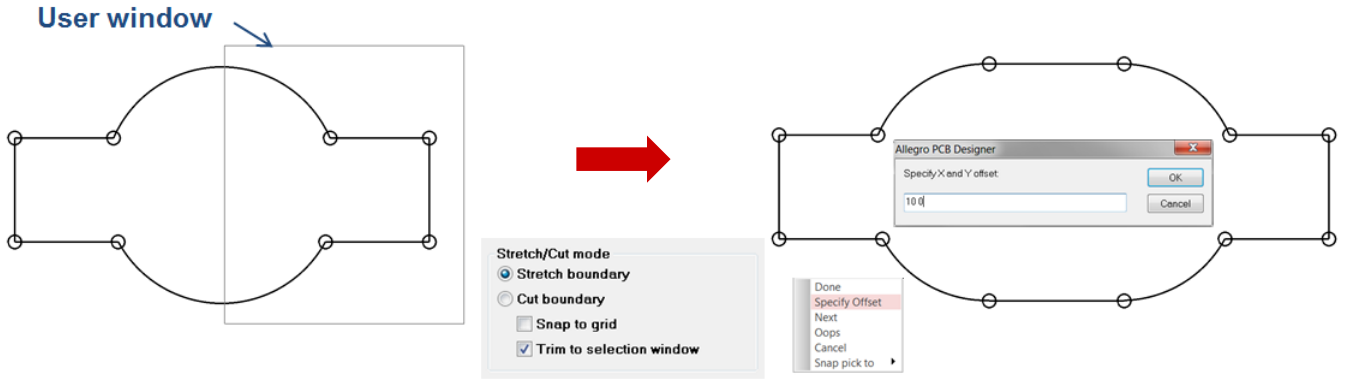
Shape Utilities – Advanced Boundary Edit

- Change arc mode
  - Parameters of existing arcs can be changed in Options panel. End points of adjacent segments will be adjusted automatically. Tuning possible by using +/- buttons

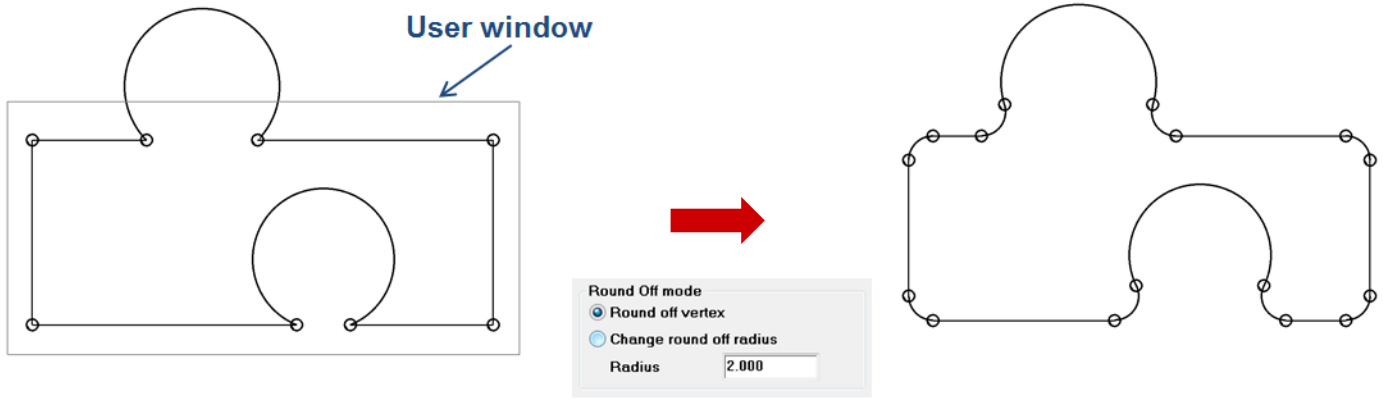


Shape Utilities – Advanced Boundary Edit

- Other highlights
  - Stretch / Cut on arc segments in conjunction with Trim option

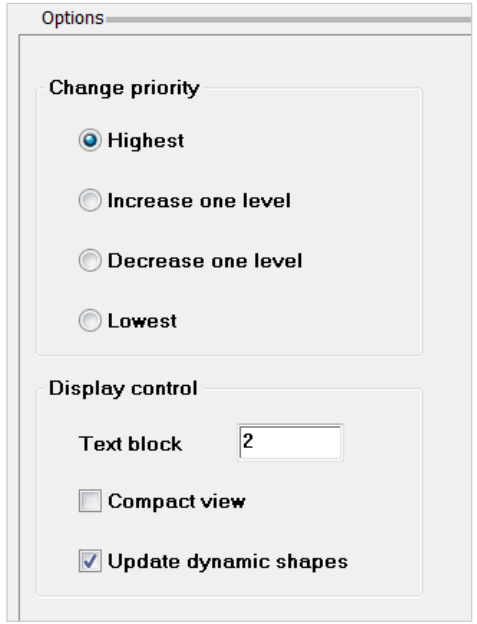


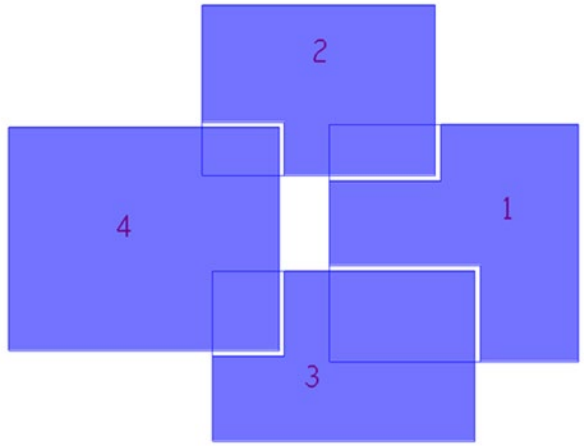
  - Round Off with adjacent arc segments



Shape Utilities – Priority

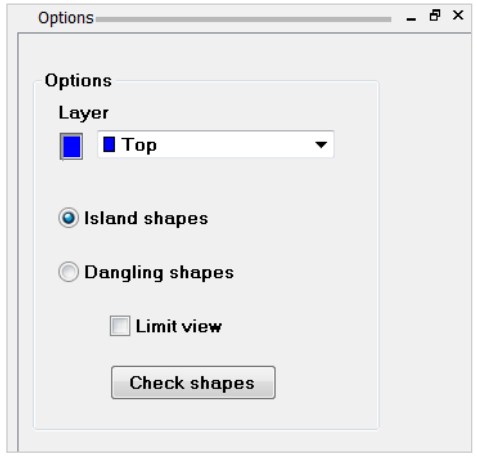
- Interactive application to modify the priority of a dynamic shape
- Use model
  - Select shapes by subsequent picks
  - Choose **RMB > Complete selection** to enter priority edit mode
  - Use one of the options and select a shape to modify the priority
    - Highest
    - Increase one level
    - Decrease one level
    - Lowest
- Priority numbers are displayed dynamically

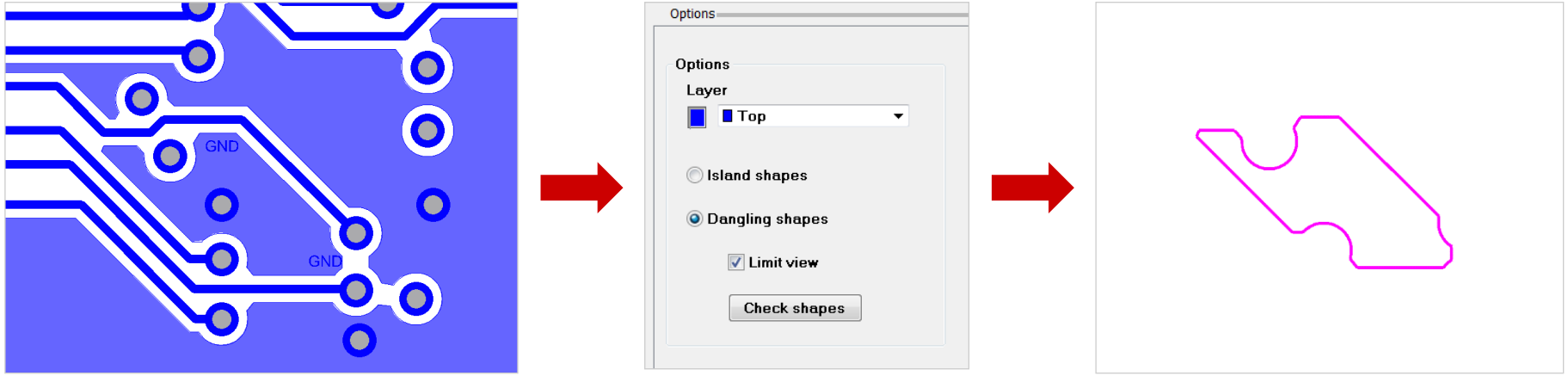




Shape Utilities – Check Status

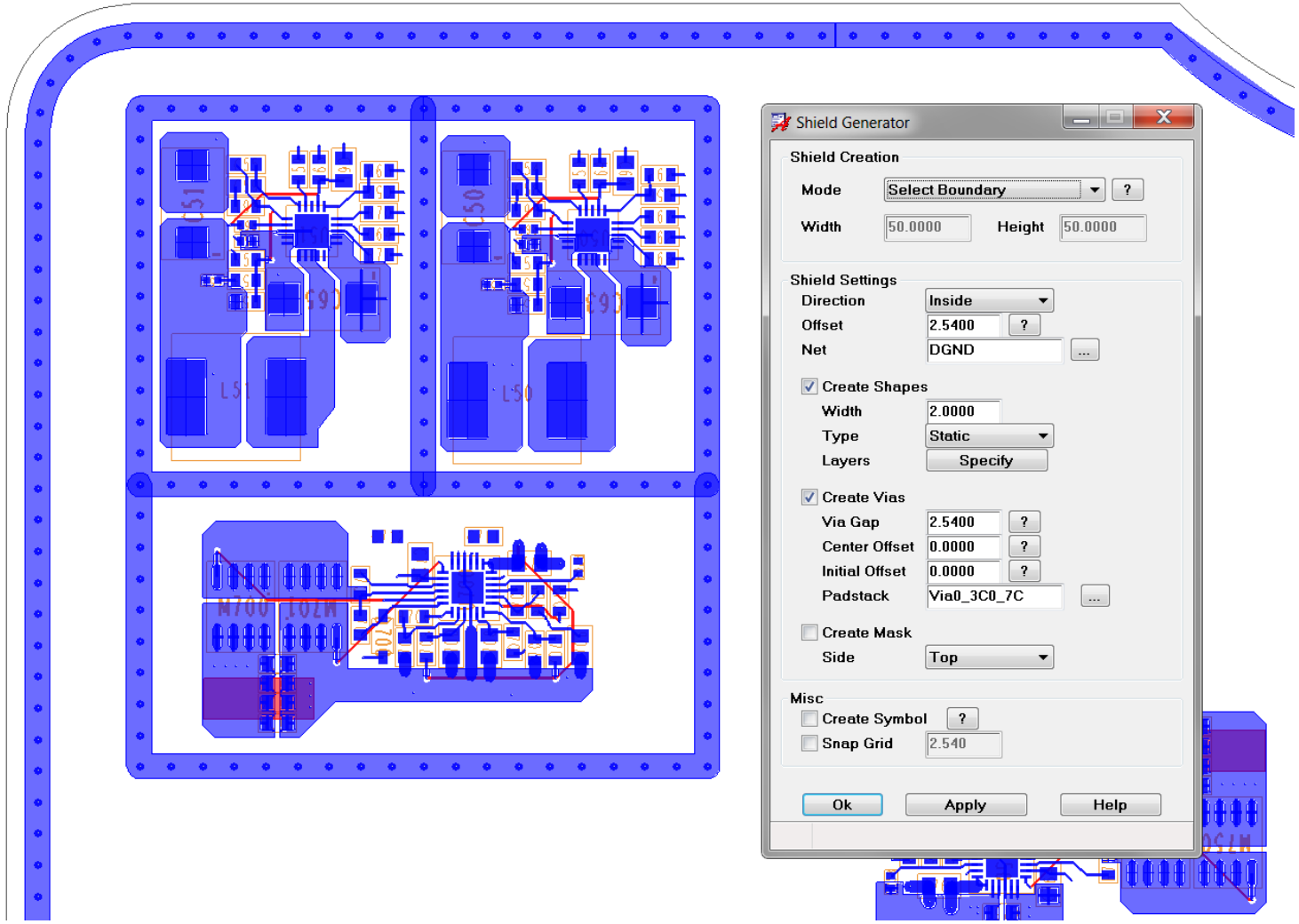
- Utility to check and highlight island and dangling shapes
  - Islands: 0 connections
  - Dangling shapes: Only 1 connection
- Such shapes can act as antennas and cause EMI issues





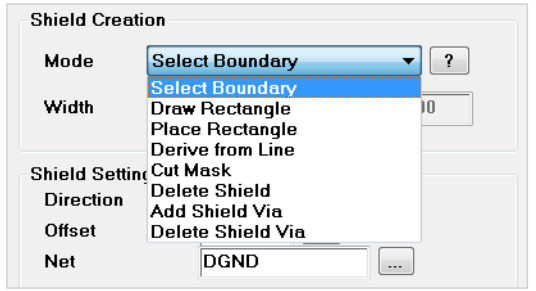
Shield Generator

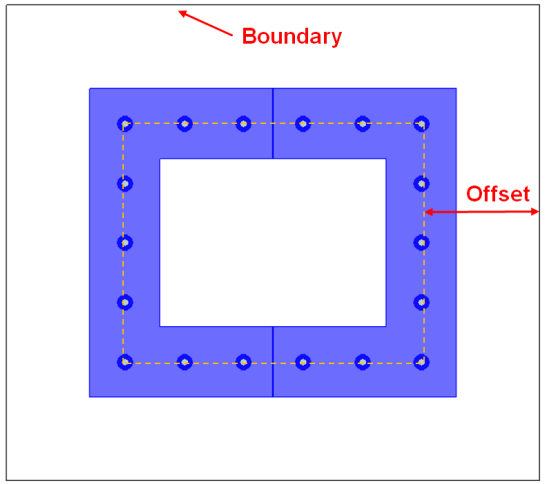
- Facilitates the generation of shape and via pattern for shielding purposes
- Includes shield rings along board outline (e.g. for ESD protection) as well as the generation of shield boxes for RF circuits

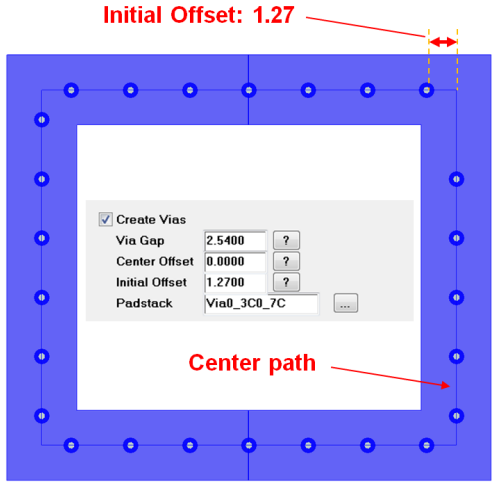


Shield Generator

- Different modes for shield generation
  - Select Boundary
  - Draw Rectangle
  - Place Rectangle
  - Derive from Line
  - …
- Shape parameters
  - Direction, offset, width, layers, …
- Via parameters
  - Via gap, offset inside ring, initial offset, …
- Mask generation and cutting capabilities for solder mask and paste mask
- Ability to create groups or symbols

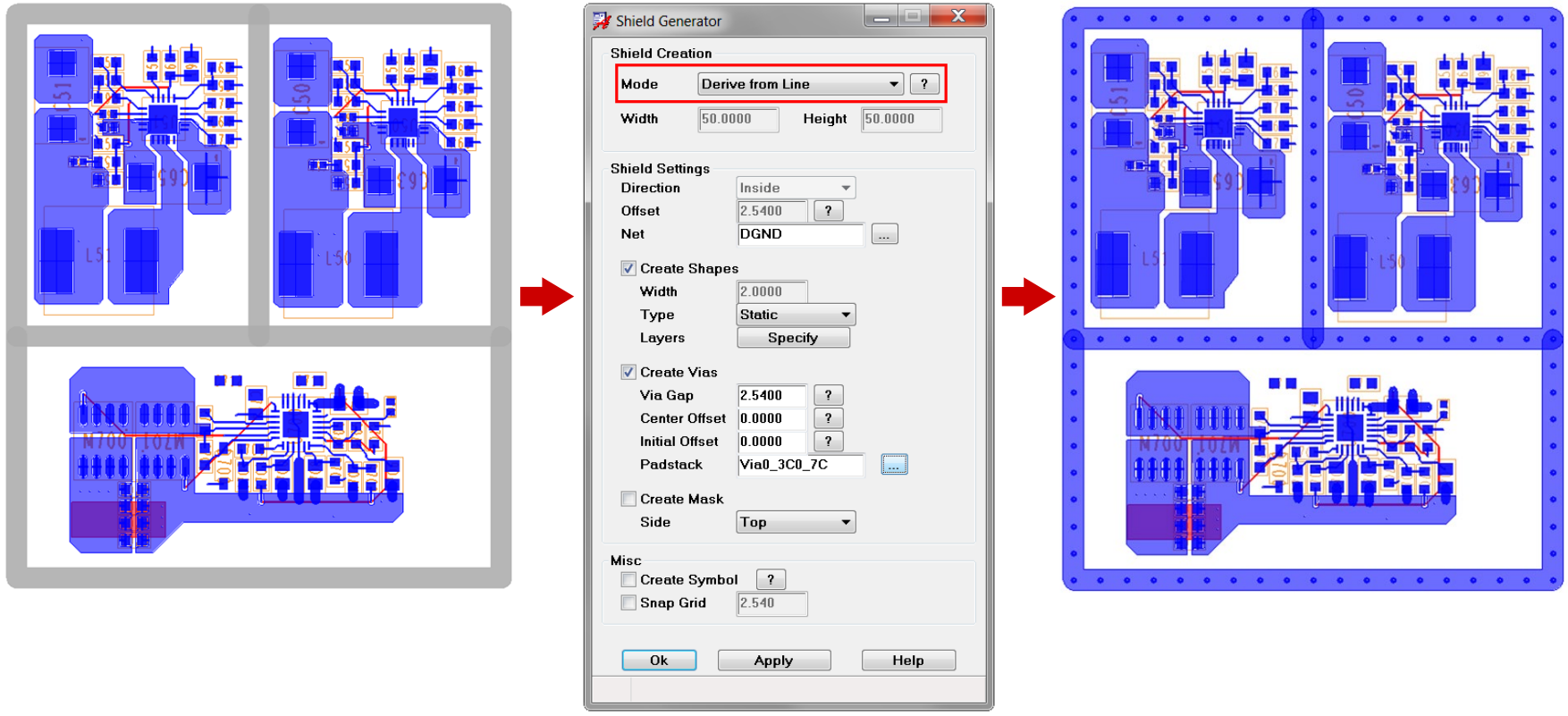






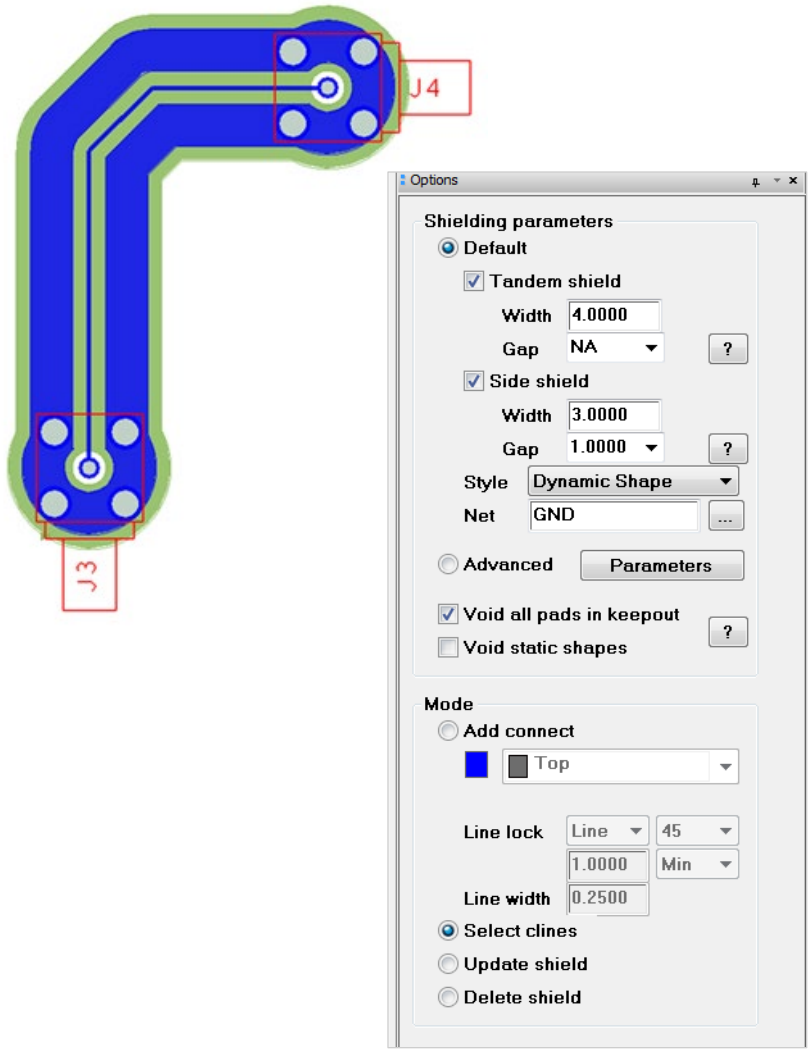
Shield Generator

- Derive from Line
  - This mode allows you to use construction lines as template and derive shield structure. Useful if shield box has partitions with arbitrary segmentations



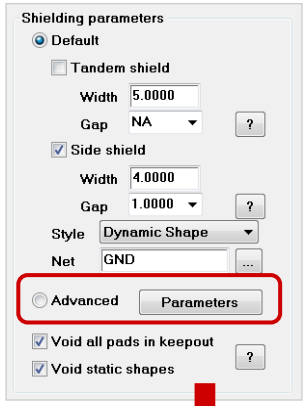
Shield Routing

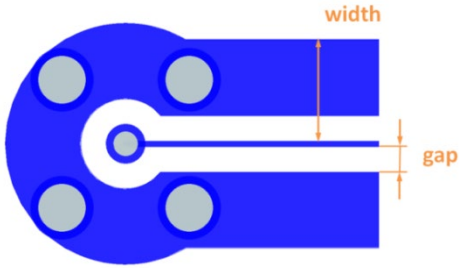
- Creates shield for critical signals in a semiautomatic way
  - Through interactive routing including dynamic preview
  - By selecting existing clines
- Support for side and tandem shields including parameters for gap and width and net name
- Support for dynamic or static shapes as well as route keepouts
- Advanced parameters can be used to control layers individually
- Parameters stored in database for each shield structure separately
  - Existing shields can be updated at any time without reentering information

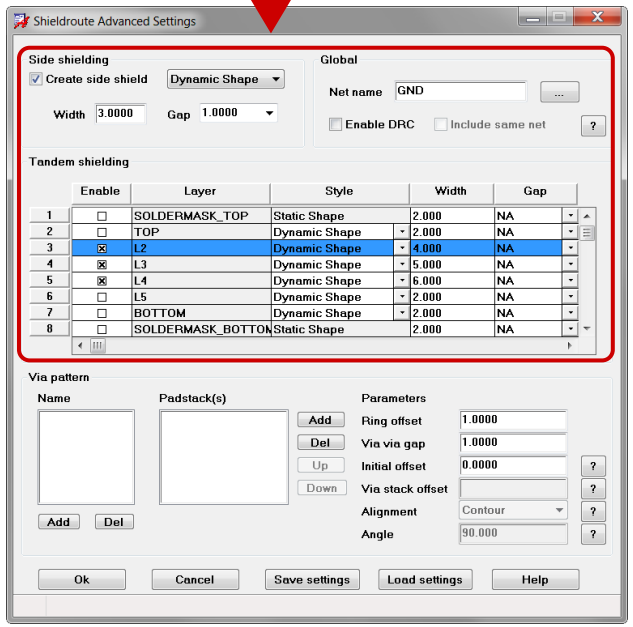


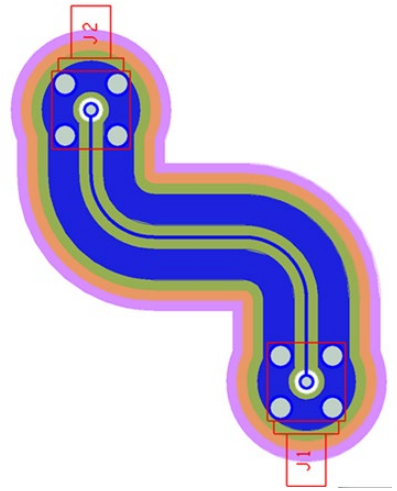
Shield Routing

- Default shield parameters
  - For regular applications
  - Side shielding (width and gap)
  - Tandem shielding (width) on adjacent layers only
  - Shape style and net name
- Advanced parameters
  - Can be used to define parameters for several layers individually
  - Export / Import settings for reuse purposes



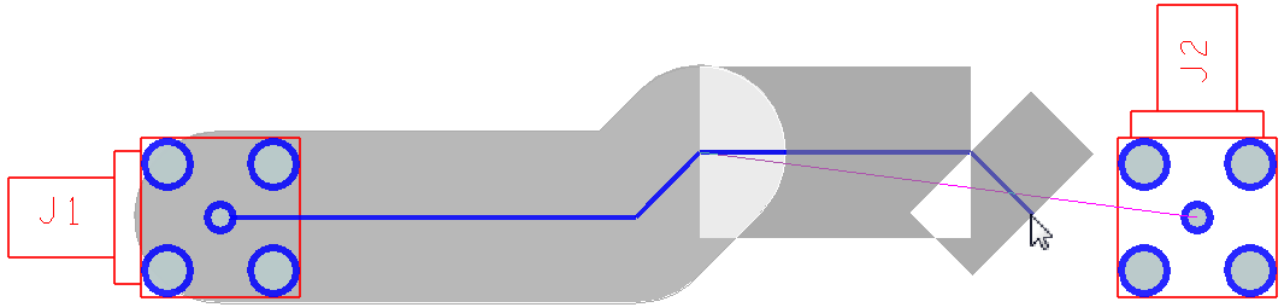




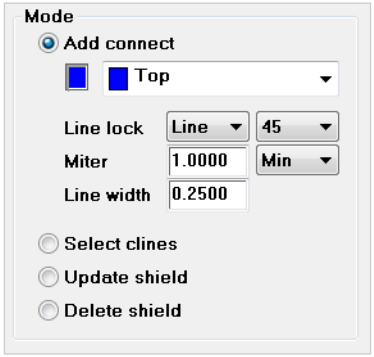


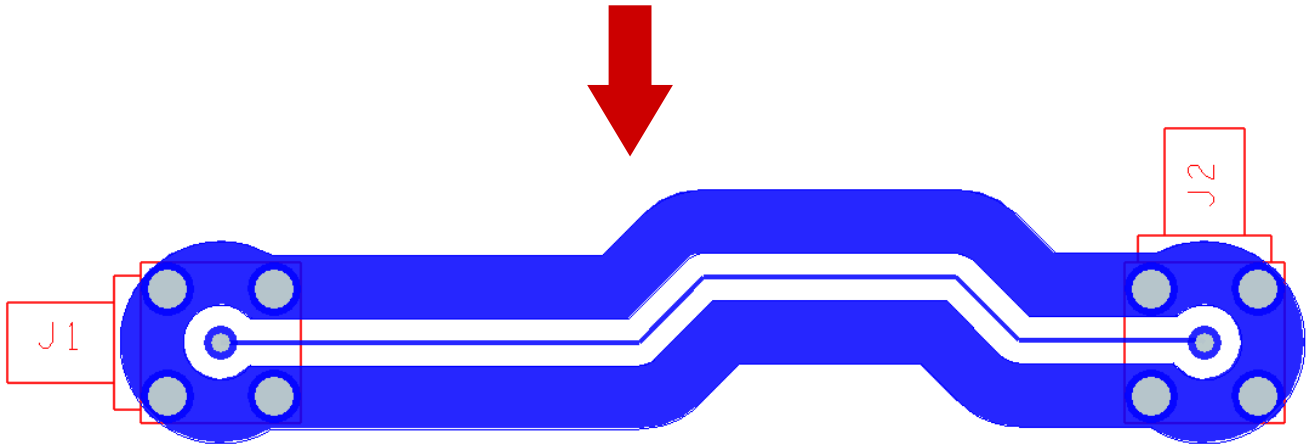
Shield Routing

- Routing shields interactively



Dynamic preview while routing with cursor

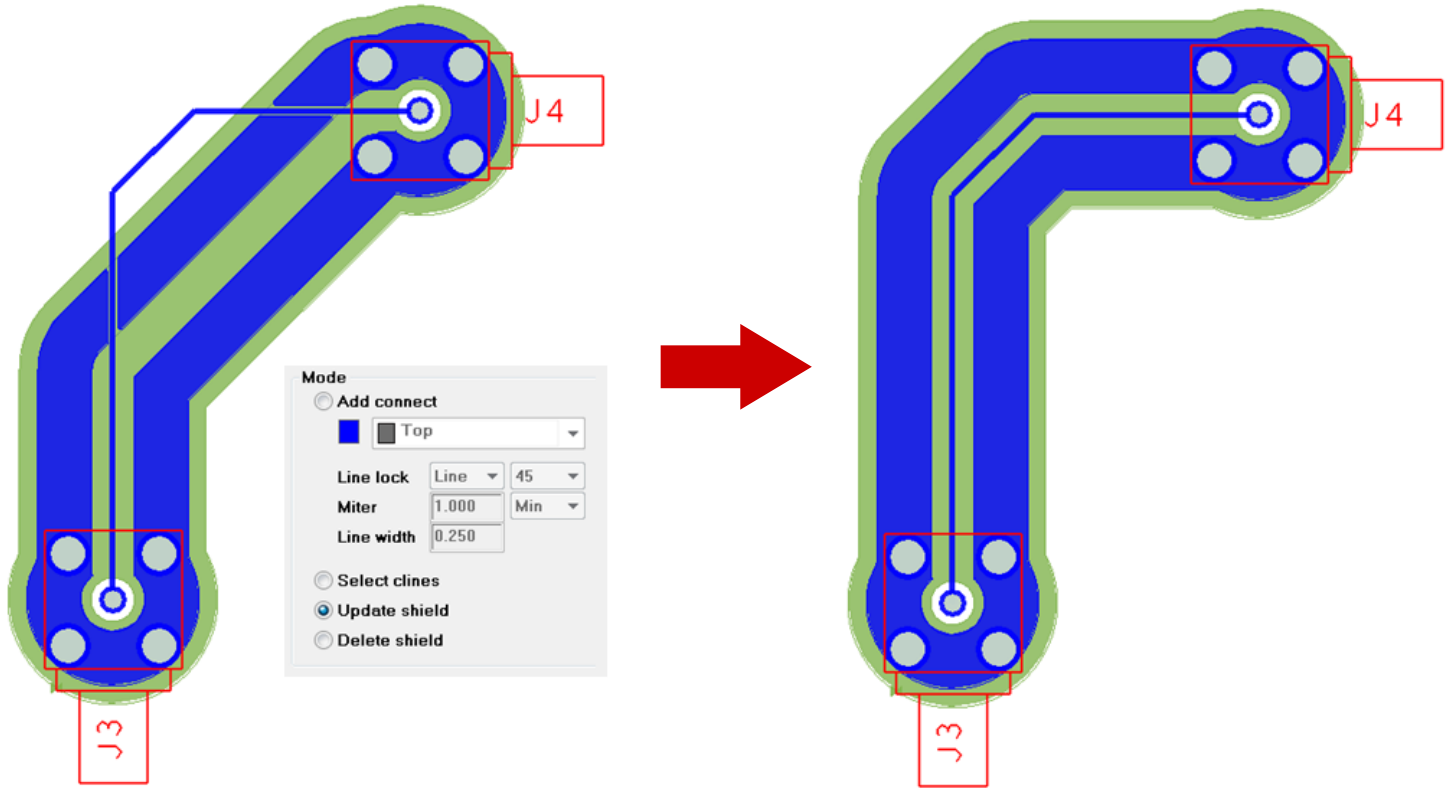




Final structure once snapping to pin or via

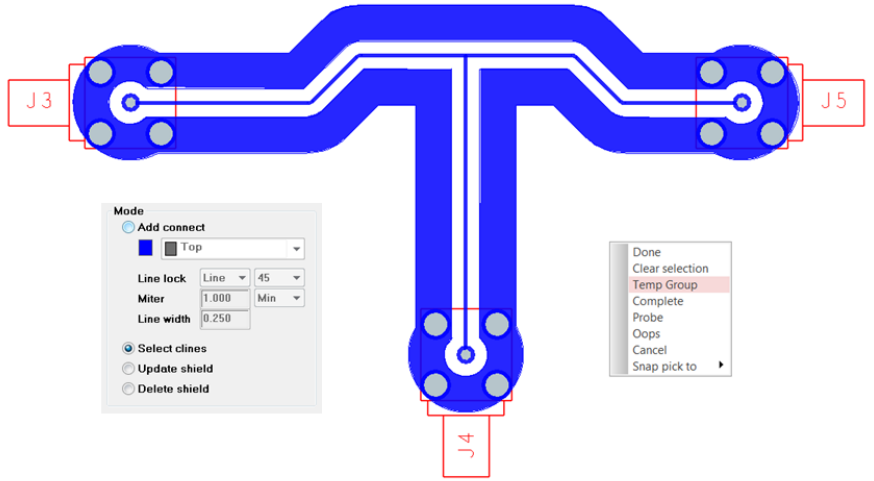
Shield Routing

- Updating existing shield structures due to routing modifications
  - Seamless update since parameters are stored in the database for each shield structure

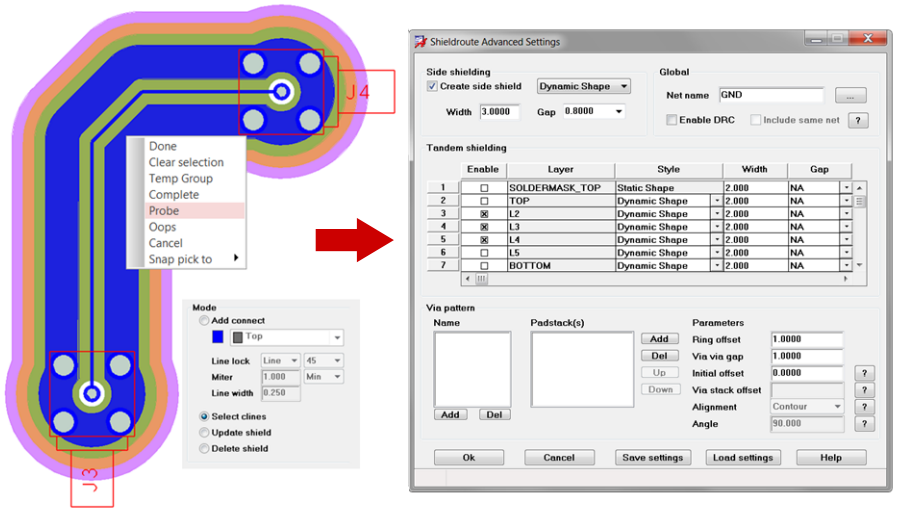


Shield Routing

- Creating combined shields for several contiguous clines
  - Through **Temp Group** command

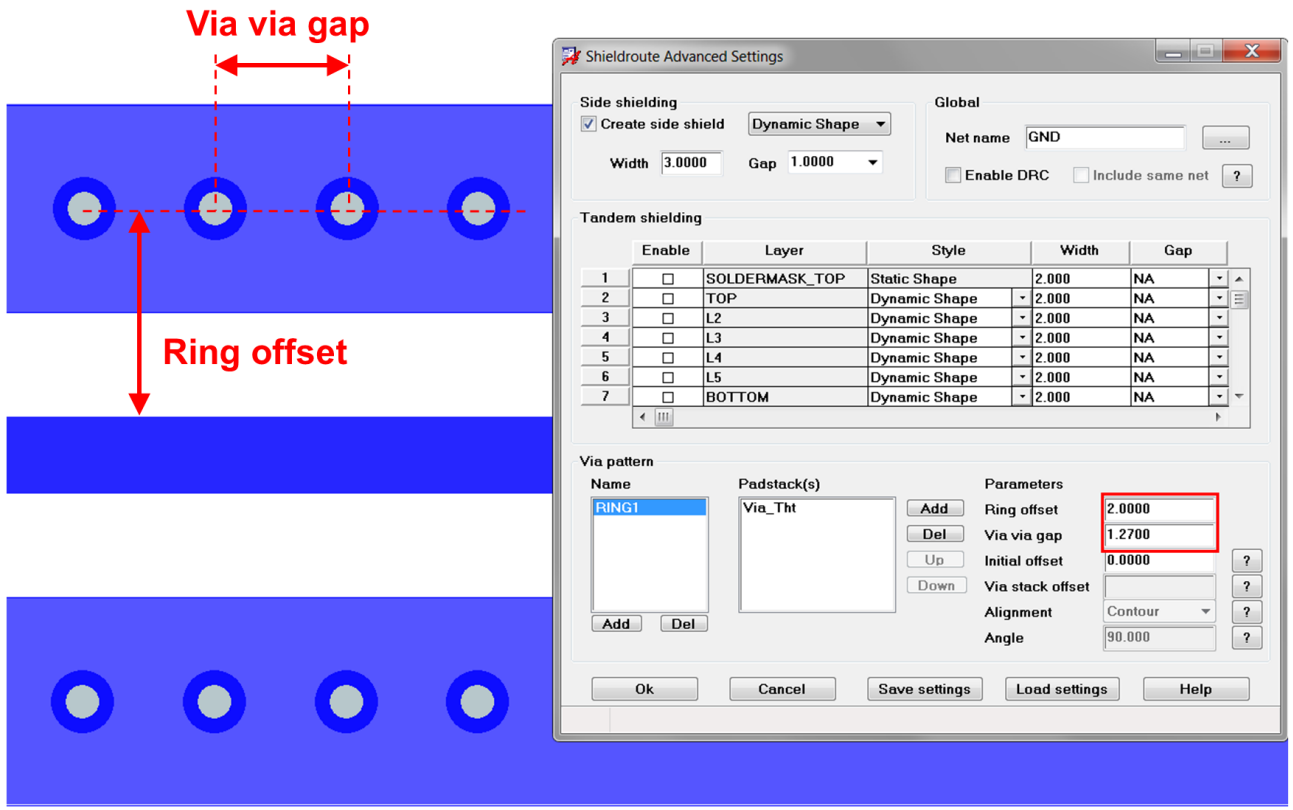


- Parameter probe
  - Simply copy parameters from one structure to another
  - Parameters will be extracted and can be applied to other clines



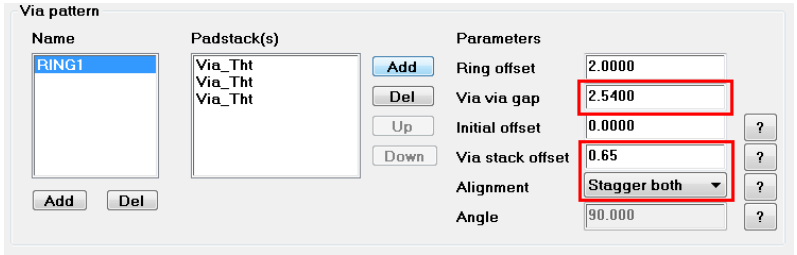
Shield Routing

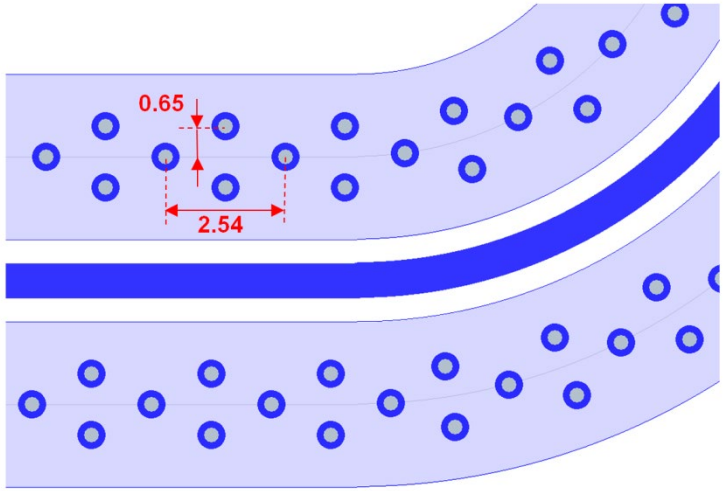
- Via pattern generation
  - Use **Advanced Parameters** form to specify
  - Multiple rings can be specified
  - Settings which apply to padstacks, offsets, alignment, angles, etc.

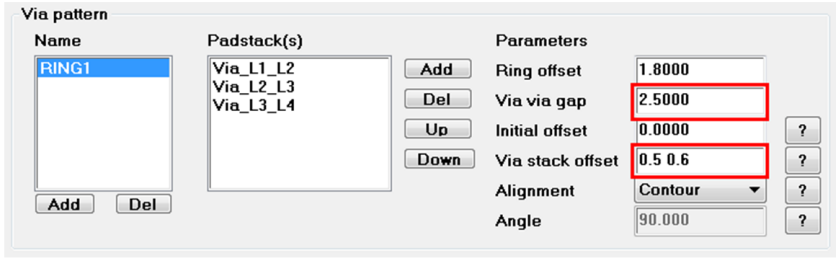


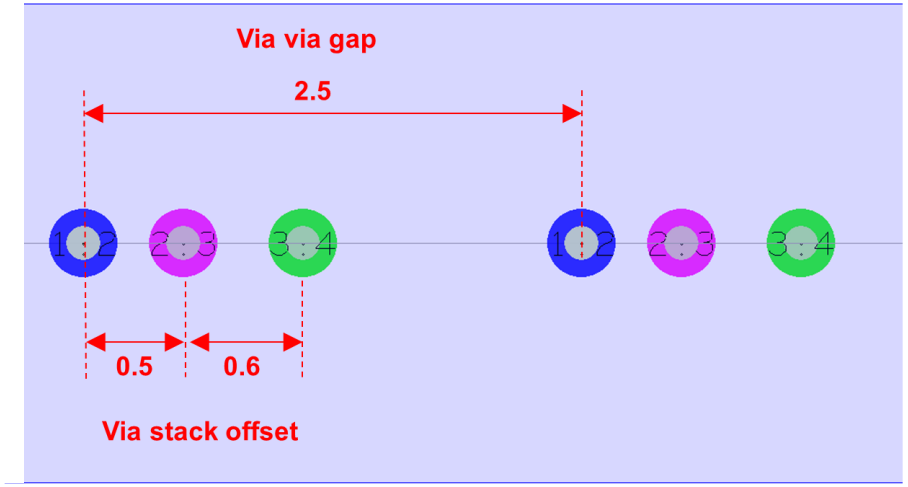
Shield Routing

- Advanced via pattern settings
  - Multiple padstacks (e.g. microvias)
  - Parameter for main stitching gap and gaps within in the stack
  - Staggering option





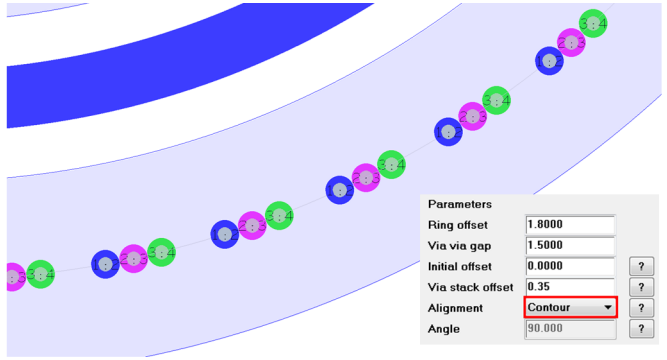




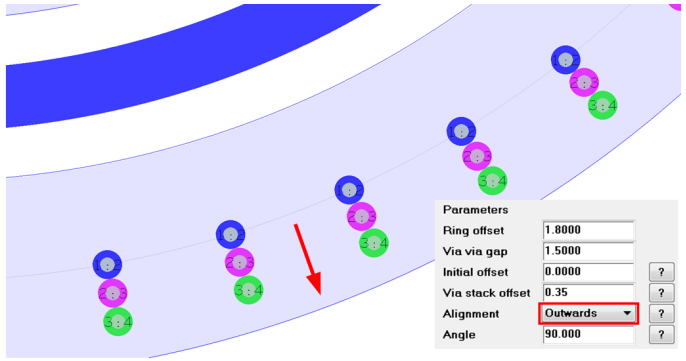
Shield Routing

- Microvia stacking within ring

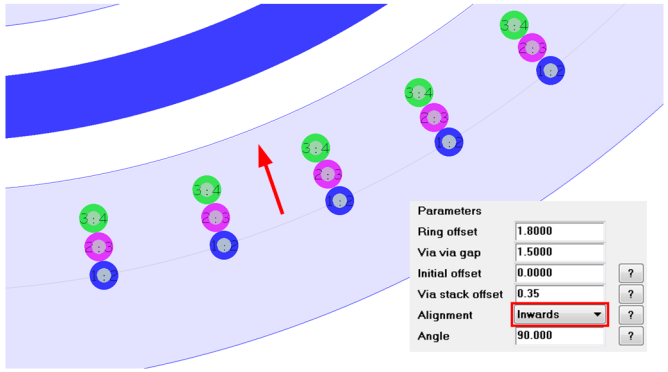
Contour



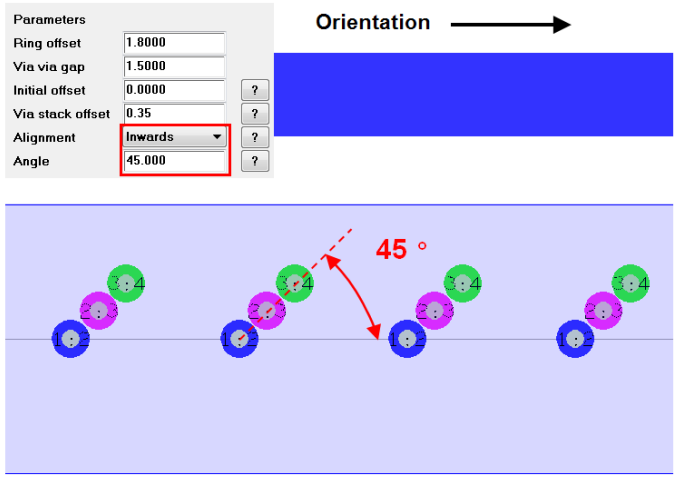
Outwards



Inwards

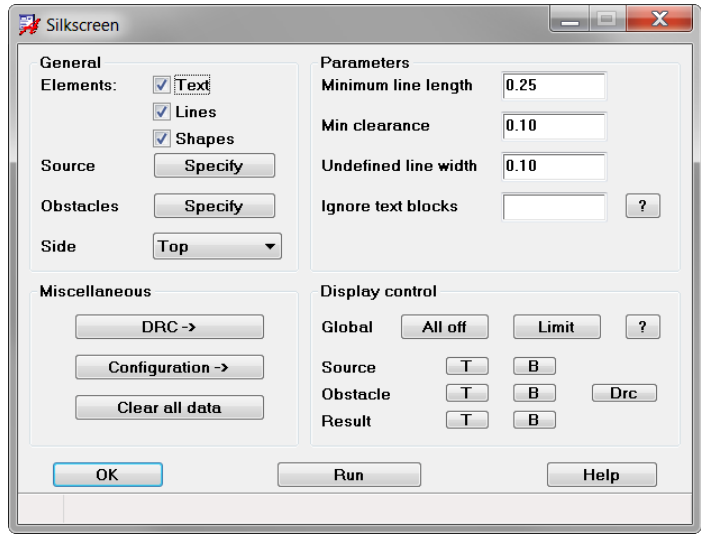


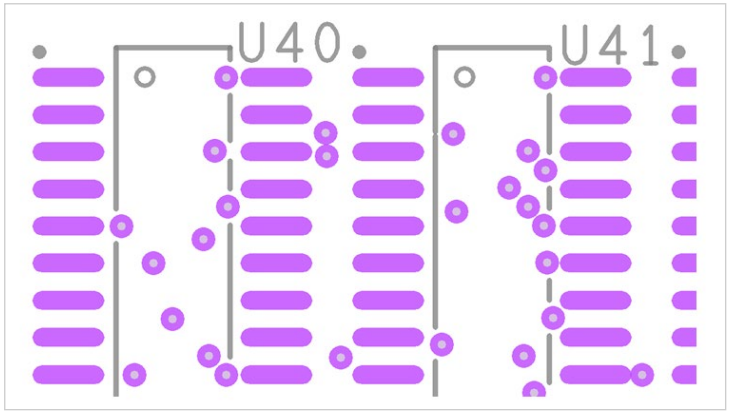
45 deg inwards

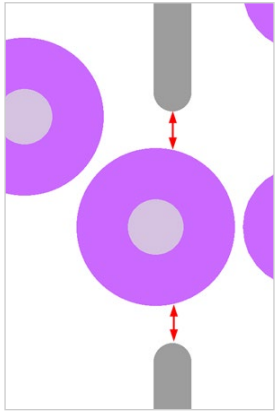


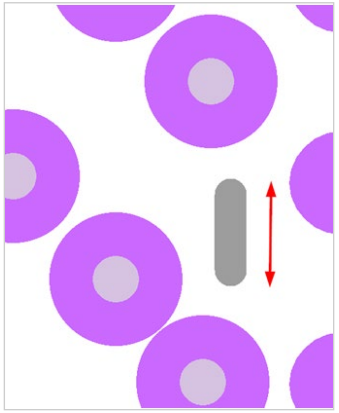
Silkscreen

- Powerful silkscreen utility
- Configuration
  Objects to silk e.g. lines and labels can be configured as well as obstacles which require silk objects to be cut e.g. soldermask, keepout areas
- Rules
  Clearances and minimum segment length can be defined



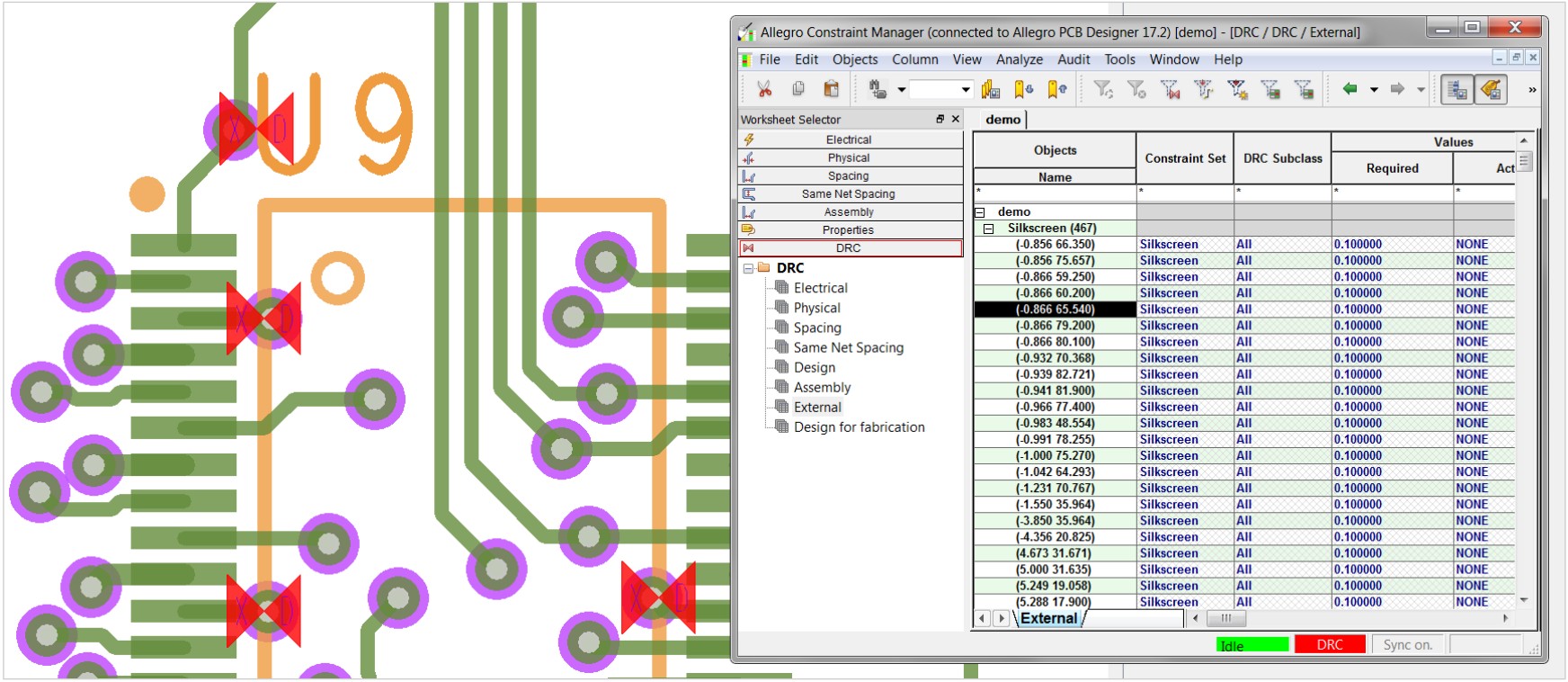






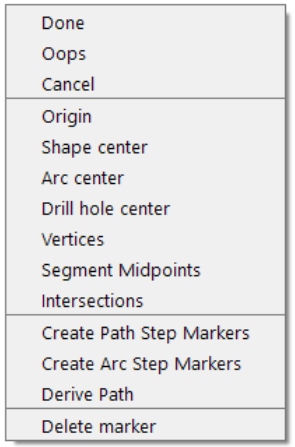
Silkscreen

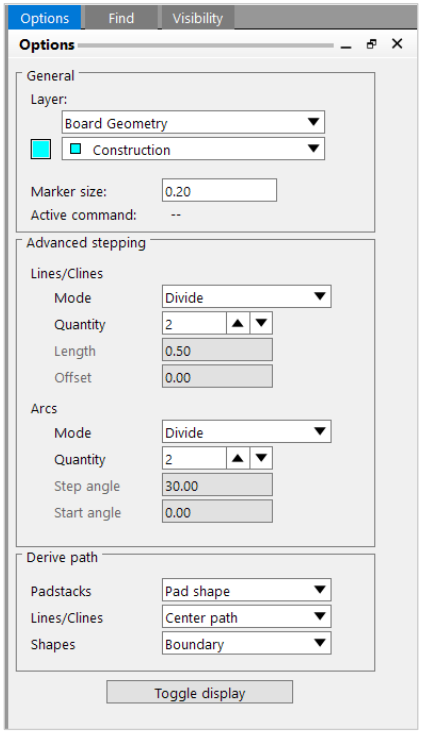
- DRC
  Before generating silkscreen data, a DRC check can be performed, indicating all violations helping users to identify problems and fix them before actual data is generated

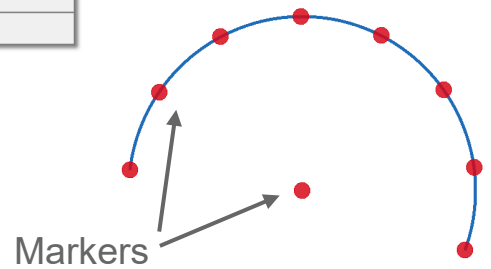


Snap Generator

- Creates persistent markers for snapping operations in PCB Editor
  - Reducing amount of travelling through context menus or using shortcuts
  - Using **Snap pick to – Persistent snap (Shape Center)** then increases efficiency
- Basic markers
  - Origin, Center, Vertices, Midpoints
  - Intersections
- Advanced step markers
  - Divide / Incremental path stepping
  - Angular stepping for arc segments
- Derive path from objects for further processing
  - E.g. pad boundary, slot holes

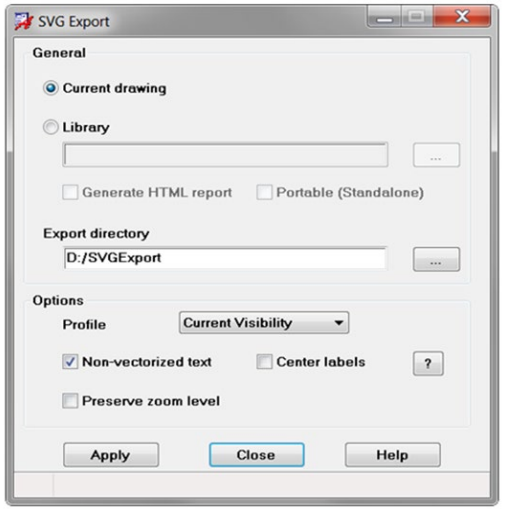


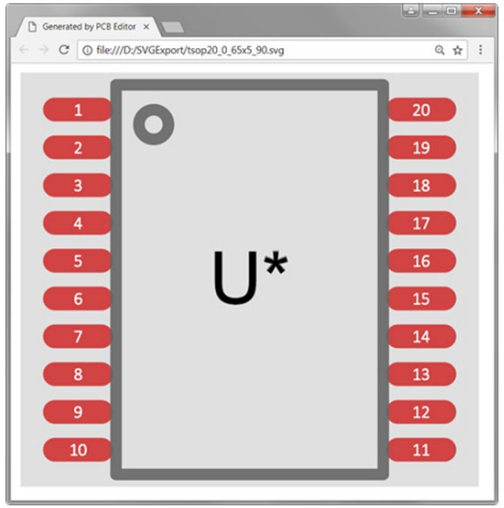




SVG Export

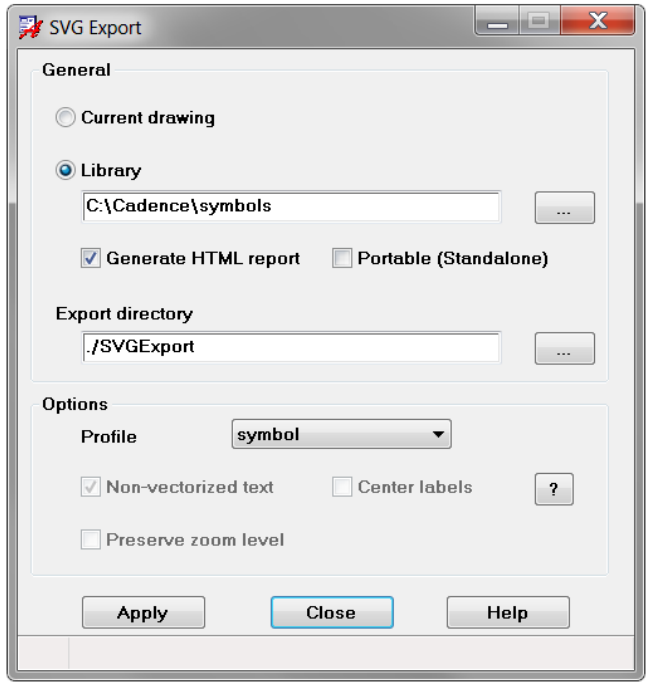
- Generates SVG data out of **PCB Editor**
- Export SVG from current drawing
- Export SVGs for a complete footprint library including HTM report generation
- Profile support
  - Content (layers) and styles (e.g. colors, opacity, non-vectorized texts, etc.) can be specified using predefined profiles

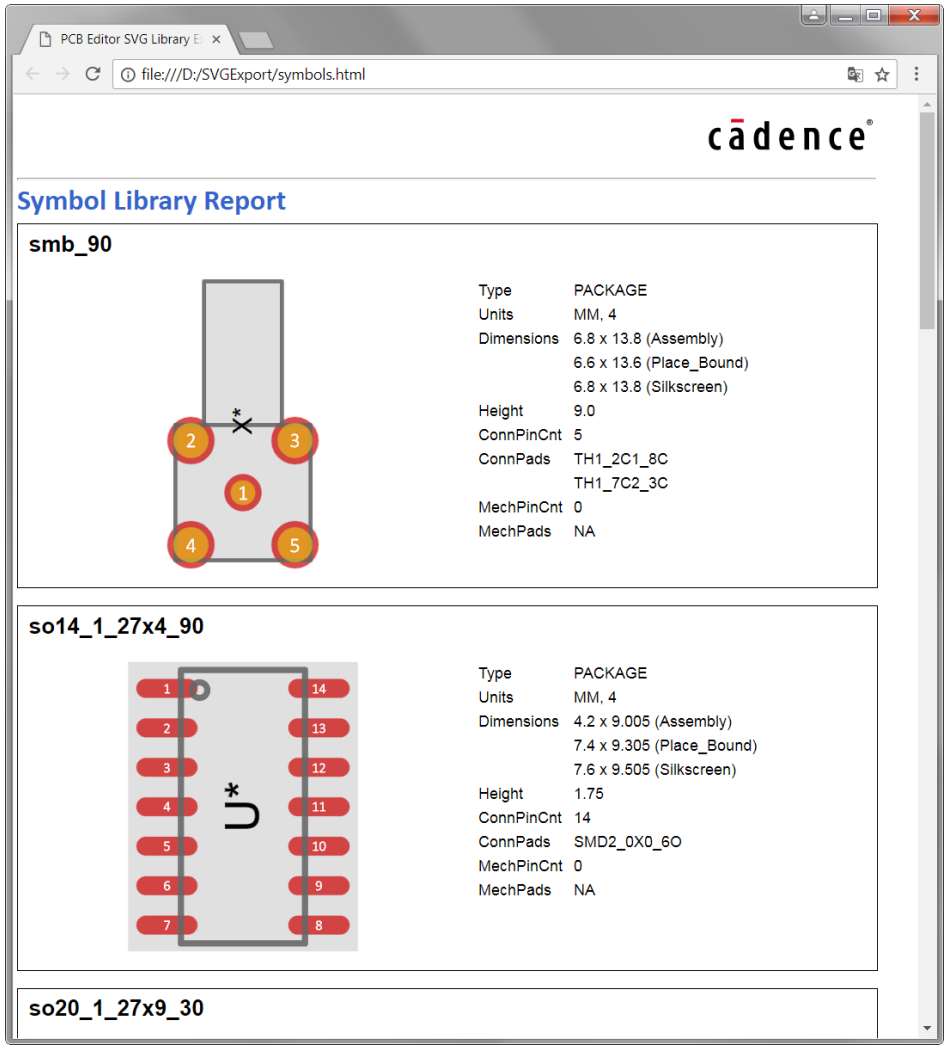




SVG Export

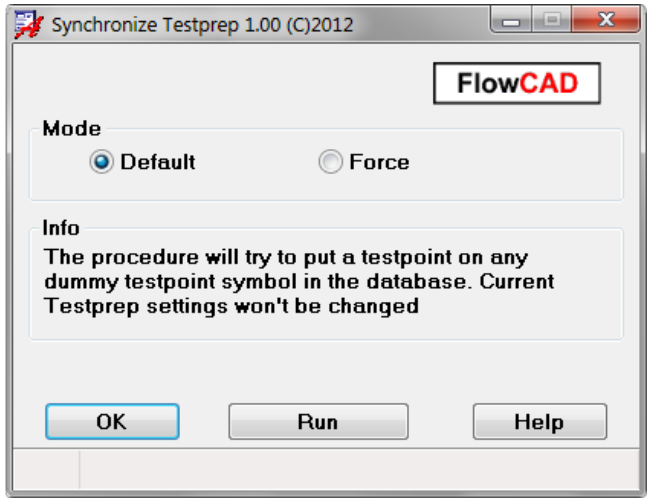
- Example for HTML library report

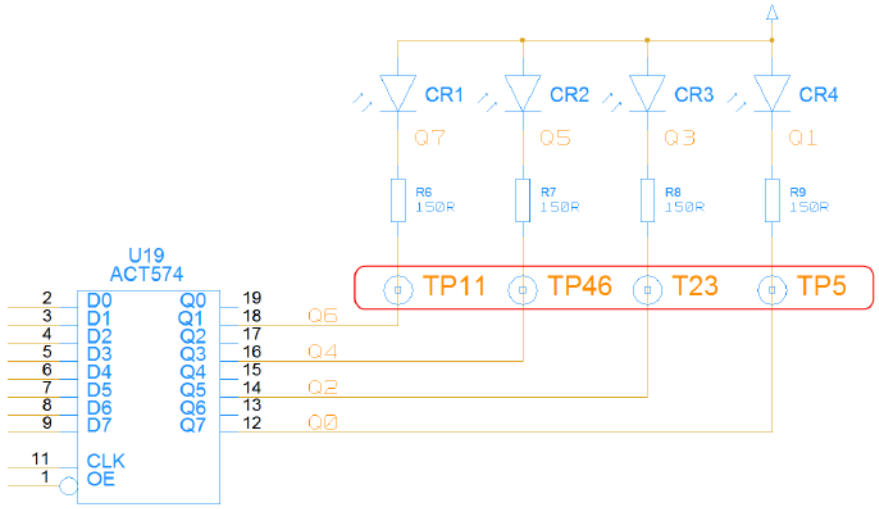


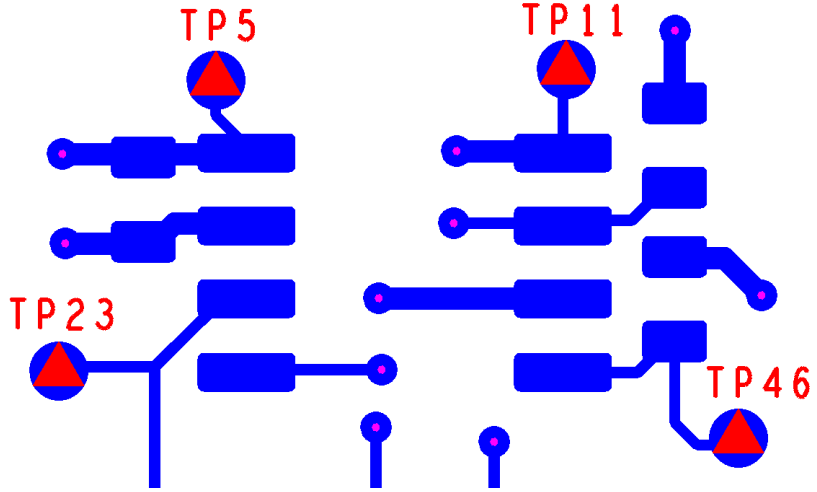


Synchronize Testprep

- Automates the testpoint assignment in PCB Editor when dummy testpoint symbols (one-pin components with Refdes TP*) have been used in the schematic
- Generates testpoint on corresponding pin in PCB
- Post processing can then be done using PCB Editor Testprep functionality

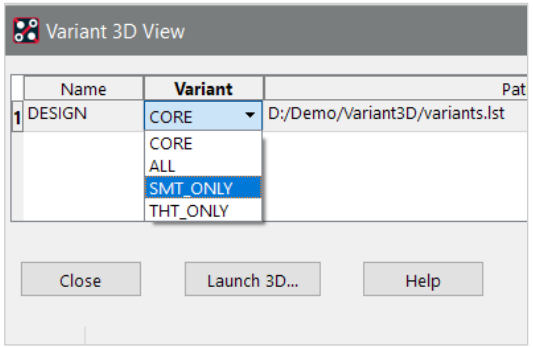




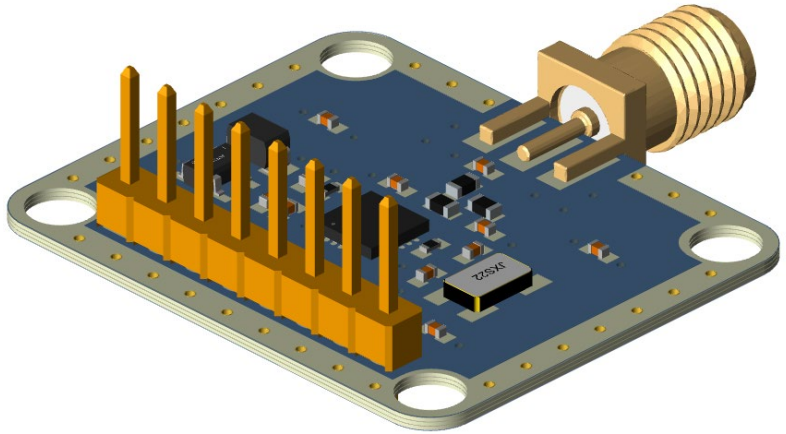


Variant 3D

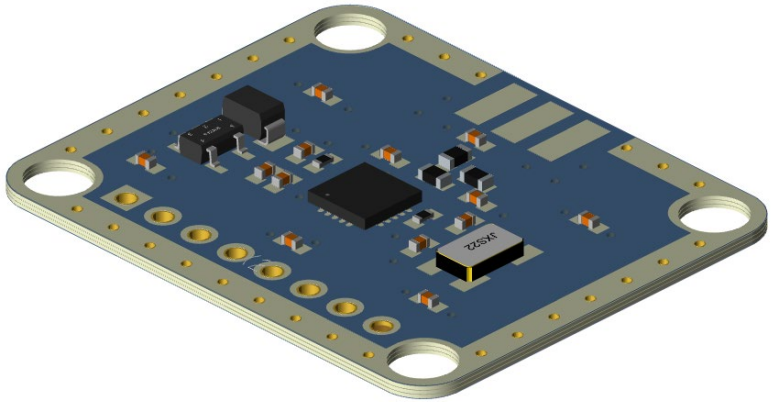
- Application that supports 3D variants
  - Based on data from variants.lst
  - Single boards
  - Regular panels
  - Multi board panels



CORE

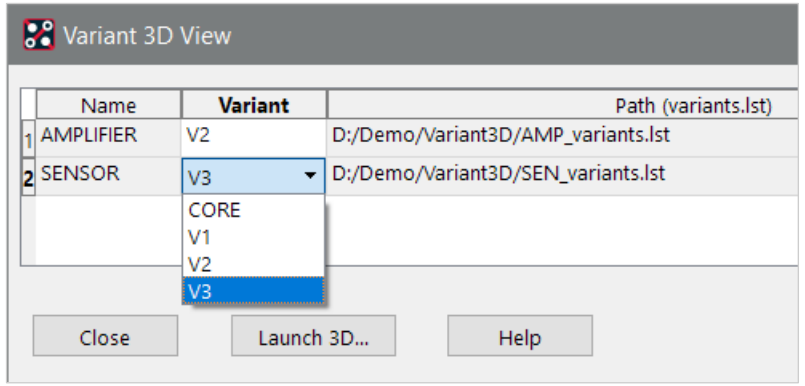


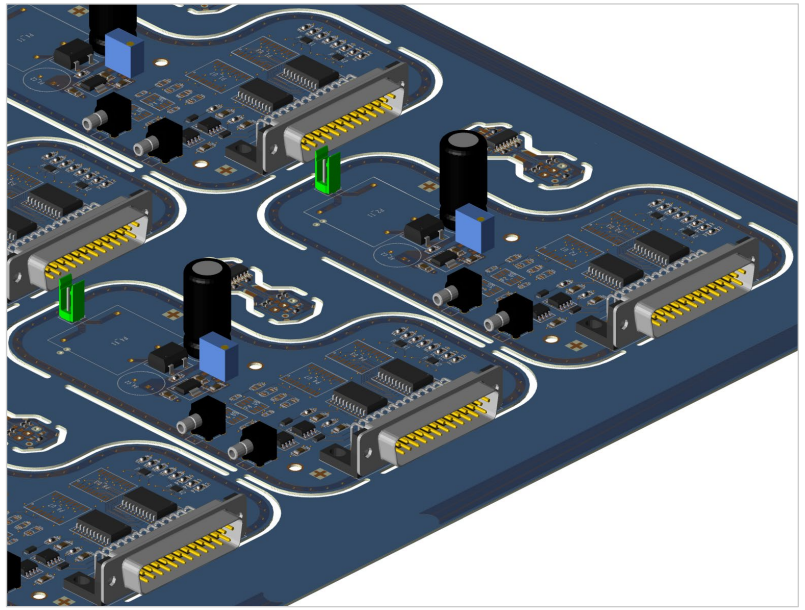
SMT_ONLY

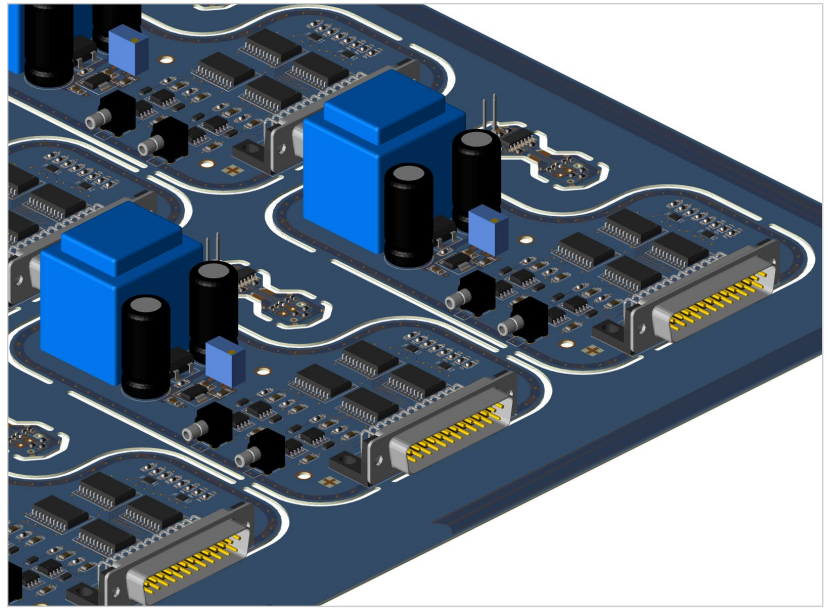


Variant 3D

- Multi board panels





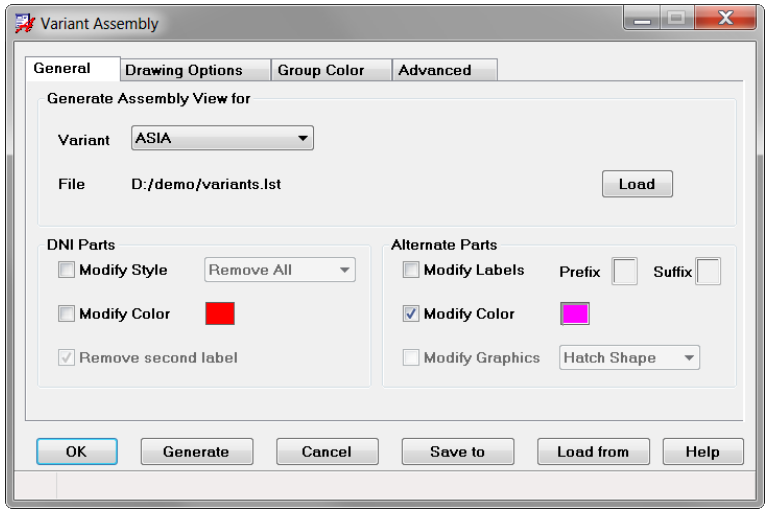


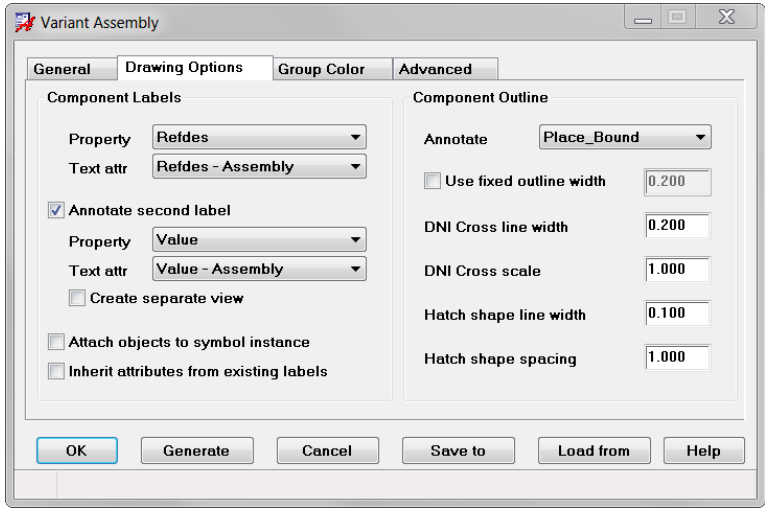
Variant Assembly

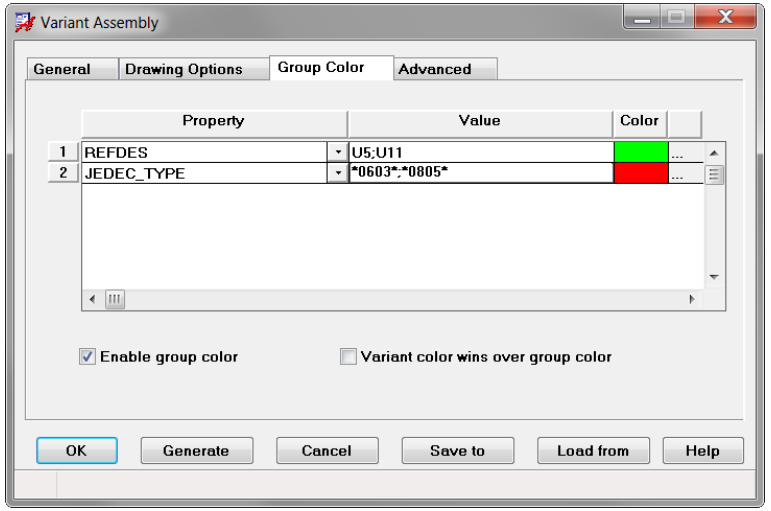
- **Gives customers even more flexibility when creating variant assembly views**
- **Features**
  - Automatic generation of all assembly variant views in one step
  - Customizable label content, e.g. Refdes, Value, Part_Number with the ability to annotate two labels per component
  - Customizable component outline, e.g. Assembly, Place_Bound, Silkscreen, …
  - Customizable style for DNI components, e.g. remove all or draw a thick cross through the label, …
  - Customizable style for Alternate components by using label prefix / suffix, changing colors or hatching component outline
  - Supports rule based coloring of objects, e.g. all SMT in green
  - Automatic mirroring of bottom view for better readability
  - Settings stored in database

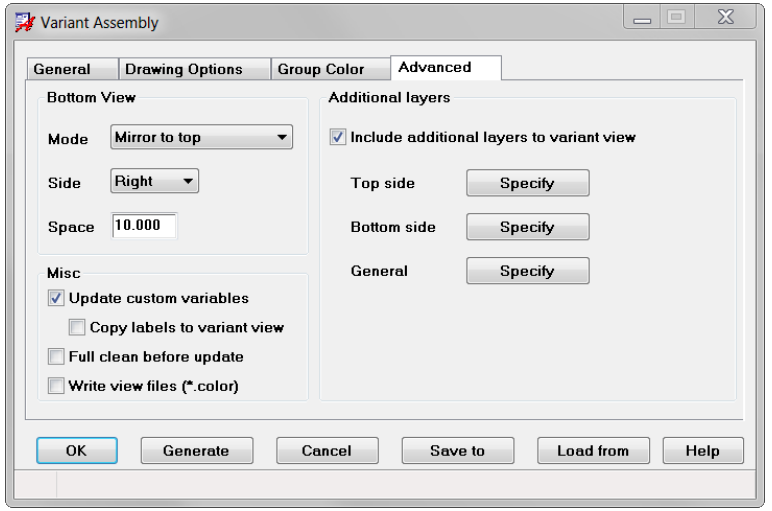
Variant Assembly

User interface



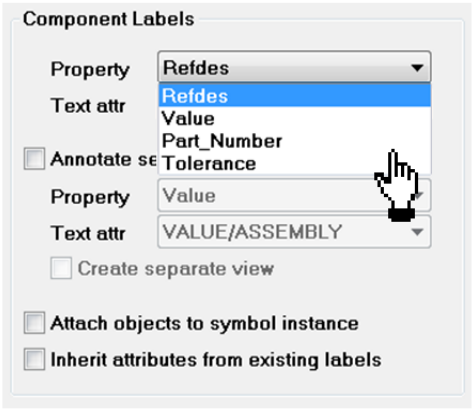


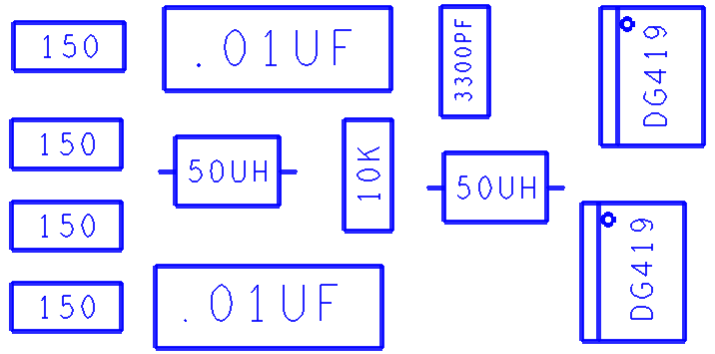




Variant Assembly

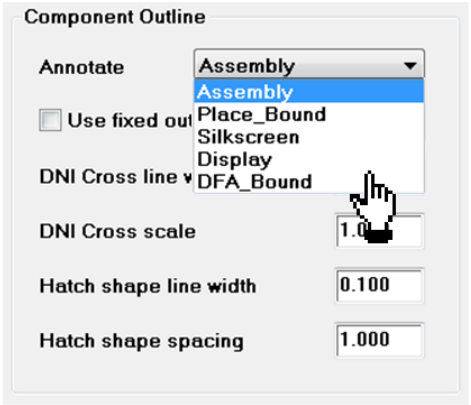
Customizable label content to be displayed (default is Refdes)

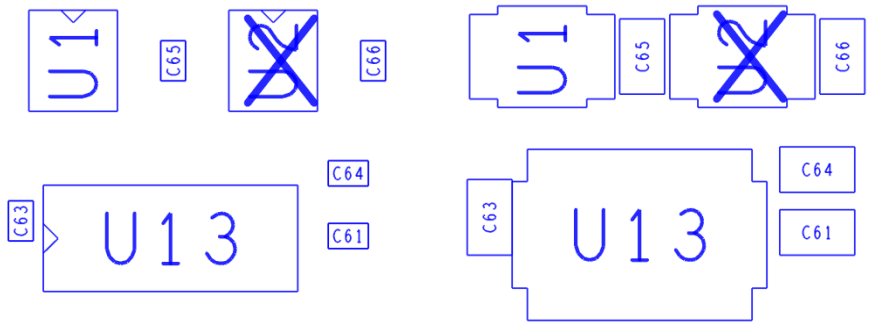




e.g. VALUE property

Customizable component outline to be displayed (default is Assembly)





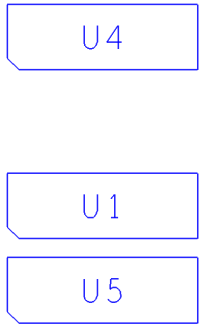
Assembly outline

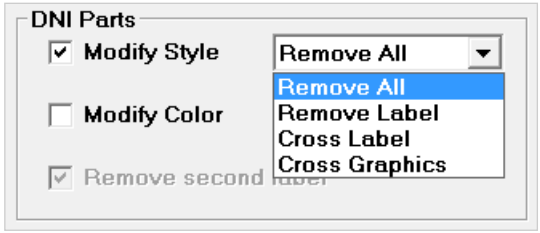
Placebound outline

Variant Assembly

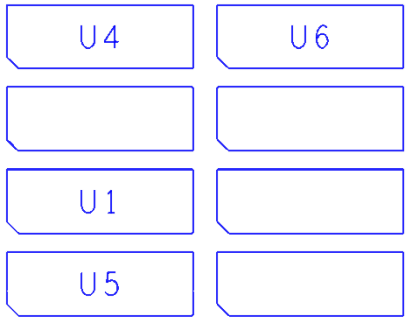
Available styles for DNI parts

Style “Remove All”

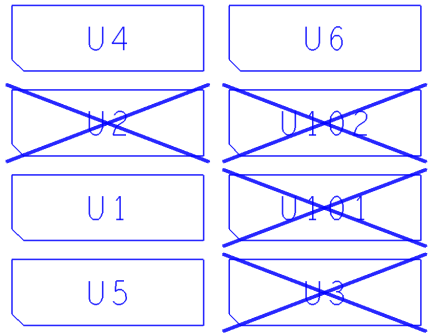




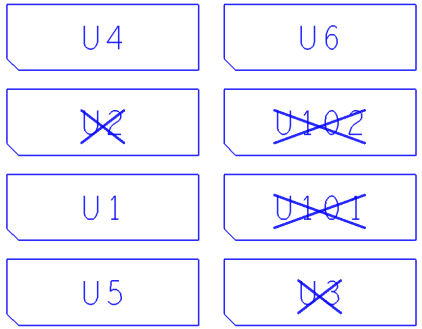
Style “Remove Label”



Style “Cross Graphics”



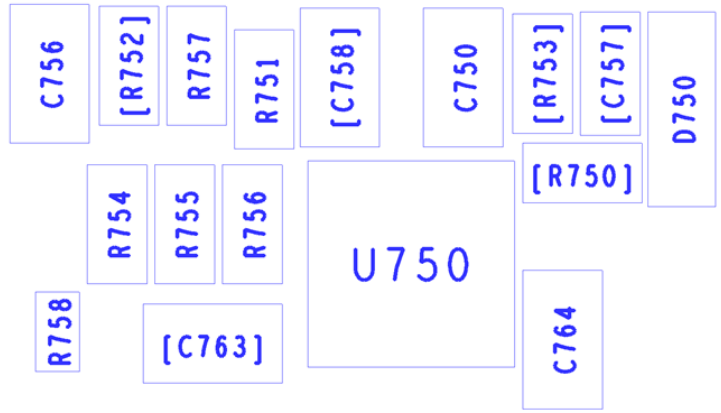
Style “Cross Label”



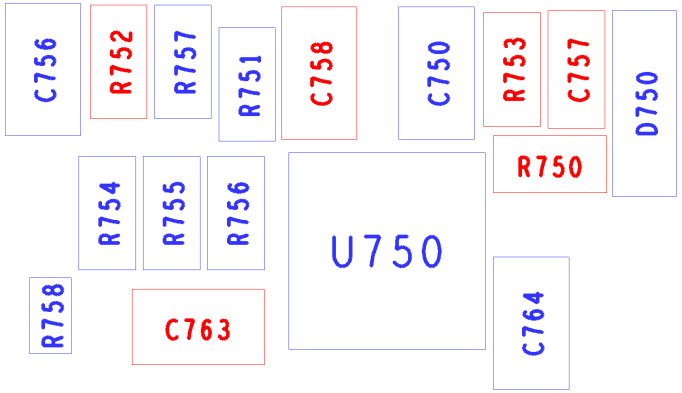
Module: Variant Assembly

Available styles for alternate parts

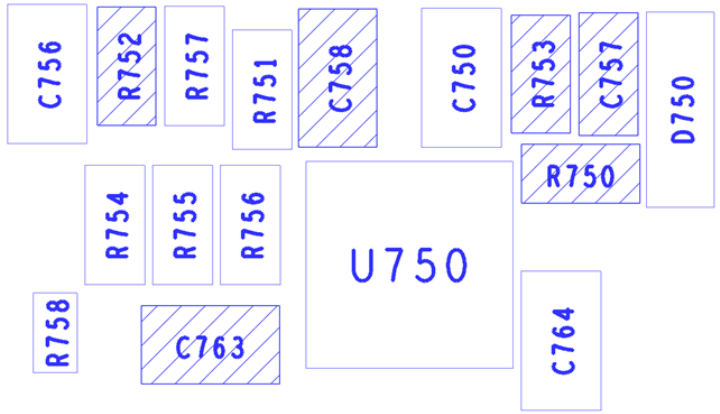
Style “Modify Labels”



Style “Modify Colors”

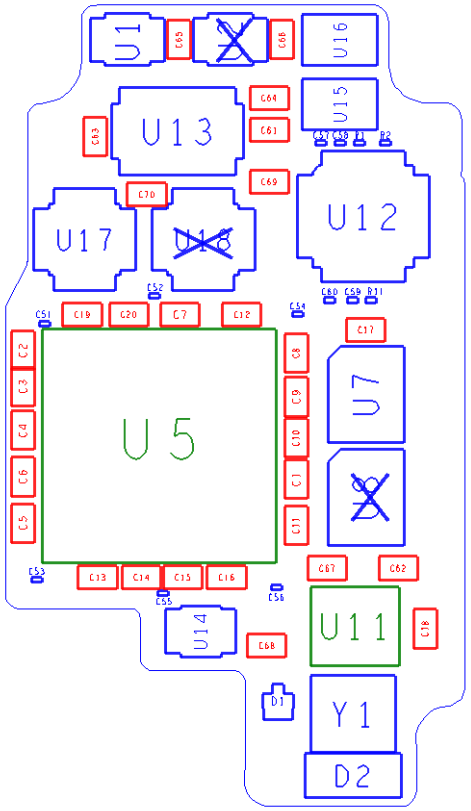


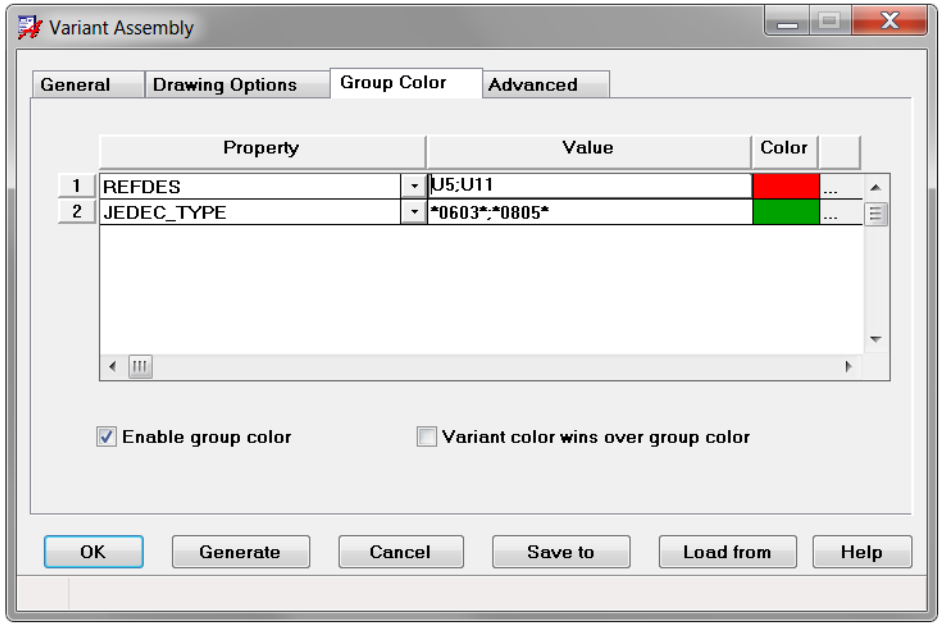
Style “Modify Graphics”



Module: Variant Assembly

Rule based coloring of components

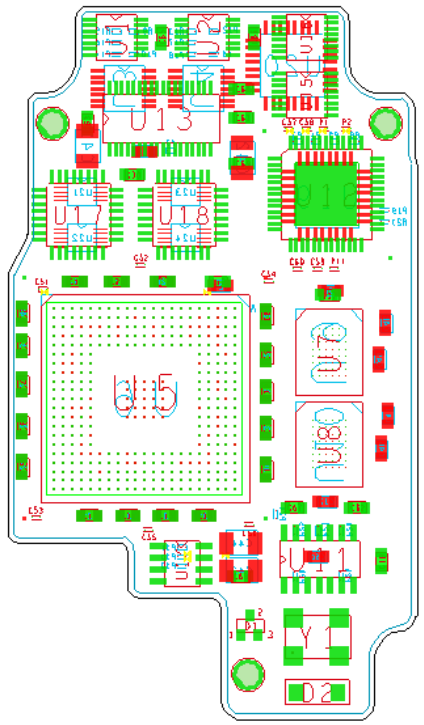


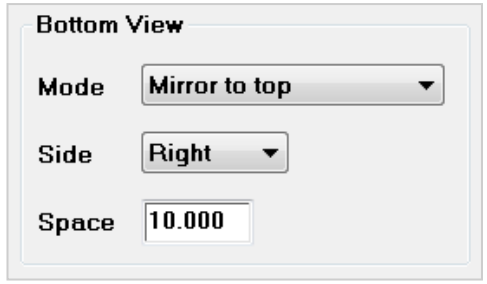


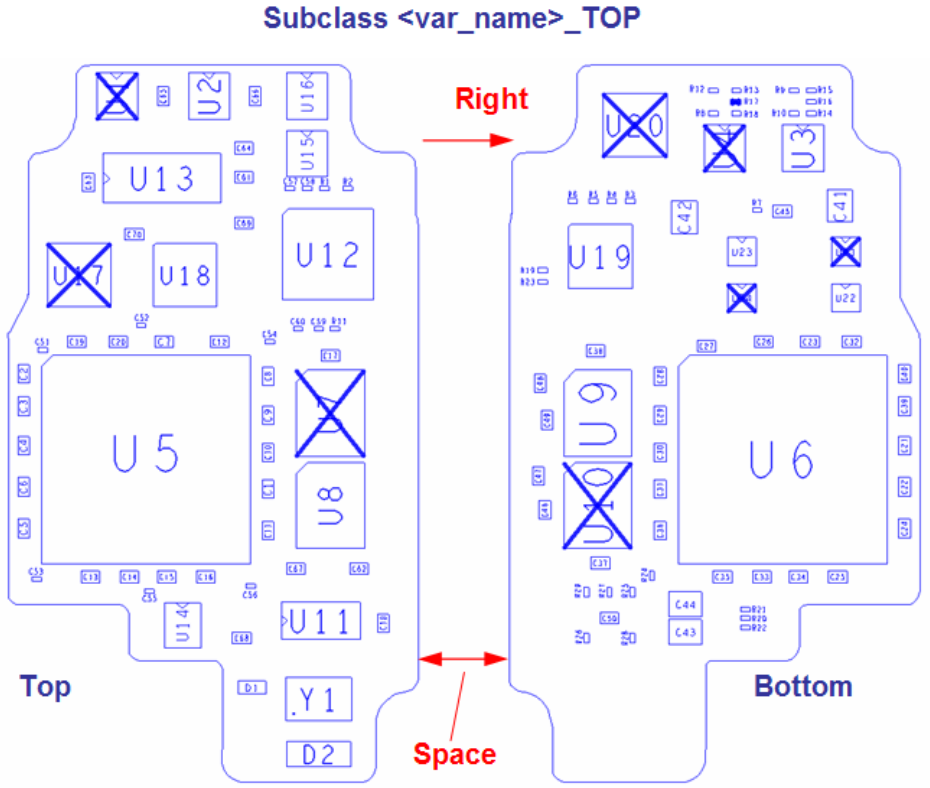
- Color rules can be linked to individual properties
- Several match pattern per rule
- Wildcard support

Variant Assembly

Automatic mirroring of bottom view e.g. side by side to top view





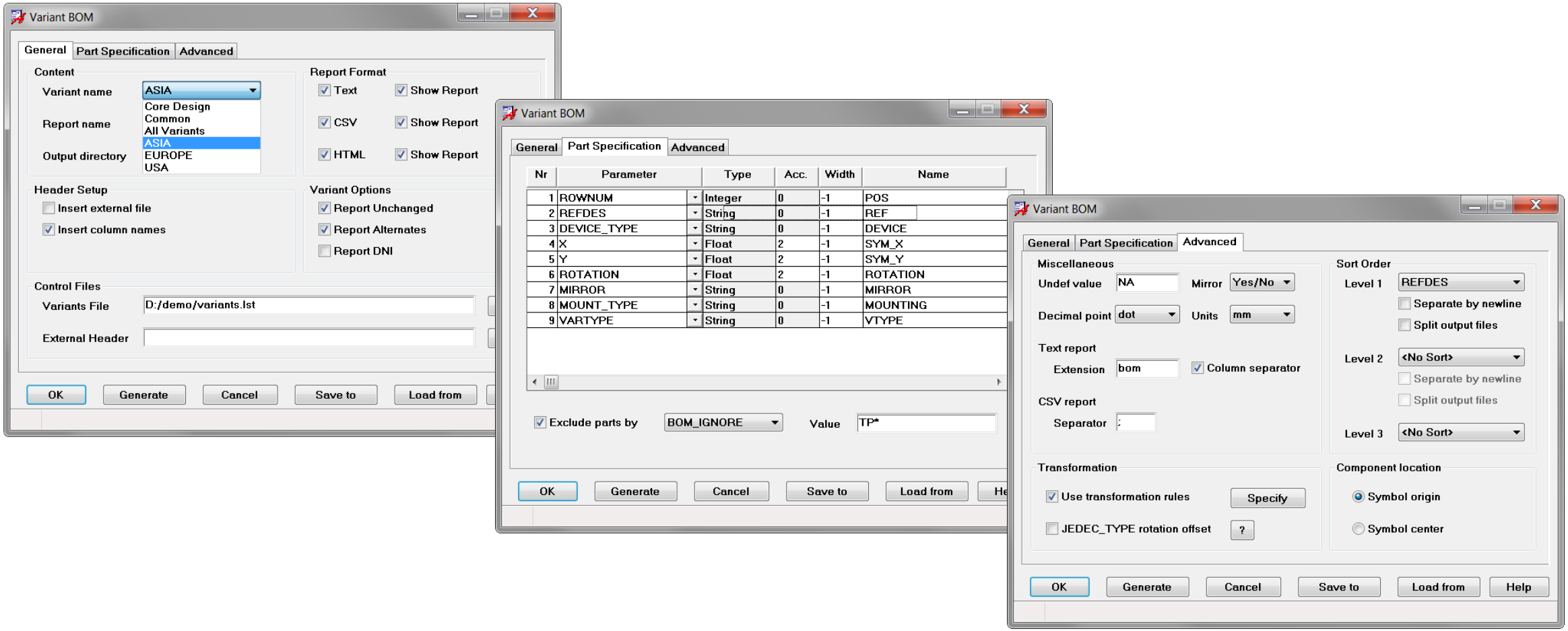


Variant BOM

- **Creates various reports (BOM) from layout database taking variant information into account**
  - Generates reports (e.g. pick & place) data for a variant
  - Can be used for reports on core design also
- **Configurable content**
  - Any database attribute
  - Ability to distinguish between common and variant parts
  - Exclude BOM non-relevant parts (e.g. dummy testpoints)
  - Header information, order of columns, column width
  - Hierarchical sorting up to three levels
  - Option to split output files
  - Settings stored in database, export and import capabilities
- **Output format**
  - HTML, ASCII, CSV

Variant BOM

User Interface



Variant BOM

Report Formats

CSV

File: D:/floware_demo/variant_assembly_bom/worklib/root/physical/master.csv

File Close Help

```
POS;REF;DEVICE;SYM_X;SYM_Y;ROTATION;MIRROR;MOUNTING;VTYPE
1;C1;CAP_805-120PF550V805;114.94;108.33;90.00;NO;SMT;BASE
2;C2;CAP_805-120PF550V805;88.01;121.03;90.00;NO;SMT;BASE
3;C3;CAP_805-120PF550V805;88.01;117.48;90.00;NO;SMT;BASE
4;C4;CAP_805-120PF550V805;88.01;113.16;90.00;NO;SMT;BASE
5;C5;CAP_805-120PF550V805;88.01;104.01;90.00;NO;SMT;BASE
6;C6;CAP_805-120PF550V805;88.01;108.58;90.00;NO;SMT;BASE
;124.59;0.00;NO;SMT;BASE
;120.78;90.00;NO;SMT;BASE
;116.46;90.00;NO;SMT;BASE
94;112.40;90.00;NO;SMT;BASE
94;103.76;90.00;NO;SMT;BASE
58;124.56;0.00;NO;SMT;BASE
8;98.68;0.00;NO;SMT;BASE
0;98.68;0.00;NO;SMT;BASE
76;98.68;0.00;NO;SMT;BASE
08;98.68;0.00;NO;SMT;BASE
79;123.06;0.00;NO;SMT;BASE
63;93.60;90.00;NO;SMT;BASE
5;124.59;0.00;NO;SMT;BASE
2;124.59;0.00;NO;SMT;BASE
1;113.16;270.00;YES;SMT;BASE
1;108.58;270.00;YES;SMT;BASE
2;124.59;180.00;YES;SMT;BASE
1;104.01;270.00;YES;SMT;BASE
8;98.68;180.00;YES;SMT;BASE
51;124.59;180.00;YES;SMT;BASE
86;124.08;180.00;YES;SMT;BASE
94;120.78;270.00;YES;SMT;BASE
94;116.46;270.00;YES;SMT;BASE
94;112.40;270.00;YES;SMT;BASE
94;108.33;270.00;YES;SMT;BASE
5;124.59;180.00;YES;SMT;BASE
76;98.68;180.00;YES;SMT;BASE
0;98.68;180.00;YES;SMT;BASE
```

Text

File: D:/floware_demo/variant_assembly_bom/worklib/root/physical/master.bom

File Close Help

POS	REF	DEVICE	SYM_X	SYM_Y	ROTATION	MIRROR	MOUNTING	VTYPE
1	C1	CAP_805-120PF550V805	114.94	108.33	90.00	NO	SMT	BASE
2	C2	CAP_805-120PF550V805	88.01	121.03	90.00	NO	SMT	BASE
3	C3	CAP_805-120PF550V805	88.01	117.48	90.00	NO	SMT	BASE
4	C4	CAP_805-120PF550V805	88.01	113.16	90.00	NO	SMT	BASE
5	C5	CAP_805-120PF550V805	88.01	104.01	90.00	NO	SMT	BASE
6	C6	CAP_805-120PF550V805	88.01	108.58	90.00	NO	SMT	BASE
7	C7	CAP_805-120PF550V805	103.51	124.59	0.00	NO	SMT	BASE
			114.94	120.78	90.00	NO	SMT	BASE
			114.94	116.46	90.00	NO	SMT	BASE
			114.94	112.40	90.00	NO	SMT	BASE
			114.94	103.76	90.00	NO	SMT	BASE
			109.58	124.56	0.00	NO	SMT	BASE
			95.38	98.68	0.00	NO	SMT	BASE
			99.70	98.68	0.00	NO	SMT	BASE
			103.76	98.68	0.00	NO	SMT	BASE
			108.08	98.68	0.00	NO	SMT	BASE
			121.79	123.06	0.00	NO	SMT	BASE
			127.63	93.60	90.00	NO	SMT	BASE
			93.85	124.59	0.00	NO	SMT	BASE
			98.42	124.59	0.00	NO	SMT	BASE
			88.01	113.16	270.00	YES	SMT	BASE
			88.01	108.58	270.00	YES	SMT	BASE
			98.42	124.59	180.00	YES	SMT	BASE
			88.01	104.01	270.00	YES	SMT	BASE
			95.38	98.68	180.00	YES	SMT	BASE
			103.51	124.59	180.00	YES	SMT	BASE
			109.86	124.08	180.00	YES	SMT	BASE
			114.94	120.78	270.00	YES	SMT	BASE
			114.94	116.46	270.00	YES	SMT	BASE
			114.94	112.40	270.00	YES	SMT	BASE
			114.94	108.33	270.00	YES	SMT	BASE
			93.85	124.59	180.00	YES	SMT	BASE

HTML

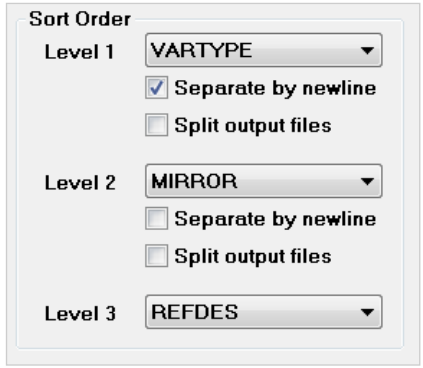
File: D:/floware_demo/variant_assembly_bom/worklib/root/physical/master.html

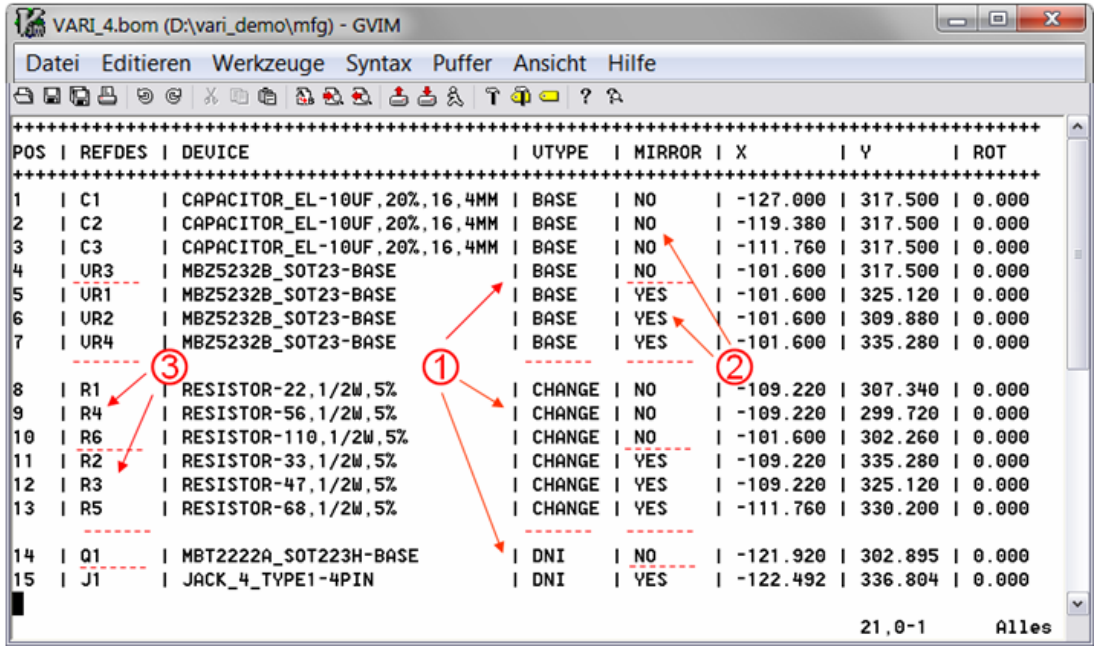
Search: Match word Match case

POS	REF	DEVICE	SYM_X	SYM_Y	ROTATION	MIRROR	MOUNTING	VTYPE
1	C1	CAP_805-120PF550V805	114.94	108.33	90.00	NO	SMT	BASE
2	C2	CAP_805-120PF550V805	88.01	121.03	90.00	NO	SMT	BASE
3	C3	CAP_805-120PF550V805	88.01	117.48	90.00	NO	SMT	BASE
4	C4	CAP_805-120PF550V805	88.01	113.16	90.00	NO	SMT	BASE
5	C5	CAP_805-120PF550V805	88.01	104.01	90.00	NO	SMT	BASE
6	C6	CAP_805-120PF550V805	88.01	108.58	90.00	NO	SMT	BASE
7	C7	CAP_805-120PF550V805	103.51	124.59	0.00	NO	SMT	BASE
8	C8	CAP_805-120PF550V805	114.94	120.78	90.00	NO	SMT	BASE
9	C9	CAP_805-120PF550V805	114.94	116.46	90.00	NO	SMT	BASE
10	C10	CAP_805-120PF550V805	114.94	112.40	90.00	NO	SMT	BASE
11	C11	CAP_805-120PF550V805	114.94	103.76	90.00	NO	SMT	BASE
12	C12	CAP_805-120PF550V805	109.58	124.56	0.00	NO	SMT	BASE
13	C13	CAP_805-120PF550V805	95.38	98.68	0.00	NO	SMT	BASE
14	C14	CAP_805-120PF550V805	99.70	98.68	0.00	NO	SMT	BASE
15	C15	CAP_805-120PF550V805	103.76	98.68	0.00	NO	SMT	BASE
16	C16	CAP_805-120PF550V805	108.08	98.68	0.00	NO	SMT	BASE

Variant BOM

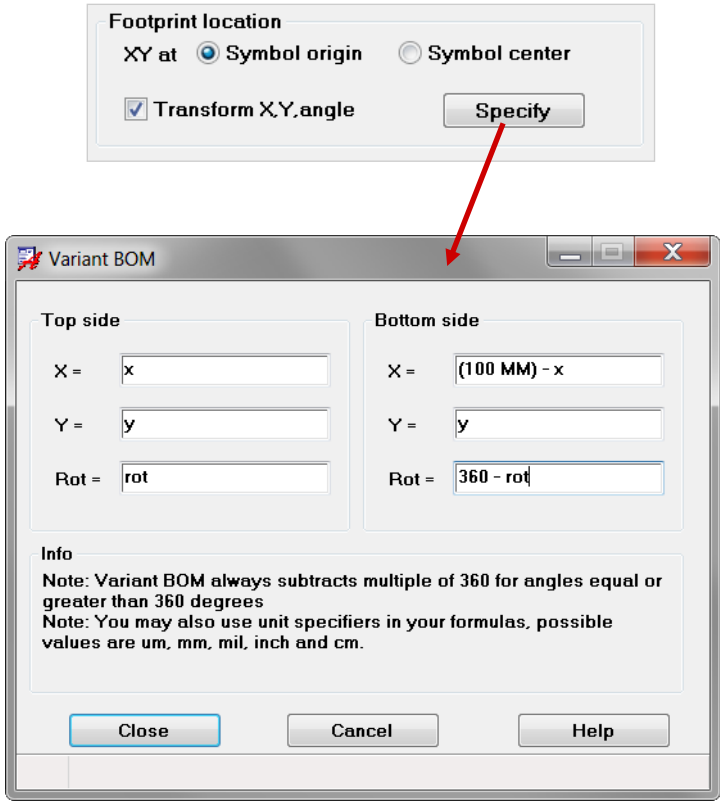
- **Hierarchical sorting**
  - Up to three levels
  - Options to add newline for level 1 and level 2
  - Options to split output files for level 1 and level 2





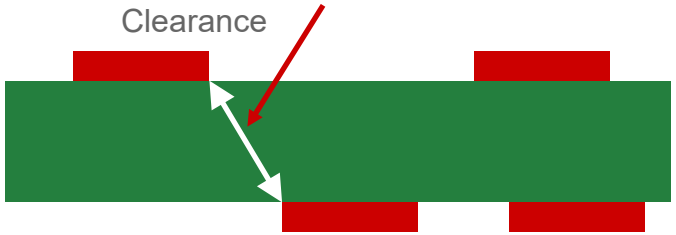
Variant BOM

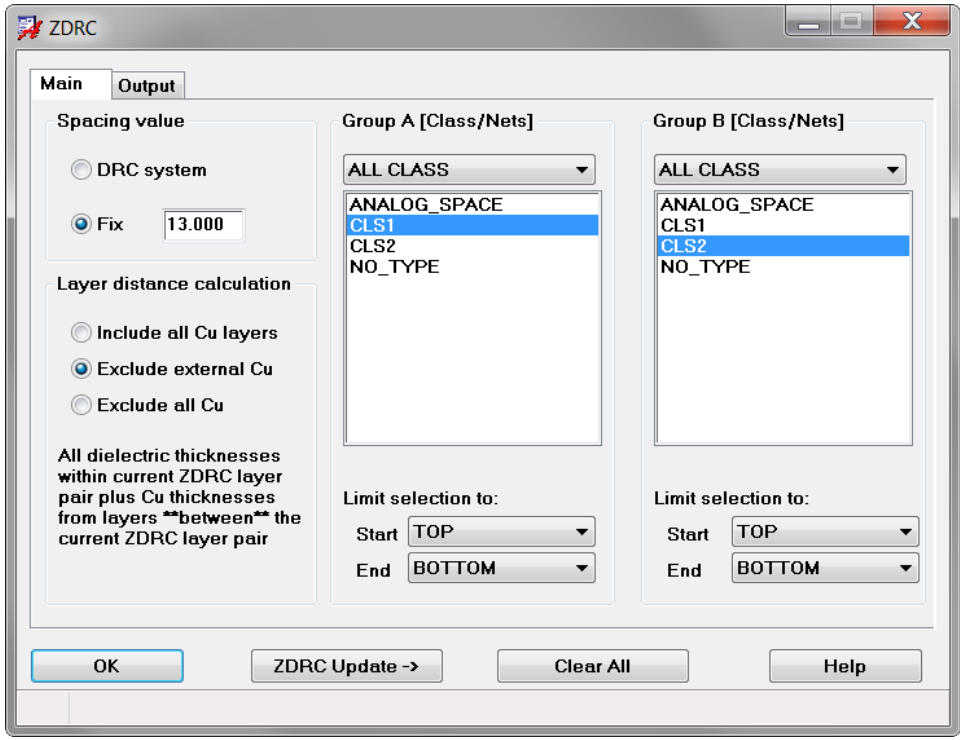
- **Transformation rules**
  - Sometimes users need to transform x, y and rotation due to Pick & Place requirements from manufactory
  - E.g. always subtract 360 from angles given by PCB Editor for components on BOTTOM side
  - Formulas can be specified for TOP and BOTTOM separately
  - Unit specifiers such as MM, MILS etc. are supported



Z-DRC

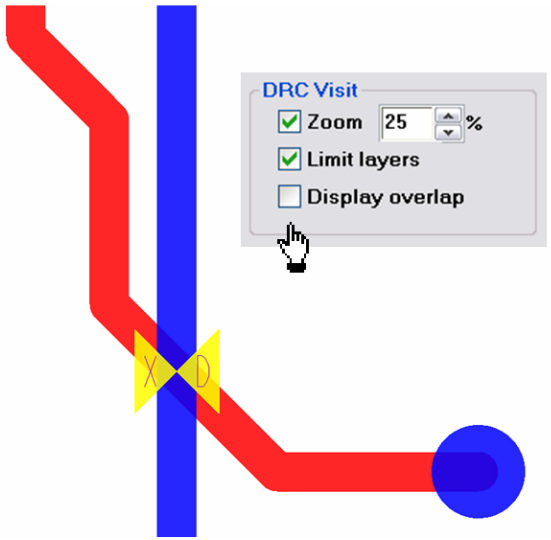
- Checks clearances along the Z-axis
- Useful for applications which have to meet safety and explosion requirements
- Objects to be checked can be specified on net or netclass basis in any combination
- Spacing value can be specified manually or derived from DRC system **(Constraint Manager)**
- Graphical DRC: Markers & Overlapping
- Cross probing and filter capabilities

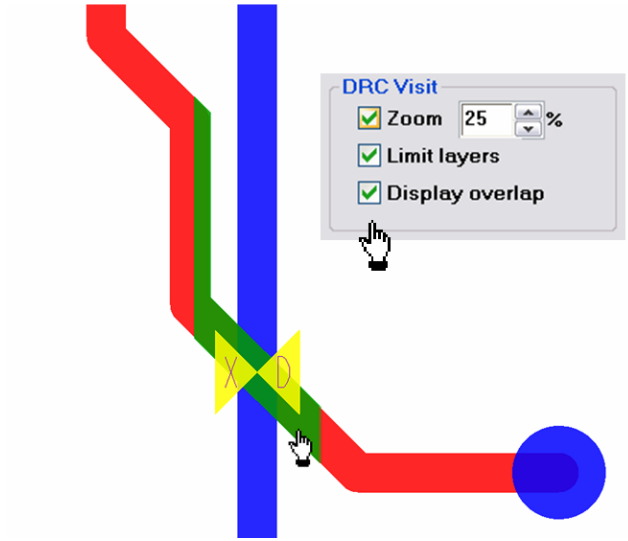


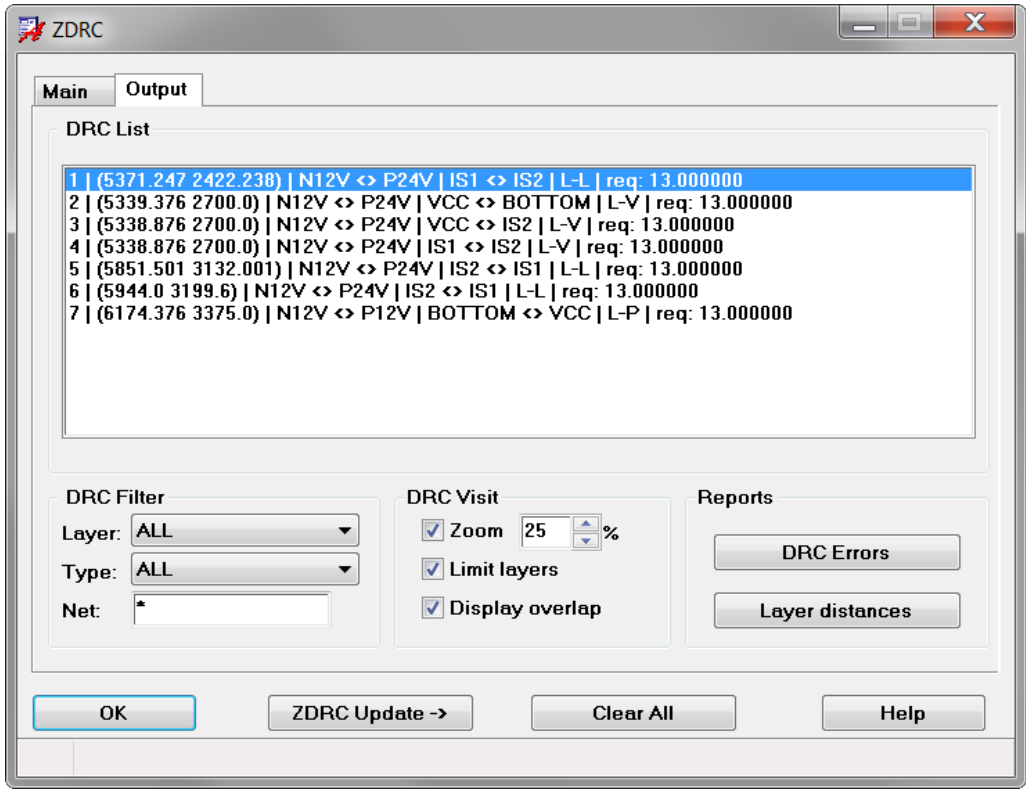


Z-DRC

- The negative margins (amount of overlapping) can be displayed once a DRC has been selected in the Output tab







FloWare Modules
Schematic Entry

OrCAD X Capture / Allegro X Design Entry CIS

FloWare Modules Schematic Entry

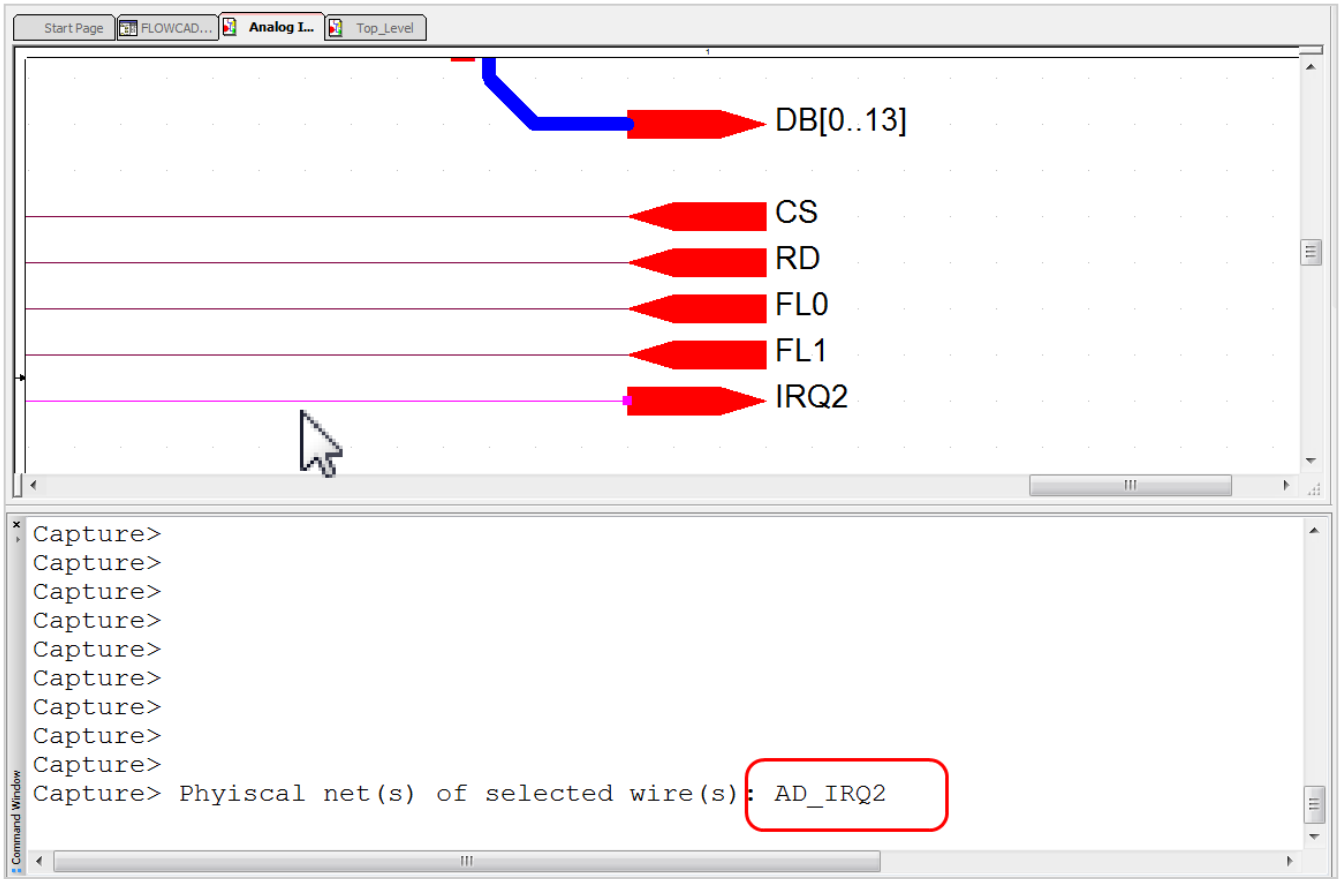
- Flat Net Utilities
- Smart Aliases
- Split Wire
- Testpoint Check
- Tortoise SVN Integration
- Update Titleblock

Flat Net Utilities

- TCL applications with features to report and display the complete physical net (flat net) over all pages
- Very useful for review purposes when working with hierarchical designs
- Fully integrated into standard operations (e.g. select)
- Features
  - Report the physical net name in the command window while selecting wires in the canvas
  - Display the physical net name in tooltip
  - RMB > Highlight / De-highlight physical net over the full hierarchy

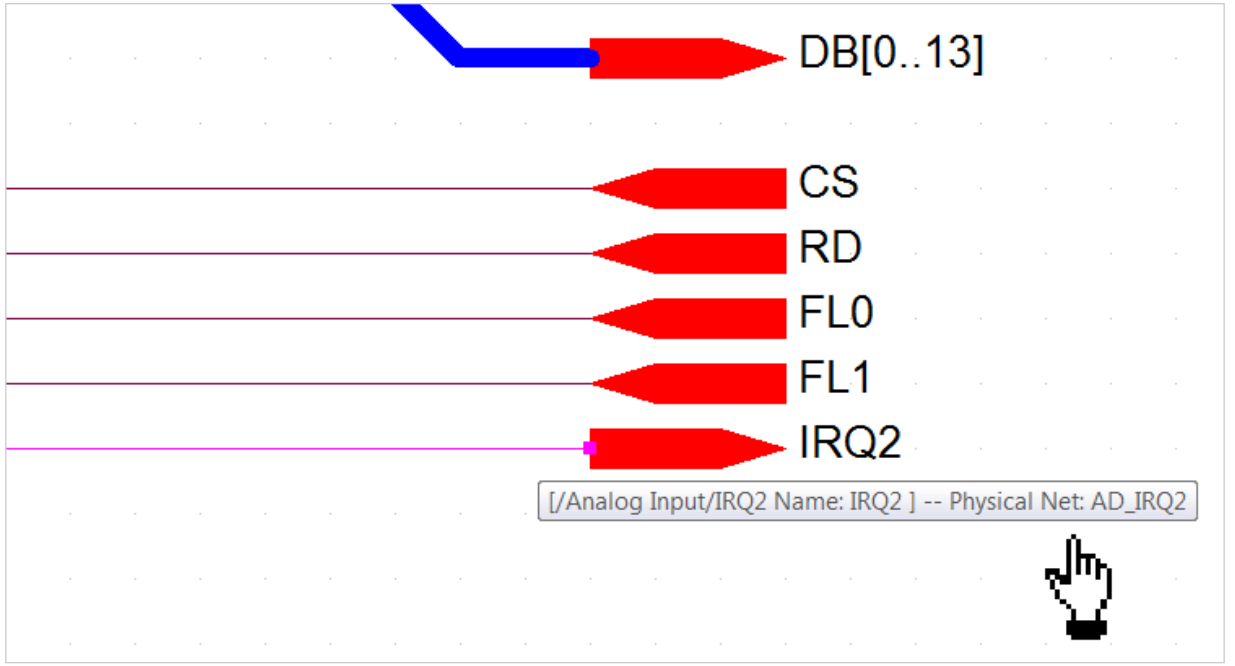
Flat Net Utilities

Physical net name report



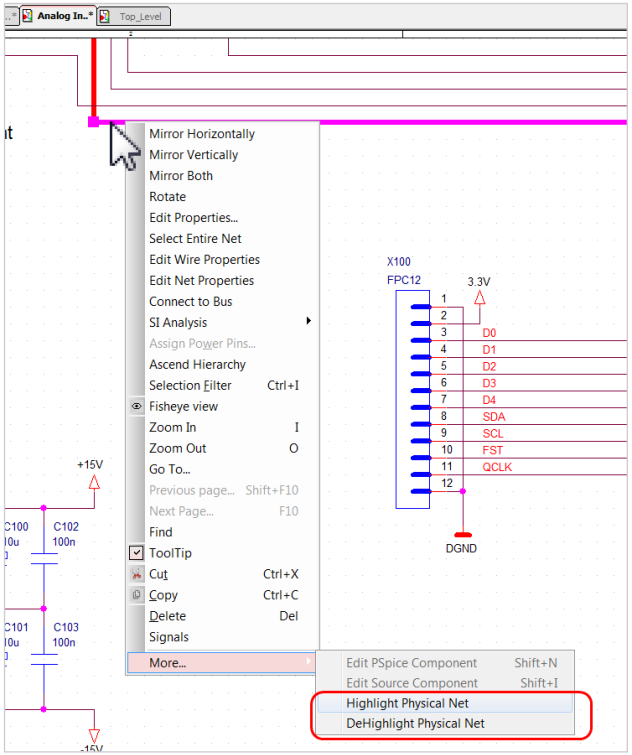
Flat Net Utilities

Tooltip reporting physical net name

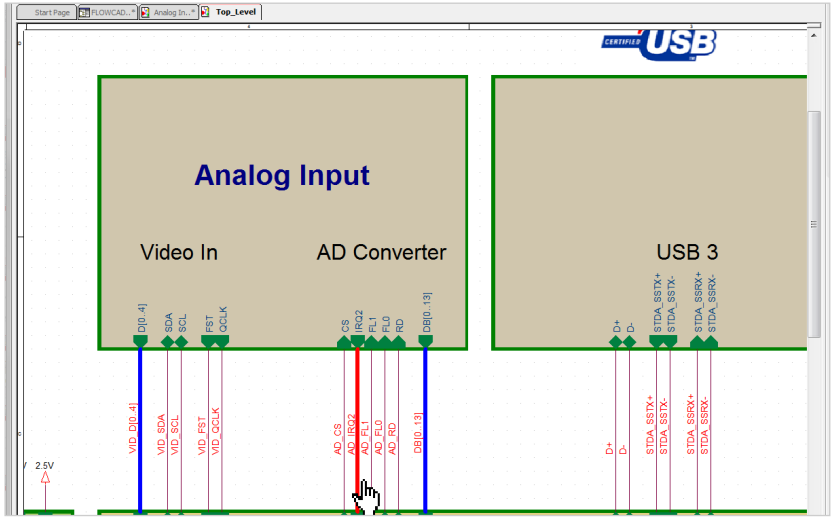


Flat Net Utilities

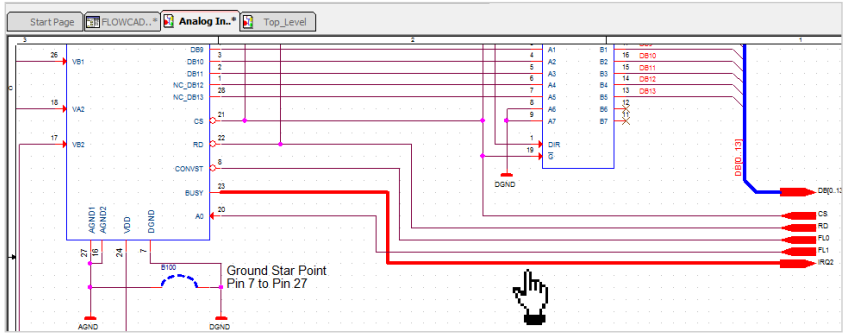
- Highlight / De-highlight physical net on all pages / hierarchies



Top level design

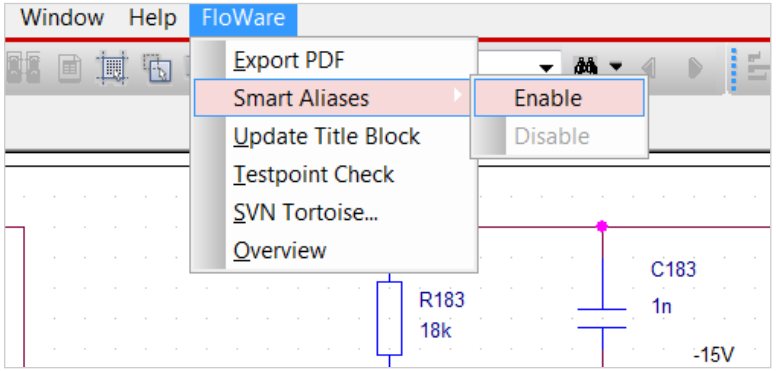


Analog subblock



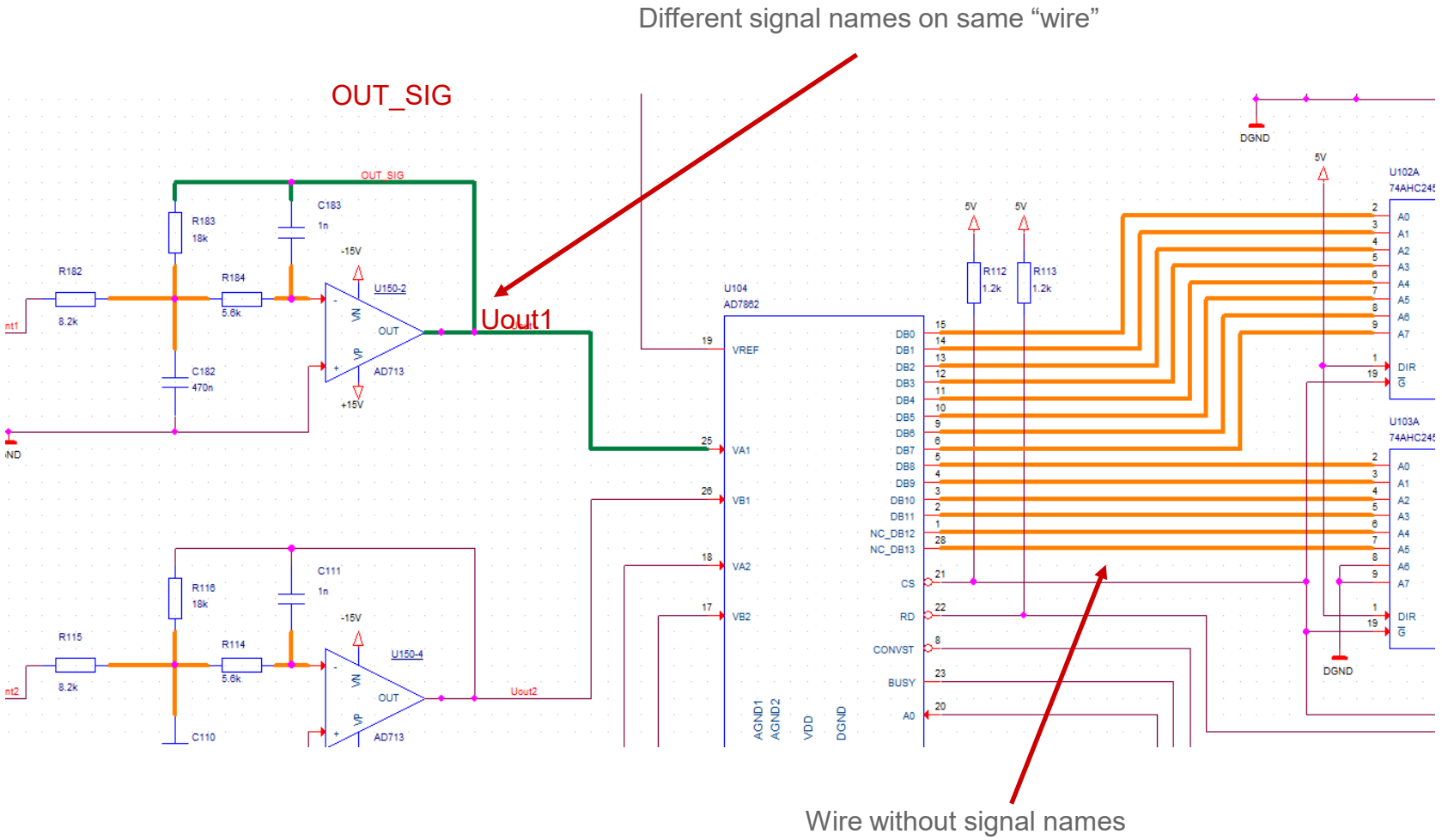
Smart Aliases

- TCL application with smart editing and highlight capabilities when working with user defined signal names (aliases)
- Features
  - Dynamic highlighting of unnamed wires
  - Dynamic highlighting of wires with multiple different signal names
  - Smart rename when editing a signal name



Smart Aliases

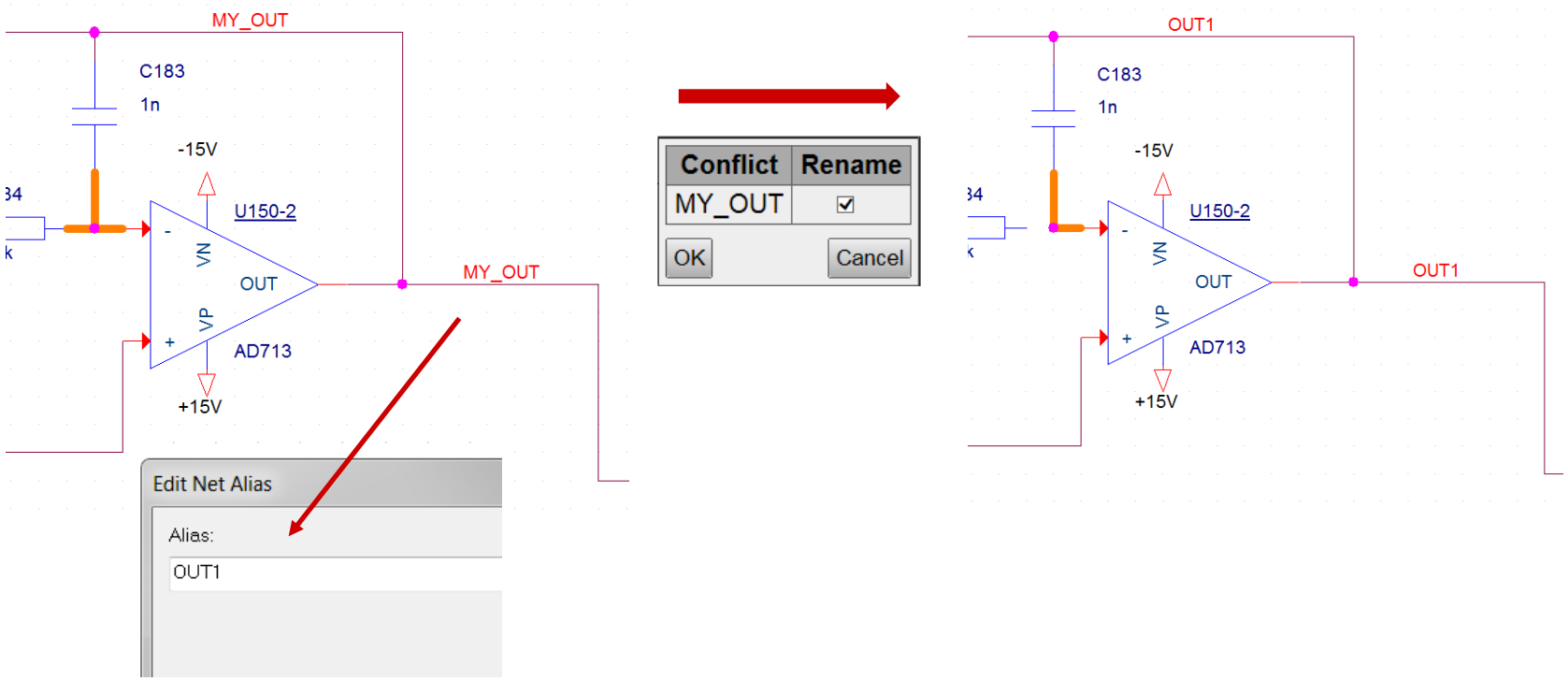
- Dynamic Highlight



Smart Aliases

- **Smart Rename:** Keeps signal names in sync even if signal names have been assigned at multiple locations

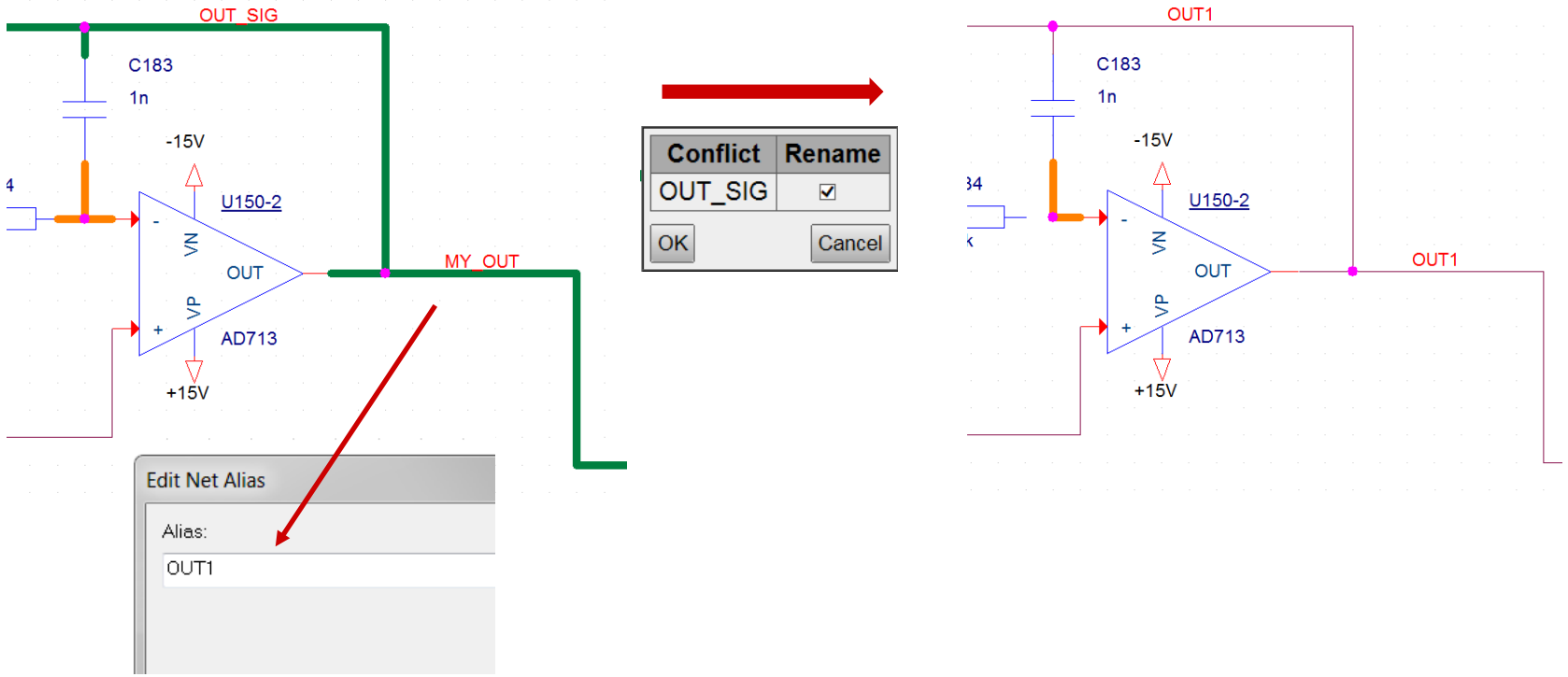
e.g. Rename MY_OUT to OUT1



Smart Aliases

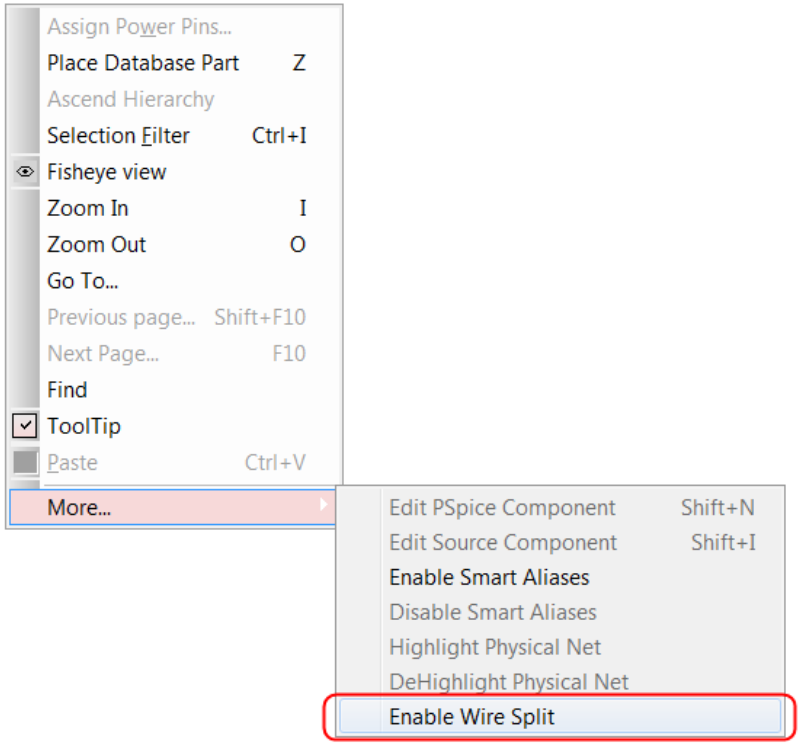
- **Smart Rename:** Even helps resolving conflicts when different signals names were present

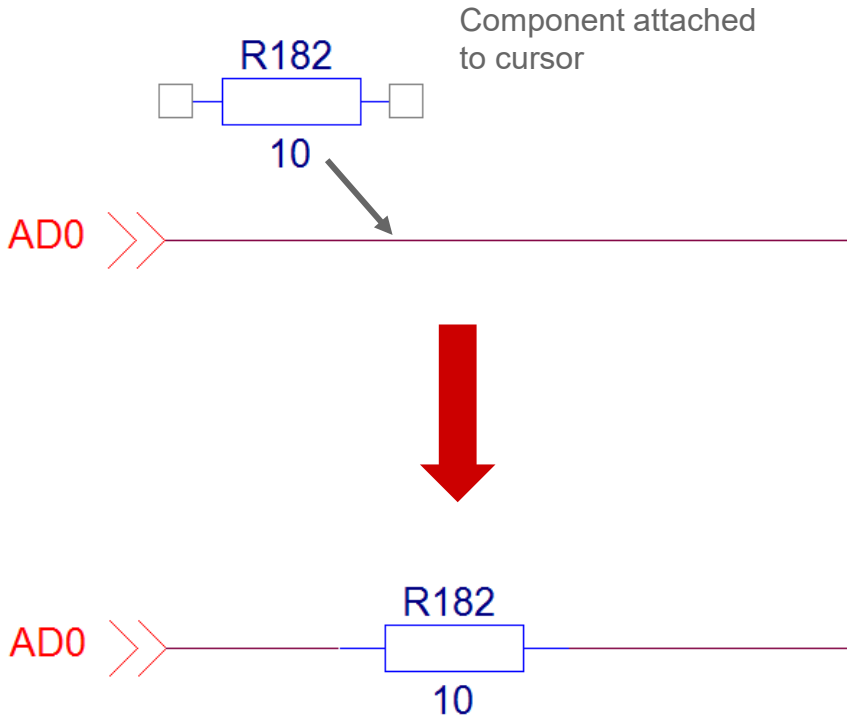
e.g. Rename MY_OUT to OUT1



Split Wire

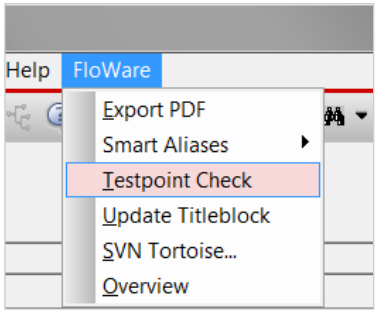
- Provides automatic wire split when components (e.g. resistors) are placed / dropped on wires
- Enable / Disable through context menu

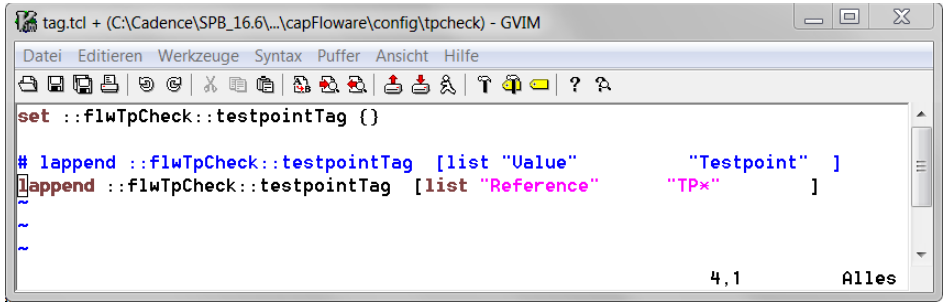


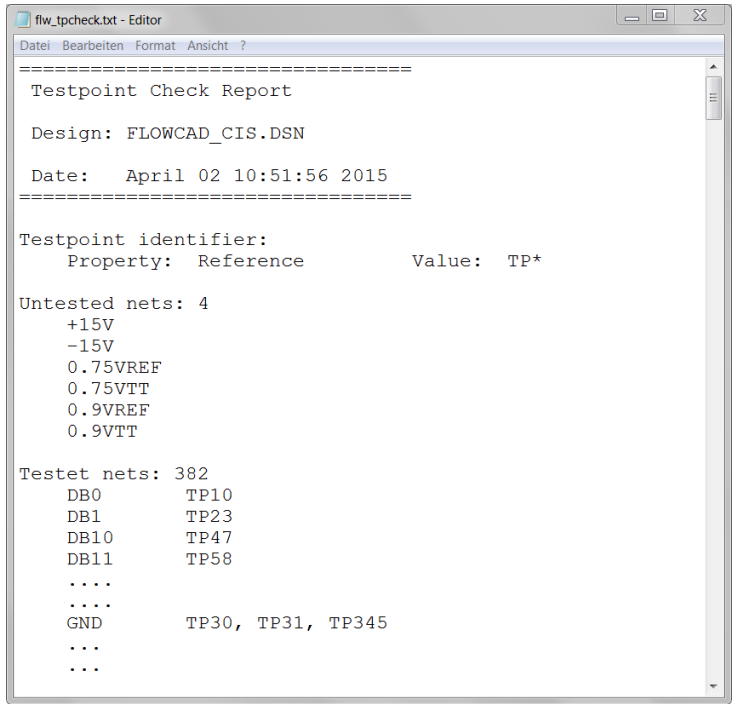


Testpoint Check

- Check testpoint coverage for whole design
- Based on user-defined testpoint components (e.g. One-pin components TP*)
- Configurable search criteria
  - Reference = TP*
  - Value = Testpoint
- Status report

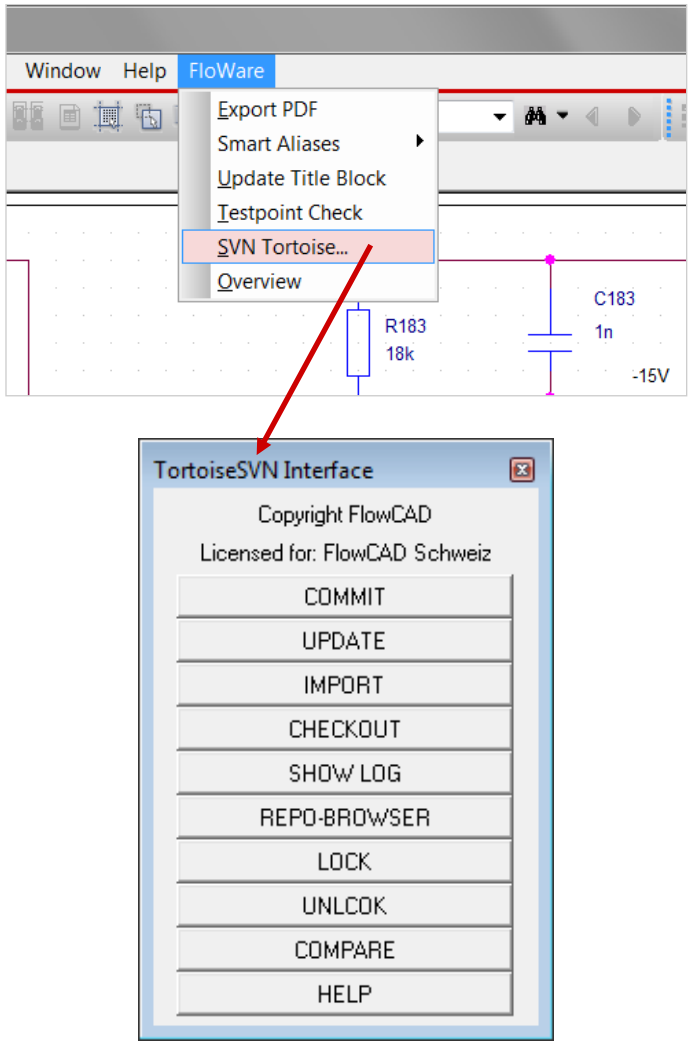






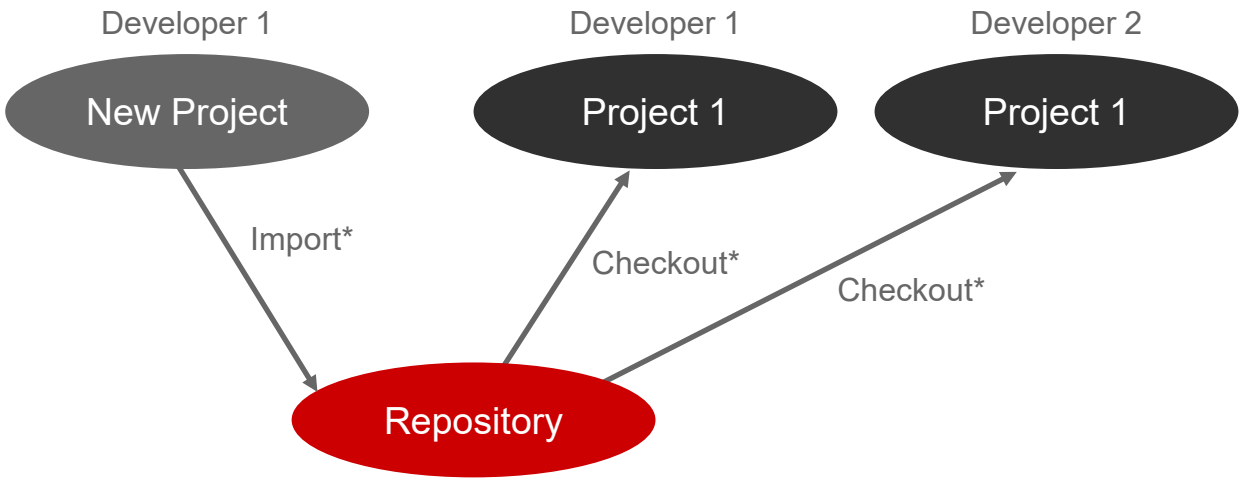
Tortoise SVN Integration

- **Features**
  - Import a project to a SVN directory
  - Committing your project to the server
  - Load the latest project version from the server
  - View the log-file
  - Checkout a directory
  - Lock / unlock a project
  - Compare – **only with CIS license**
  - Each command is directly available in **Capture**
  - This module always use your entire project directory
- **Prerequisites**
  - Tortoise SVN (Open Source)
  - SVN Server (Open Source)



Tortoise SVN Integration

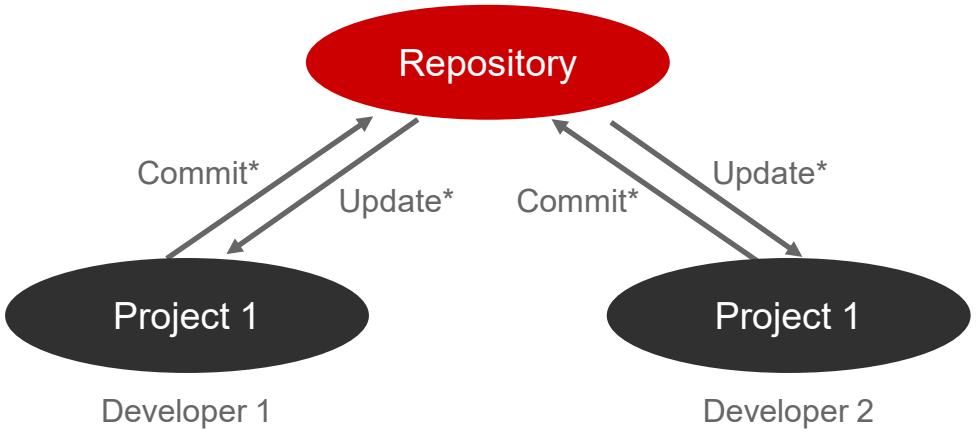
Use model: Creating a new project



* Commands launched from the Capture TortoiseSVN interface

Tortoise SVN Integration

Use model: During the daily use



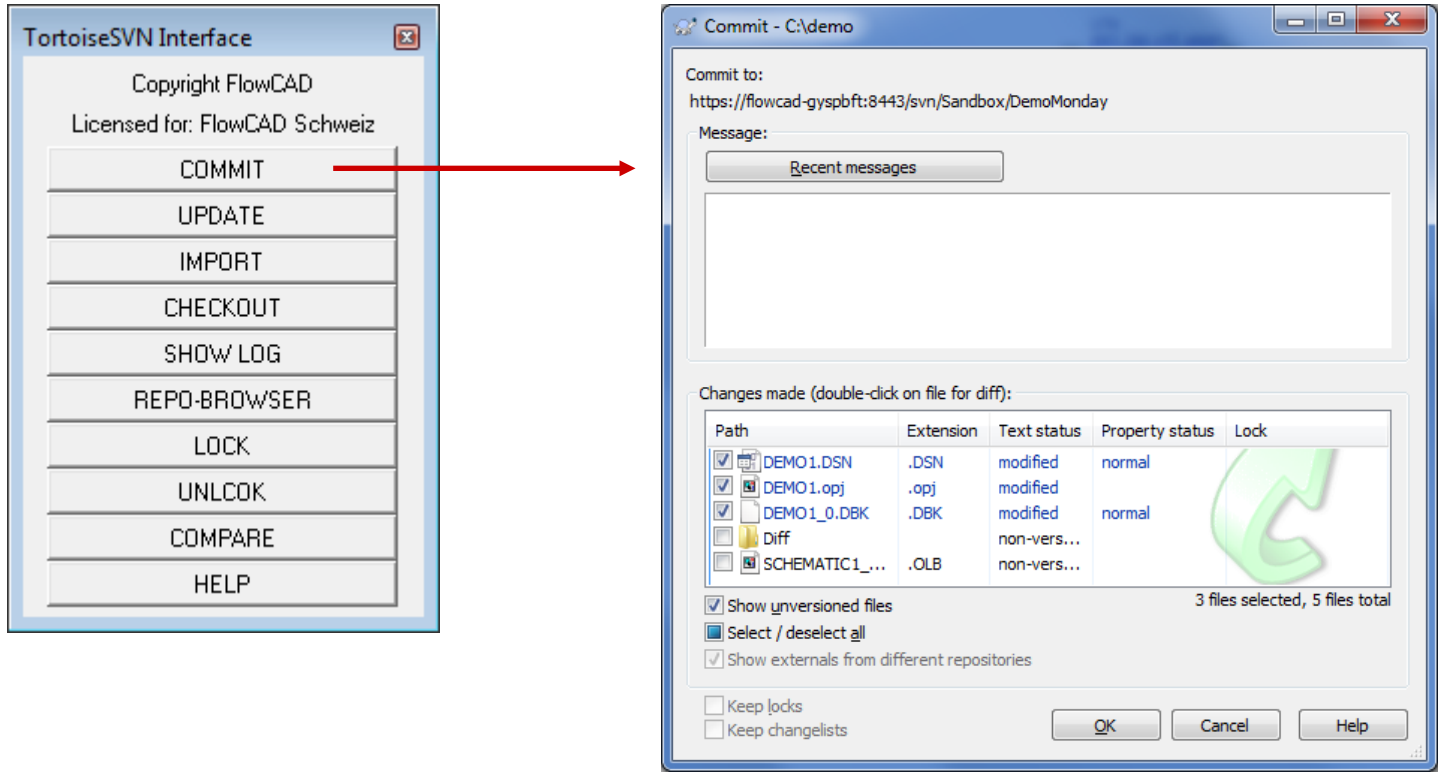
* Commands launched from the Capture TortoiseSVN interface

Stored on the SVN Server

Stored on your personal drive

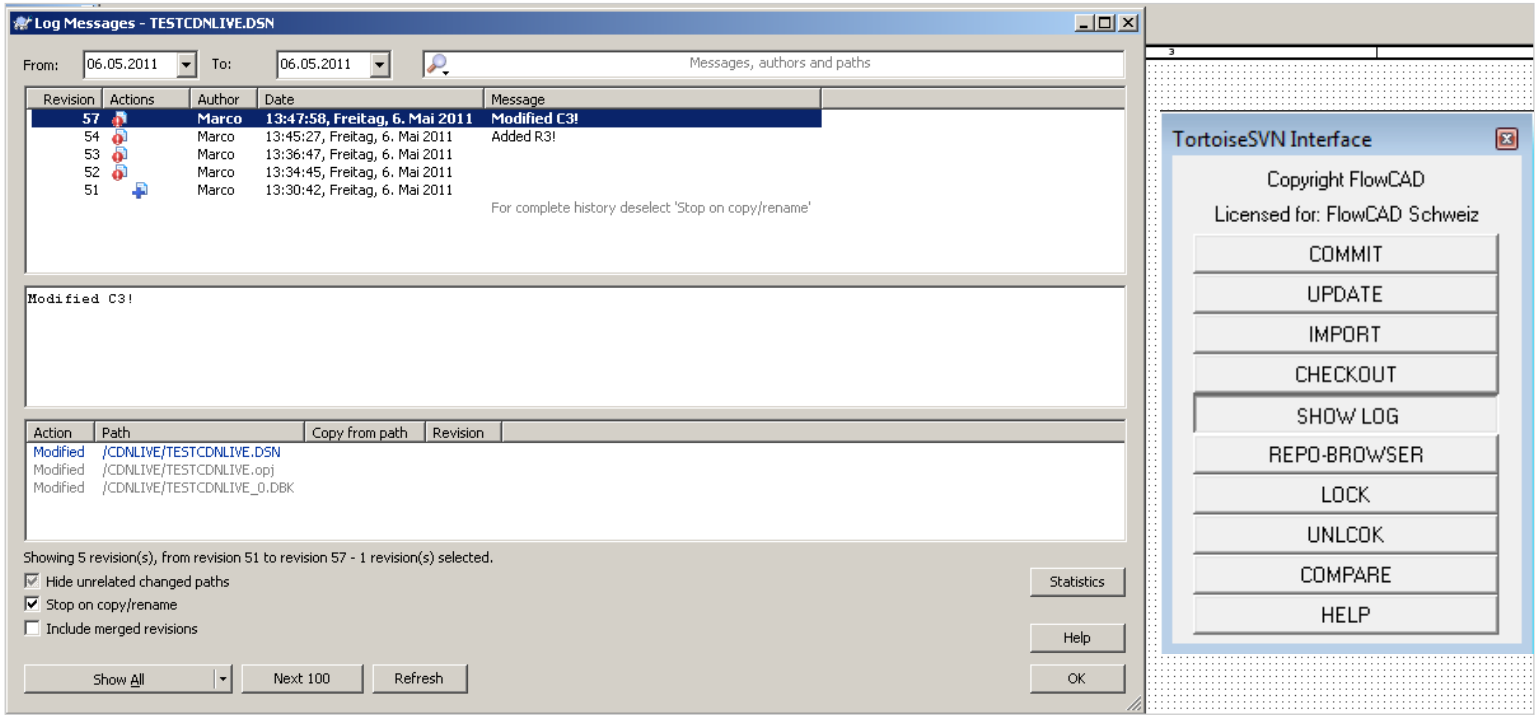
Tortoise SVN Integration

- When committing a project, you can add messages which will be stored on your server, for example:



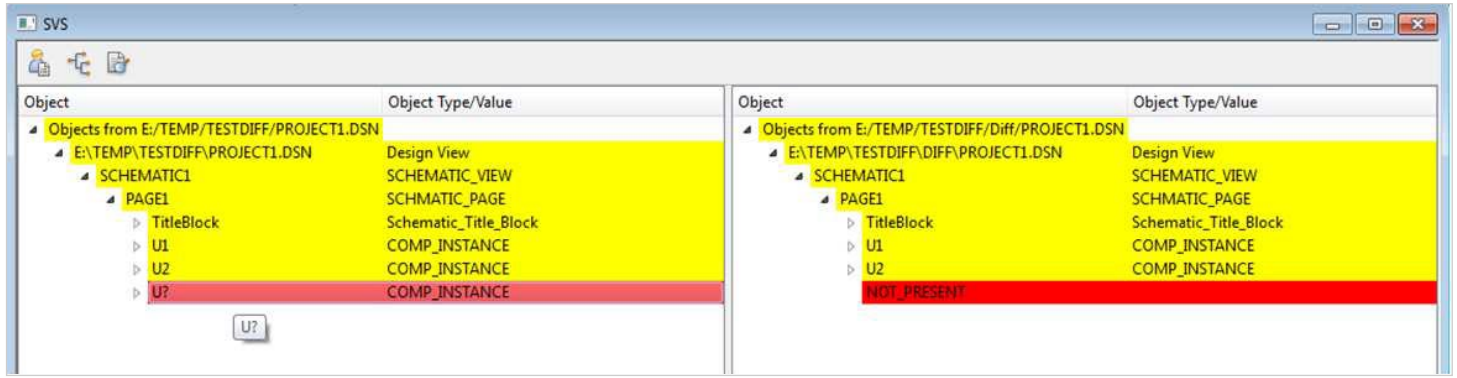
Tortoise SVN Integration

- View the log messages on your project history



Tortoise SVN Integration

- **Design Compare:**
  The latest version from the SVN Server will be compared with your local version



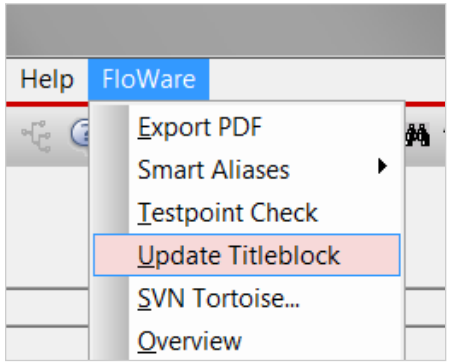
Local version

Version from the SVN Server

- This command works only when you have a CIS license

Update Titleblock

- Automatic update of titleblock properties
- Driven by external configuration file customvar.cfg
- Variant aware



customvar.cfg + (D:...l_Kit\project) - GVIM1

Datei Editieren Werkzeuge Syntax Puffer Ansicht Hilfe

```
[Customvar BASE]
Title=FlowCAD Evaluation Kit BASE
Doc=S30861-Q4711-X-2
RevCode=1.9

[Customvar ASIA]
Title=FlowCAD Evaluation Kit ASIA
Doc=S30861-Q4812-X-3
RevCode=B.4

[Customvar EUROPE]
Title=FlowCAD Evaluation Kit Europe
Doc=S30861-Q4913-X-4
RevCode=1.5

[Customvar USA]
Title=FlowCAD Evaluation Kit USA
Doc=S30861-Q5014-X-r5
RevCode=3.1
```

20,0-1 Anfang

Variant Name = USA

FlowCAD

FlowCAD
München - Zürich - Gdansk
www.FlowCAD.eu

Title
FlowCAD Evaluation Kit USA

Size		Document Number	Rev
A3		S30861-Q5014-X-r5	3.1

Date: Tuesday, March 31, 2015 Sheet 1 of 19

Coffee Break

