

FloWare Modules – Enhancing Productivity

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FloWare Features

- General purpose utilities
 - Functions not in standard tool yet
 - Not written for one specific customer
 - Everybody should benefit
- Easy installation
 - Also casual users must be able to install FloWare
 - No variables
 - Menus will be created automatically
 - Integrates perfectly into existing customizations
- Documentation
 - Full documentation is provided for every module

Tools	FloWare	Help			
€ 🤇	Setup		►	1 🔁 3D 🗄 拱 🌑 🗖 🕯	
	Display		•		
	Edit		•	Advanced Mirror	F
	Draft		•	Anti Tamper Mesh PCB	
	Shapes		•	Change Width	
	Check/R	eview	•	Coil Designer	
	Docume	ntation	•	Contour Place	
	Manufac	ture	•	Cross Copy	
	Signal In	tegrity	•	Derive Via	
	Custom		•	Digital Soldermask	
	Import		•	Label Tune	
	Export		•	Polar Grid 🔹 🕨	
	Miscella	neous	•	Push to Grid	
	Overviev	v		Replace Via	
				Shield Generator	
				Shield Routing	
				Stretch Flex	

FloWare Under the Hood: Skill Interface

- The PCB Editor Skill in Cadence Allegro is a powerful scripting language used to automate and customize tasks within the PCB design environment. It allows users to write scripts that can manipulate design objects, automate repetitive tasks, and create custom functions to enhance the design workflow.
- Key aspects of PCB Editor Skill
 - Automation

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- Customization
- Data manipulation
- User interaction
- No platform dependencies

procedure(my_pp() let((report_file port) ./my_pick_and_place.txt" report_file = port = outfile(report_file "w") fprintf(port "Refdes Footprint Location\n" foreach(cmp ax1DBGetDesign()->components fprintf(port "%L %L %L \n\screw cmp->symbol->name cmp->symbol->xy) close(port) when(isFile(report_file) axlUIUiewFileCreate(report_file "My Report" nil));let);proc

	So My Report
•	, 💉 🗙 📛 🔁 💭 🖶 🕐 Search:
Т1	Refdes Footprint Location
	"B700" "NET_SHORT" (<u>59.9 16.7</u>)
	"B750" "NET_SHORT" (<u>161.0 30.0</u>)
2 ∕os⇔ * ,	"B100" "NET_SHORT" (<u>124.2 88.9</u>)
	"Y800" "CRY_MA306" (<u>108.179 20.404</u>)
	"X205" "USB3A_FEMALE" (<u>94.2 10.2</u>)
(C123	"X200" "PCI EX X4 RA" (<u>127.385 2.156</u>)
\ +	"X104" "SMB 90" (<u>183.92 210.16</u>)
	"X103" "SMB 90" (<u>183.92 201.56</u>)
Demo Des	"X102" "SMB 90" (<u>183.92 183.46</u>)
	"X101" "SMB 90" (<u>183.92 192.36</u>)
	"X100" "ZIF12 FLEX" (<u>104.0 72.0</u>)
Command	"X1" "HEADE2X10" (<u>51.1 10.6</u>)
Pick first element	"U801" "BGA665 26X26 10" (<u>115.2 47.9</u>)
Pick first element.	"U800" "TSOP20 0 65X5 90" (<u>117.7 20.4</u>)
Pick first element.	"U750" "MLPQ24" (<u>139.5 21.2</u>)
Pick first element. Pick first element.	"U700" "MLPQ24" (<u>81.4 25.5</u>)
pp	"U603" "FBGA82 11X13 08" (<u>148.0 82.0</u>)
No element found.	"U602" "FBGA82 11X13 08" (<u>148.0 68.0</u>)
Command >	"U601" "FBGA82 11X13 08" (148.0 54.0)

Getting Started with Skill

- Start an interpreter window by typing set TELSKILL and start talking with the database
 - No compiling necessary
- Write some commands e.g.
 printf("Hello world\n")
- Refer to documentation axl API, which give you a list of commands which allow you to access information from the database
- Extend your skills with Skill by testing, writing, checking etc. Be curious!



C:\Cadence\SPB_23.1\share\pcb\examples\skill\DOC\FL	INCS	
^{Name} ▲ ■ axlGetMetalUsageForLayer.txt	Größe 1 1.93 KB 1	^{Typ} Fext
axlImpdedanceGetLayerBroadsideDPImp.txt	1,021 Bytes 1	ſext
axllmpdedanceGetLayerBroadsideDPWidth.txt	1 KB 1	ſext
axlImpdedanceGetLayerEdgeDPImp.txt	847 Bytes 1	ſext
axlImpdedanceGetLayerEdgeDPSpacing.txt	907 Bytes 1	Fext
axlImpdedanceGetLayerEdgeDPWidth.txt	927 Bytes 1	Fext
axllsEtchLayer.txt	623 Bytes 1	ſext
axllsLayer.txt	451 Bytes 1	ſext
axllsLayer la egative.txt	625 Bytes 1	ſext
axllsVisibleLayer.txt	504 Bytes 1	ſext
axlLayerCreateCrossSection.txt	1.59 KB 1	ſext
axlLayerCreateNonConductor.txt	548 Bytes 1	ſext
axlLayerDelete.txt	1.49 KB 1	ſext
axlLayerExternal.txt	605 Bytes 1	ſext
axlLayerGet.txt	1.12 KB 1	ſext
axlLayerPriorityClearAll.txt	443 Bytes 1	ſext
axlLayerPriorityGet.txt	1.25 KB 1	ſext
axlLayerPriorityRestoreAll.txt	476 Bytes 1	ſext
axlLayerPrioritySaveAll.txt	573 Bytes 1	ſext
axlLayerPrioritySet.txt	2.73 KB 1	ſext
axlLayerSet.txt	1.27 KB 1	ſext
axlLayerViaLabel.txt	649 Bytes 1	ſext
axlPadOnLayer.txt	1.19 KB 1	ſext

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FloWare Modules PCB Editor

- Advanced Mirror ٠
- **Advanced Testpoint Check** .
- Anti Tamper Mesh PCB
- **AOI Check**
 - Assign Net to Via
 - **Barcode Generator** ۰
 - Batchplot ۰
 - CAF-DRC
 - Change Width
- **Class Color**
- **Cleanliness Check**
- **Coil Designer**
- **Contour Place**
 - Cross Copy
 - **Cross Section Generator** .
 - **Custom Variables** .
 - **Design Compare**
- **Digital Soldermask**
- **Drafting Utilities**

- Drawing Designer (legacy)
- **Drawing Size** •
- **Drawing View Manager** •
- Edge Plating •
- **FPGA** Utilities •
- Highlight Dummy Pins •
- **IBIS** Prototype Modeler •
- Label Generator •
- Label Tune •
- Mask Generator
- NC Panel Route •
- Net Color View
- Net Min Gap
 - Padstack Finder
 - Padstack Usage
- Panelization
 - PCB Library Plot
 - **Polar Grid Utilities** •
 - Post Processing

- Push to Grid
- Quick Symbol Edit
- Replace Via
- Shape Utilities
- Shield Generator
- Shield Routing
- Silkscreen •
- Snap Generator
- SVG Export
- Svnchronize Testprep

Videos available on

- Variant 3D
- Variant Assembly
 - Variant BOM
 - Z-DRC

YouTube



Advanced Mirror

- Enables mirror operations while moving or copying elements
 - Mirror across subclasses (Geometry and Layer)
 - Mirror on the same subclass (Geometry only)
- Including placement and routing
- Selection through window or single pick, dynamic preview
- Special handling for symbols, vias and text in Geometry only mode





Advanced Testpoint Check

- Addresses various rules for testpoint checking
 - Testpoint to Testpoint check
 - Testpoint to Component check taking component height into account
 - Visualization of restriction areas
 - DRC marker generation

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- Constraints reuse through configuration files







Advanced Testpoint Check

- Spacing rules may be specified
 - As fixed spacings

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- Using rulesets, which account for component height





Anti Tamper Mesh PCB

• Useful for Hardware Security Modules (HSM)

 In order to actively detect and respond to external attacks a convoluted maze of wires (mesh) can be used to monitor changes in resistance, capacitance, breaks, shorts etc.

• Features

- Number of signals, width, spacing, ...
- Region select, keepouts, destination layer, ...
- Randomness







AOI Check

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- Helps users to check AOI related rules directly in PCB Editor
- Shadowing can cause serious issues in verification process

D		D:
Parameters Camera angle	19.00	Diagram
Direction	All 👻	0
		h h
General Como boundary	lace_Bound 🔻	Shadows
General Comp boundary P Derive height from sym	lace_Bound •	Shadows Image: state st



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AOI Check

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 Shadows can be calculated in various directions based on specified camera angles taking component height into account



• Special rules apply to 3D inspection systems





Assign Net to Via

- Enables users to change the net on existing vias
- No need to delete and route new ones
- Use model

- Select net from list (including wildcard support) or by context RMB > Pick Net
- Click on one or more vias
- Choose RMB > Done to confirm









Assign Net to Via

Example





Barcode Generator

- Prints barcodes on a PCB layer as part of the manufacturing process
- Supporting definitions
 Code 39, Code 128, QR Code and Data Matrix
- Adjustable parameters corresponding to selected code
- Additional drawing options (e.g. show text, inverted display)
- Dynamic preview during parameter change
- Parameter preset through configuration file





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		Setu Disp Edit Draf Shap Chec Docu Man Sign Custo Misc Over	p lay t k/Review umentatic ufacture al Integrit om ellaneous view	k k k k k y k k		Barco Cross Custo Displ Draw Padst PCB I	ode s Sect om Va lay La tack L Libran	ion ariable bel Te Jsage y Plot	s • xt er	Code 39/128 QR Code Data Matrix	23
						Varia	expoi int As	rt sembly	y		





Barcode Generator



对 Barcode Gene	erator Code39/128 📃 🛛 🔀
General Text	CADENCE
Class Subclass	BOARD GEOMETRY
Specification Code 39	Ode 128
Barcode Size Barcode hei Barcode wid Min bar widt Margin Top/ Margin Left/	ght 10.000 th 19.040 Fix value h 0.170 Fix value Bot 2.000 Right 2.000
Misc Embed tex Invert struc OK	t into barcode using block 4



🕻 Barcode Generator QR-Code 📃 🖂
General
Enter text manually
http://www.cadence.com
© Read from file
Class/Subclass
BOARD GEOMETRY V ASSEMBLY_NOTES V
Encoding Version 3 → (29 × 29) ▼ Ecc level M ▼ Drawing Unit size 0.30 ▼ Invert structure Merge shapes
Info Capacity: Numeric: 101 Alphanumeric: 61 Bytes: 42 Text status: Chars: 22 Type: byte
OK Status Place Help



Enter text	manually
http://ww	w.cadence.com/welcome.html
Read from	n file
Class/Subcla	ass
BOARD GE	EOMETRY - / ASSEMBLY_NOTES
Options	
Size	AUTO Process tilde
Encoding	
Lincounity	
Drawing	
Unit size	0.30 V Invert structure
	U.6U Merge shapes
Margin	



- Creates documentation
 - Fully automated
 - Multipage or single page files
 - Visibility control based on views (color views as well as artwork views), similar to visibility panel
 - Order of view items can be changed by user
 - Plotsets allow grouping views into separate PDF files
 - Load and save configuration to disk
 - Three modes
 - PDF Export from Allegro / OrCAD PCB Editor
 - HTML Export
 - Batchplot (legacy)





- Multiples viewsets can be defined
- A viewset may contain
 - Film records

- ...

- Color views (!!)
- Each viewset corresponds to one PDF file to be generated – Name of the PDF file can be specified (output)
- Each viewset may reference a profile to be used during PDF export
 - E.g. black white print only
 - With / without meta data
- Single push button to generate all data ...



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Options

Mode



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Setup Viewsets for PDF Export

- Use context menu in tree view
 - Rename
 - Edit
 - $-\operatorname{\mathsf{Add}}$
 - Delete
- Edit views
 - Select film views
 - Select color views
 - Change order



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Other Modes

- HTML Export
 - Generates an HTML report including SVG graphics
 - Setup regarding viewsets and profiles similar to PDF Export
- Batchplot (legacy)
 - Selecting Setup will launch the existing / legacy application
 - Still available and supported

科 Publisher				×
Options				
Mode	PDF Export	×		
Configuration	PDF Export HTML Export Batchplot			
Export to director	у			_
Export	Close		Help	





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Final document opened with Acrobat Reader



CAF-DRC

- Special DRC for Conductive Anodic Filaments (CAF) on PCBs
- Performs Hole-to-Hole clearance checks along the fiber structure
- Based on voltage classification
- Adjustable fiber orientation





CAF-DRC

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• Use model

- Classify nets by voltage property or by spacing net class
- Launch application
- Specify rules and select mode to be used
- Export / import rules for reuse purposes
- Run DRC

🚰 Allegro Constraint Manager	(connected to A	Allegro PC	B Designer (was Performance L)	16.6) [cafdrc_by_net_voltage] -
<u>File E</u> dit <u>O</u> bjects <u>C</u> olum	n <u>V</u> iew A <u>n</u> aly	ze <u>A</u> udit	<u>T</u> ools <u>W</u> indow <u>H</u> elp	cā
axonq	Man ADD	RESS	✓ 1/2 1/2 1/2	🌆 🐔 🦾 🖦 🗯
Worksheet selector	ф ~ X	cafdr	c by net voltage	
Electrical		Curu	c_by_net_tokuge	
+ Physical			Objects	Voltage
Spacing		Туре	S Name	v
Same Net Spacing		*	*	*
Properties		Dsn	cafdrc_by_net_voltage	
R Net		Net	P12V	12 V
		Net	VCC	5 V
General Properties		Net	AGND	0 V
Ratsnest Bundle Prop	perties	Net	N12V	-12 V
🖻 🗁 Component		Net	UNNAMED_1_2N4339_6	6P_S
庄 🌆 Component Properti	es	Net	UNNAMED_1_2N4339_6	6P_D
Pin Properties		Net	UNNAMED_1_2N2222_6	P_E
		Net	UNNAMED_1_2N2222_6	P_C
		Net	UNNAMED_1_2N2222_6	P_B
		Net	UNNAMED_1_1N4148_1	1P_CAT
		Net	UNNAMED_1_1N4148_1	1P_AN
		Net	UNNAMED 1 1N4148 9	PCAT





CAF-DRC

Results

- DRC markers in PCB Editor and Constraint Manager including cross probing
- Visualization of DRC polygons on DRAWING FORMAT subclasses CAFDRC_DV1, _DV2, DV3 and _DV4
- Handles all drill and slot types

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Change Width

- · Change the width of clines and clines segments
- Supporting a filter mechanism in that the changes are only applied to segments matching a given width
- Select by Pick, Window, Temp Group or Find By Name
- Highlight and report functionality including cross probing

Segment Rep	ort			X
	? Search:	Match word Match ce	ise	
Width	Start	End	Layer	
1.0	(144.5 26.8)	(144.5 27.875)	ETCH/TOP	
1.0	(139.25 28.25)	(139.25 24.65)	ETCH/TOP	
1.0	(137.7 26.8)	(137.7 28.3)	ETCH/TOP	
1.0	(140.8 27.975)	(140.8 26.8)	ETCH/TOP	
1.0	(137.45 19.2)	(136.152 19.2)	ETCH/TOP	
1.0	(137.525 19.275)	(137.45 19.2)	ETCH/TOP	
1.0	(130.4 26.9)	(130.4 28.075)	ETCH/TOP	
1.0	(134.1 28.05)	(134.1 27.05)	ETCH/TOP	
1.0	(135.8485 19.1)	(135.5 19.1)	ETCH/TOP	
1.0	(135.8704 19.1146)	(135.8485 19.1)	ETCH/TOP	
1.0	(136.007 19.1712)	(135.8704 19.1146)	ETCH/TOP	
1.0	(136.152 19.2)	(136.007 19.1712)	ETCH/TOP	
1.0	(132.1 19.2)	(133.6 19.2)	ETCH/TOP	
1.0	(135.5 19.1)	(135.4 19.2)	ETCH/TOP	
1.0	(133.6 19.2)	(133.6 17.9)	ETCH/TOP	
1.0	(135.4 19.2)	(135.4 17.4)	ETCH/TOP	
1.0	(87.3 27.5)	(88.8 27.5)	ETCH/TOP	
1.0	(87.3 28.8)	(87.3 27.5)	ETCH/TOP	
1.0	(90.5 19.8)	(90.5 18.625)	ETCH/TOP	
1.0	(86.8 18.65)	(86.8 19.65)	ETCH/TOP	
1.0	(85.5 27.5)	(83.4 27.5)	ETCH/TOP	
1.0	(85.5 29.0)	(85.5 27.5)	ETCH/TOP	
1.0	(81.65 18.45)	(81.65 22.05)	ETCH/TOP	
4				► [



🔽 Enable On-Line DRC



Class Color

- Enables users to color spacing net classes for review and documentation purposes
 - Color chooser
 - Legend support
 - Settings stored in database
 - Export / import settings

Legend Generate/Update legend Text block	ock 5
CLASS	COLOR
HIGH VOLTAGE	
PE	
POWER	
SECONDARY	
SWITCH	

	Provine Net Class	Color	1	1
	Spacing Net Class	Color		
1	HIGH VOLTAGE			
2	PE			E
3	POWER			
4	SECONDARY			
5	SWITCH			
.ege	end			
.ege	end Generate/Update legend Text bloc	k 5		
_ege Conf	end Generate/Update legend Text bloc iguration	k 5		
_ege Conf	end Generate/Update legend Text bloc iguration Save to file Load	k 5 from file		



Assign	Color				
					Γ
Nex	d >>			Ca	incel

Cleanliness Check – Technical Cleanliness

- Technical Cleanliness refers to the performance of components, assemblies and systems related to particle contamination in automotive and other applications
- On PCB's such particles (e.g. conductive particle from aluminum cover) may cause short circuits
- The probability failure depends on
 - Particle size
 - Contact area size
 - Number of contact areas
- For more information refer to document ZVEI Guideline for Technical Cleanliness from <u>https://www.zvei.org/</u>





Technical Cleanliness

- Analyzes the PCB layout for contact areas caused by particles with a given size
- The contact area specifies the area in which a particle will cause a short, no matter how the particle is oriented
- Cleanliness Check calculates and visualizes contact areas using shapes and writes a report
- By sweeping the particle size the information from the output can be used to feed cleanliness assessment calculator from ZVEI

Cleanliness Check	- 🗆 X
General	
Particle size	1.0000
Side	Тор 🔻
Min shape aperture	0.0050
☑ Merge contact area shapes	
🗹 Enable data tiling	2.00
☑ Ignore small voids	20
Subtract open copper	
Create DRC	
Misc	
Clear 👻	Report
Close Run	Help 🔻
Range is 0.0000 to 1000.0000	





Technical Cleanliness

- Menu button Report
- Particle count per layer
- Short Area

- Sum of particle shape areas from layer CLNS_CONTACT_TOP (BOTTOM)
- Short Area
 - Shape area on merged layer CLNS_RESULT_TOP (BOTTOM)
- Design Area
 - Area from **DESIGN_OUTLINE** minus **CUTOUT**



🔀 Cleanliness Report					
🔎 🗙 🗁 🖡	🔒 실 🥝 Search:		Ġ 🌖 🗐 Match word 🗐 Match		
Cleanline	ess Report:				
Design: Date:	board04.brd May 21 13:39:56	2019			
Units:	MM				
Units:	MM ParticleCount	ShortArea (sq mm)	ShortAreaMerge (sq mm)		
Units: TOP	MM ParticleCount 295	ShortArea (sq mm) 69.748	ShortAreaMerge (sq mm) 68.980		
Units: TOP BOTTOM	MM ParticleCount 295 129	ShortArea (sq mm) 69.748 24.221	ShortAreaMerge (sq mm) 68.980 24.041		



- Includes useful functions when designing planar spiral inductors on a PCB
- Support for different spiral pattern
 - $-\operatorname{Round}$

- Rectangle
- Octagon
- Hexagon
- Features
 - Parameterized input in terms of width, spacing, number of turns, etc.
 - Support for rotation, flipping and scaling
 - Dynamic preview during parameter change

riound rie	ectangle	Octagon Hexagon			
Parameters			Diagram		
Width	1.000	Spacing 1.000			
Diam X	6.000	Rotation 0.00			
Turns	3			Spacing Width †	
Scale	1.000	Clockwise	Diem X		
Calculated	Extents:	18.000 × 17.000			
Calculated General	Extents:	18.000 × 17.000	Miscellaneous		
Calculated General Create coil or	Extents: n subclass	18.000 × 17.000	Miscellaneous	VIA	
Calculated I General Create coil or	Extents: n subclass keepout	18.000 X 17.000	Miscellaneous Add pad at start Add pad at end	VIA	*
Calculated General Create coil or Add route	Extents: n subclass keepout Subclass	18.000 × 17.000	Miscellaneous Add pad at start Add pad at end	VIA VIA	
Calculated General Create coil or Add route	Extents: n subclass keepout Subclass Offset	18.000 × 17.000	Miscellaneous dd pad at start dd pad at end Convert structure to Endcap style:	VIA VIA shape	*
Calculated General Create coil or Add route	Extents: n subclass keepout Subclass Offset	18.000 × 17.000 TOP • ALL • 0.000	Miscellaneous Add pad at start Add pad at end Convert structure to Endcap style: Inner Round V	VIA VIA shape Start/End Roun	* * d



Basic spiral patterns

Round

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Octagon



Rectangle



Hexagon





Rectangle spiral with corner modifications

Mitered corners

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Parameter Width	0.500	Spacing 0.500			Miter
Diam X	10.000	Diam Y 5.000		t t	
Turns	4	Rotation 0.000		Diam Y	widtl
Scale	1.000	Clockwise	◄	Diam X	-•••
🖌 Change	e corner		11		
Style	Miter 🗸	Size 1.000		ŧ	
Calculater	d Extents	18 000 × 12 000			



Rounded corners







• Other features

- Realization as a combination of cline segments or one single shape
- Addition of padstacks to the start / end points
- Automatic generation of route keepouts in the inner area





Contour Place

- Interactive placement along contour
 - Automatic snap to contour path
 - Place, Place & Spin, Spin
- Various alignment options
 - $\mbox{ Lock long side}$
 - Lock short side
 - Relative
 - Absolute
- Custom snap marker
 - For accurate control
 - Manual markers
 - Markers by intersection
 - Equidistant markers



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Contour Place

• Alignment options



Options		-	ð	×
Options				
Snap to mar	kers			
Mode				
Rotation type	Absolute 🔻			
Angle	Lock long side			
	Lock short side			
Object pick	Relative 😼			
	Absolute			
Custom markers —				
Spacing	5.0000			
Quantity	5 -	+		
Marker size	0.5000			







Cross Copy

• Problem

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- Customer needs to move objects from one class / subclass to another
- Command Edit > Copy does not support a destination layer
- Customer gets error messages, e.g. E Changing shape to a different class is not supported
- Customer has to find workarounds (e.g. export subdrawing, text edit clipboard file, import subdrawing)
- Solution
 - Cross Copy closes the gap
 - Can move or copy objects to any destination layer for various purposes
 - In contrast to Create Detail, objects are not destroyed (e.g. text will stay text!)

General:	
Destinatio	on class/subclass:
Board	Geometry 🔻
Ass	embly_Notes 🔹
Dele	ete original objects
Processing	options
Shapes:	
Type 🛛	Filled Shape 🔹 🔻
Voids 🛛	nclude 🔹
Clines/line:	s:
Conv	ert to shape
Endcap	style Round 🔻
Pins/vias:	
Mode	Pads only
Figures (sta	and-alone):
Mode 🛛	Filled Shape 🛛 🔻
Advanced:	
Merge	e all
Merge	e by net
	Toggle Layers



Cross Copy

- Advanced features
 - Shape processing
 - Include / exclude voids
 - Fill or decompose with / out voids
 - Unfill shape
 - Clines / lines processing
 - Can be converted to shape
 - Various endcap types
 - Padstack processing (pins and vias)
 - Drawn as shape on destination layer
 - All visible layers are merged
 - Resulting pad shape can be voided by drill hole information
 - Merging support
 - Selected data (find filter settings) is merged










Cross Copy

Example: Merging data to soldermask shape









Cross Copy

Example: Converting pseudo shapes (stroked lines) to real shapes



General:
Destination class/subclass:
Etch -
📕 🛛 Тор 🔹 👻
Delete original objects
Processing options
Shapes:
Type Filled Shape 🔻
Voids Include 🔻
Clines/lines:
Convert to shape
Endcap style Round -
Pins/vias:
Mode Pads only
Figures (stand-alone):
Mode Filled Shape 🔻
Advanced:
📝 Merge all
Merge by net
Toggle Layers



Note: Typical situation after importing third party Gerber data into Allegro – copper needs to be reanimated!!!



Cross Copy

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Example: Backup data on Board Geometry / Assembly_Notes for documentation purposes





- Enhanced support for rigid-flex applications
- Customizable content
 - Custom charts with more meaningful visualization
 - Layer attributes, order, ...
 - Colors, fill styles, ...
 - Vias, stacked vias, backdrill and embedded status support
- SVG export

- Export graphics for documentation purposes
- Configuration stored in db
- Automatic update

Available Content Layer ID > Number Type > Name Name Up PRIMARY Stackup Tol Plus Down PRIMARY Stackup 1 Tol Plus Include Options FLEX Stackup Reset Vias Drawing options Embedded Setup	Chart BUILDUP	~	Add Delete
Backdrill	Available Layer ID Number Type Name Material Thickness Tol Plus Tol Plus Tol Plus Tol Plus/Minus PRIMARY Stackup FLEX Stackup	Jup Down < Reset	Content Number Name PRIMARY Stackup FLEX Stackup PRIMARY Stackup 1 Include Options Vias Stacked vias Embedded Setup Backdrill





- Content can be defined for each stackup from cross section individually
- Also symbols can be placed individually







- A custom chart let's you combine stackups in an arbitrary order
- Feature many customer were asking for ...
- Additional information (vias, stacked vias, etc., can be applied to each stackup item individually)







• Backdrill support



etup			
Chart PRIMARY	Y ×	Add Delete	
Available		Content	
Layer ID		Number	
Number	>	Stackup	
Type Namo		Material Thickness	
Material	Up	THICKIESS	
Thickness			
Tol Plus	Down		
Tol Plus/Minus			
Stackup	۲		
	Deret	Include Options	
	Reset	Vias	
		Stacked vias	
		Embedded Setup	
Drawing options		✓ Backdrill	
OK Diasa	-> Lindato	More -> Heln	



• Embedded component support







• Various drawing options

		Style
		Design OSVG Export
		Conductor
V Cross Section Generator	- 🗆 X	Conductor Dielectric
Symbol	Style	Mask Via Dia
Symbol width 2000.000	Design OSVG Export	Drill span Backdrill Embedded status
Row spacing 0.000	Conductor	Text
Column spacing 80.000	Color	Spacing 20.000
Text block 4	Shape Fill 🔨	
Text block title 4	Width 4.000	
Proportional thickness	Spacing 20.000	
Type Log5 ~	Fix height 80.000	Shape Fill V
Min height 80.000		Width Hatch both
ОК	Help	Spacing Hatch neg



• Export SVG

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- Mainly for documentation purp
- Separate color profile can be c

Style

🔿 Design

Mask

Color

Shape

	S	Generat	ed by PCE	B Editor	×	+						-			\times
on purposes	< ·	\rightarrow (0	Datei D	:/Develo	oment/Pro	jects/XS	Section/F	PRIMARY	.svg		Q	☆	θ	:
an be defined	STAC	pps 🚦	🎍 Chapt	er 26. Datan	na 🧇	FRITZ!Box	🦚 Sh	aring Link	Validat	W	Dokumenttype	defini			»
		1-2	2.3	3.4	4-5 5	а-е	6 0	VS:1-5	VS:1-8						
More -> Heln	1										FR-4	0.012 MM 0.030 MM 0.203 MM			
Save settings Load settings Export SVG	2										COPPER FR-4 COPPER	0.030 MM 0.203 MM 0.030 MM			
	4				-						FR-4 COPPER	0.203 MM 0.030 MM			
Design	5										FR-4 COPPER	0.203 MM 0.030 MM			
lask v	6	-	-71		-						FR-4 COPPER FR-4	0.203 MM 0.030 MM 0.203 MM			
blor Fill V	7										COPPER FR-4	0.030 MM 0.203 MM			
Width 4.000	8	7-8	6-7	ů v							COPPER POLYIMIDE	0.030 MM 0.012 MM			
Spacing 20.000					PRIMAR	Y: 1.690 MM									



Custom Variables

- User defined variables in PCB Editor, useful for title blocks, etch texts etc.
- Similar to Design Entry HDL
- Automatic update of variables across all subclasses
- Variant support

- History capabilities
- Variable values can be sourced from external control file or even cpm-file

	Edit cont	ext USA 💌	Add Limit View	
	Туре	Name	Value	1
1	С	DOC_NO	W30861-Q6789-MFG	
2	С	PROJECT	PN-5916-X-3	
3	С	TITLE	Control Unit	
4	С	VARIANT_NAME	USA Version	
	•			•
)ptions		Specify	Filter display	•
)ptions Layer Visibil	• Mapping ity	Specify Show All Hide All	Filter display Name *	×

	Title <mark>Co</mark>	ntr	οI	Unit						
-	Project <mark>PN</mark>	- 59	16-	X-3						
-	Doc No. <mark>W3</mark>	086	61-C	6789	-1	MFG				F
-	Variant <mark>US</mark>	ΑV	ers	ion						
-	Size A3	so	ale	1:1		Page	1	o f	4	
	7					8				



Custom Variables

Define Placeholders

Parameters
Variable name:
PART_NUMBER
Display value:
<part_number></part_number>
Destination layer
Drawing Format 🔹
☐ Title_Block
Attributes
Block 3 🚔 Rot 0.0000
Align Left 🔻 Mirror No 💌
Advanced
Type Standard 🔻
History None 🔻
Mode
Add placeholder
C Modify placeholder
🔘 Delete placeholder

Update Example

Сa	dence De	sign	Sу	stems		Title	Control Unit
B.4	RTM			10/31/15	RNICK		
A.2	Outline mod	ificati	on	02/18/15	BWILKE	Project	PN-4815-X-1
A.1	Initial Rela	eose		01/12/14	DTASIC	Doc No.	W30861-Q1234-MFG
						Variant	Core Design
Rev	Descriptio	渊 Custom	Variable	S			Poge 1 of 4
		Custom	variable	·			8
_			Edit cor	text BASE	•	Add	Toggle Display
			Type	1	Name	1	Value
		1	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	DATE	Hume	10/21/15	
		2	C	DESCRIPTIO	N	BTM	
		3	C C	DOC NO		W30861-0123	34-MEG
		4	c	PROJECT		PN-4815-X-1	
		5	C	REVISION		B.4	
		6	С	TITLE		Control Unit	
		7	С	USER		RNICK	
		8	С	VARIANT_N/	AME	Core Design	
		Options Layer I	Mapping	Update I	Specify history ->	Filter displa Name Value Update variable	ay es -> Help
	(



Design Compare

- Compares two databases and identifies the differences
- Useful when tracking changes in the product lifecycle
- Two modes

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- Standard Compare

Generates an HTML report with differences that apply to netlist, placement, BOM, testpoints, etc.

- Graphical Compare

Based on IPC-2581 all or individual layers can be compared graphically, differences will be highlighted, markers can be generated

对 Design C	ompare
Compare	Designs
First:	D:/design_projects/amplifier_v1.brd
Second:	D:/design_projects/amplifier_v2.brd
Options	
C Stan	dard Compare (Netlist, Placement, BOM, Testpoints)
@ Grap	hical Compare (based on IPC2581)
	Use data from previous session (skip IPC export/import)
	Create new database (Recommended): ipc_compare.brd
	Use default film definitions
Ove	erride undefined width: Lines: 0.050 Texts: 0.050
Units	Millimeters 💌
	Start Cancel Help



Design Compare

Standard Compare

- HTML based report
- Expand / collapse functionality facilitates navigation

				•	-		
) 🛞 file	:///D:/design_projects/design_c	com C Q Suchen	☆ 自 ♥	Â	Ø 🖗	1	>>
ollapse	details						
							۲
					c a d	епс	e
CB E	ditor Design	Compare Re	eport				
_							
Gene	eral						
Data	base Info						
Stac	kup						
N	- 1						
Netii	st						
Com	nonents						
Com	ponents						
Com Sum	ponents ^{mary}						
Com Sum Place	ponents mary ement Changes						
Com Sum Place	ponents mary ement Changes	Design V2	Nete	1			
Com Sum Place Refdes	ponents mary ement Changes Design V1 (xy side angle)	Design V2 (xy side angle)	Note				
Com Sum Place Refdes	ponents mary ement Changes Design V1 (xy side angle) (83.9900 82.1200)	Design V2 (xy side angle) (85.5800 82.1600)	Note				
Com Sum Place Refdes	ponents mary ement Changes Design V1 (xy side angle) (83.9900 82.1200) TOP	Design V2 (xy side angle) (85.5800 82.1600) TOP	Note Placement change				
Com Sum Place Refdes	Design V1 (xy side angle) (83.9900 82.1200) TOP 90.0000	Design V2 (xy side angle) (85.5800 82.1600) TOP 90.0000	Note Placement change				
Com Sum Place Refdes	Design VI (xy side angle) (83.9900 82.1200) TOP 90.0000 (56.9900 35.1200)	Design V2 (xy side angle) (85.5800 82.1600) TOP 90.0000 (56.1000 34.3100)	Note Placement change	-			
Com Sum Place Refdes c12	Design V1 (xy side angle) (83.9900 82.1200) TOP 90.0000 (56.9900 35.1200) TOP	Design V2 (xy side angle) (85.5800 82.1600) TOP 90.0000 (56.1000 34.3100) BOTTOM	Note Placement change Placement change	-			
Com Sum Place Refdes c12	Design VI (xy side angle) (83.9900 82.1200) TOP 90.0000 (56.9900 35.1200) TOP 270.0000	Design V2 (xy side angle) (85.5800 82.1600) TOP 90.0000 (56.1000 34.3100) BOTTOM 180.0000	Note Placement change Placement change	-			
Com Sum / Place Refdes c12 L5	Design VI (xy side angle) (83.9900 82.1200) TOP 90.0000 (56.9900 35.1200) TOP 270.0000 (67.9700 77.3100)	Design V2 (xy side angle) (85.5800 82.1600) TOP 90.0000 (56.1000 34.3100) BOTTOM 180.0000 (65.2800 77.3600)	Note Placement change Placement change	-			
Com Sum Place Refdes c12 L5	Design V1 (xy side angle) (83.9900 82.1200) TOP 90.0000 (56.9900 35.1200) TOP 270.0000 (67.9700 77.3100) TOP	Design V2 (xy side angle) (85.5800 82.1600) TOP 90.0000 (56.1000 34.3100) BOTTOM 180.0000 (65.2800 77.3600) TOP	Note Placement change Placement change Placement change				

Design Compare

Graphical Compare



Layer Fe	Anterior Compare	er TOM Display Cc	Type Etch Etch Drill Mask Mask Mask Misc	Different 7 11 4 4 9 4 4 4 0	ences
1 1 2 (3 3 4 E 5 1 5 7 5 8 F 9 (0	Lay	Display Cc	Type Etch Etch Etch Drill Mask Mask Mask Misc	Different 7 11 4 4 9 4 4 0 0	ences
1 2 3 4 5 1 5 7 5 9 0	TOP GND VCC BOTTOM BOTTOM SOLDERMASK_TOP SOLDERMASK_TOP OUTLINE OUTLINE	Display Co	Etch Etch Etch Drill Mask Mask Mask Misc	7 11 1 4 9 9 4 4 0	
2 (3) 4) 5) 1 6) 5) 1 6) 5) 1 6) 5) 1 6) 5) 1 9 (0) 9) 0)	GND VCC BOTTOM BOTTOM SOLDERMASK_TOP SOLDERMASK_BOT PASTEMASK_TOP OUTLINE Compare	Display Co	Etch Etch Drill Mask Mask Misc	11 1 4 9 4 4 0	×
3 4 5 1 6 5 7 5 8 F 9 0 Design	VCC BOTTOM IPC2581DRILL_1-4 SOLDERMASK_TOP SOLDERMASK_BOT PASTEMASK_TOP OUTLINE	Display Cc	Etch Etch Drill Mask Mask Misc Misc	1 4 9 4 4 0	
4 E	BOTTOM IPC2581DRILL_1-4 SOLDERMASK_TOP SOLDERMASK_BOT PASTEMASK_TOP OUTLINE Compare	Display Cc	Etch Drill Mask Mask Misc Misc	4 9 4 4 0	
5 1 6 5 7 5 8 F 9 6	IPC2581DRILL_1-4 SOLDERMASK_TOP SOLDERMASK_BOT PASTEMASK_TOP OUTLINE	Display Co	Drill Mask Mask Misc Misc	4 9 4 0	
6 5 7 5 8 F 9 0	SOLDERMASK_TOP SOLDERMASK_BOT PASTEMASK_TOP OUTLINE	Display Co	Mask Mask Mask Misc	9 4 4 0	
7 5 8 F 9 (SOLDERMASK_BOT PASTEMASK_TOP OUTLINE	Display Co	Mask Mask Misc		
8 F	OUTLINE	Display Co	Mask Misc		*
9		Display Co	Misc	0	×
Design -	Compare	Display Co	ontrol (Selected o		•
		V1·	00/0#	my)	Baise
	compare	VI.	011/01		rtaise
Tol	lerance Check	V2:	On/Off	— _	Raise
(Create DRC	Diff:	On/Off		Raise
	Show->	Miscellar	neous		
	Hide ->	🔽 Limi	t Check to outline	extents only	
		Min Ape	erture 0.005	Min Area	0.025
Design Ir V1: amp	nfo blifier_v1.brd		V2: amplifier_v	/2.brd	
	Close	CI	ear All ->	He	lp



Digital Soldermask

- Additional features accounting for new technologies
- Developed together with Würth Elektronik
- Various modes

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- Pad ring / box
- Trace mode
- Component mode
- By region
- Parameters
 - Bridge width
 - Pin, via gap
 - Length offset

- . . .

Pagion	DESIGN	▼ Create	Diagram	
Tashralanu	Carry Cast			_ · · · · · ·
rechnology	spray coat	-	t t	Bridge width
Mode	Pad Box	▼		
Layer(s)	ТОР	▼		Length
Output	DIGITAL_SOLDER_1	▼ New		offset
Options				+
Bridge width	0.12			Din maak man
- Length Offset	0.10			Pin mask gap
Pin mask gap	0.05			
Via mask gap	0.05	🗹 Use via hole		
			*	
dvanced			Vi	a mask gap
Comp boundary	PLACE_BOUND	•		3p
Pad margin	0.15			
Min aperture	0.07			



Digital Soldermask

Pad box

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Trace mode



Component boundary



Soldermask region





Digital Soldermask

 Techniques can be combined and used to create multiple masks on separate layers, accounting for mask thickness and thickness requirements



3D canvas



- In example above:
 - Solder mask region on Digital_Soldermask_1_TOP
 - Pad box on Digital_Soldermask_2_TOP
 - Pad box on Digital_Soldermask_3_TOP

56



- Includes useful functions for drafting purposes
- Functions support dynamic preview before changes are committed
- Several functions
 - Modify line

- Modify arc / circle
- Copy array line
- Copy array arc / circle
- Trim objects
- Cut objects
- Arc2Vector
- Ellipse

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Q	Setu Disp Edit	p lay	+ + +	▼
	Draf Shap Chec Docu Man Sign Cust Misc Over	t bes ck/Review umentation ufacture al Integrity om cellaneous		Modify line Modify arc/circle Copy array line Copy array arc/circle Trim objects Cut objects Arc2Vector Ellipse Snap Generator



Modify line

- Change line attributes on a parameter basis: Coordinates as well as angle, width and length
- Angle display can be swapped
- Fix point for rotation and length changes can be chosen
- Fine-tuning capabilities for angle, width and length



Options		д ▼ ×				
	[FlowCAD				
License	CLicensed for:					
FlowCA	.D, Internal Us	e Only				
Line att	ributes					
Point	x	у				
A	170.200	63.100				
Center	176.753	67.689				
В	183.306	72.277				
Angle	35.000					
Width	0.300					
Length	16 000					
Lengu	10.000					
Options						
Angle o	lisplay 🗧	Swap				
Fiynoin	t (rotation len	ath changes)				
Center						
Tuning						
Parameter Angle 🗸						
Increme	ent 5.000	• -				



Modify arc / circle

- Change arc or circle attributes on a parameter basis:
 Center coordinate as well as radius, start angle, sector angle and width
- Fine-tuning capabilities

		>		×
CArc/circle attribute	tes	-AI	rc/circle attribut	tes
Center X	127.000		Center X	124.000
Center Y	63.000		Center Y	65.000
Radius	10.000		Radius	4.319
Start angle	45.000		Start angle	
Sector angle	90.000		Sector angle	
Width	0.200		Width	0.300

Options	д * ×
	FlowCAD
CLicensed for:	
FlowCAD, Intern	al Use Only
~Arc/circle attribu	utes
Center X	127.000
Center Y	63.000
Radius	10.000
Start angle	45.000
	00.000
Sector angle	90.000
	0.200
width	0.200
Turing	/
Parameter Ra	adius
I	
increment 0.0	



Copy array line

- Copies lines in parallel to a selected object
- Number of copies can be specified as well as air gap (or center gap respectively)
- Swap side

Options	τ * ×
	FlowCAD
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FlowCAD, Intern	nal Use Only
Copy line optio	ns
Questite	
Quantity	4
Air dan	0.700
Center gap	1.000
Swan	sido
- Swah	side

11	Copy line options		Copy line options
	Quantity 4	1.	Quantity 4
	Air gap 0.700		Air gap 0.700
	Center gap 1.000		Center gap 1.000
	Swap side		Swanside



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Copy array arc / circle

- Copies arcs in a concentric way to a selected object
- Number of copies can be specified as well as air gap (or center gap respectively)
- Direction can be chosen

Options	д т х		
	FlowCAD		
-Licensed for: —			
FlowCAD, Interr	al Use Only		
Copy arc/circle	options		
Copy outside			
O Copy inside			
Quantity	5		
Air gap	0.700		
Center gap	1.000		



Copy arc/circle	Copy arc/circle options			
Copy outside				
O Copy inside				
Quantity 5				
Air gap	0.700			
Center gap	1.000			



Copy arc/circle options				
O Copy out	O Copy outside			
Copy insi	de			
Quantity	5			
Air gap	0.700			
Center gap	1.000			



Trim objects

- Trims object endpoints to calculated intersections
- Works with arcs and line objects
- Single point mode when two intersections are found (in case of arcs), ability to swap
- Trim vertex for both objects, first only or second only

🔋 Options 🛛 🗶 ୟ	×
FlowCAD	
CLicensed for:	
FlowCAD, Internal Use Only	
Options	
Single point mode Swap	
Trim vertex from	
Both objects	
◯ First object only	
O Second object only	





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Trim objects: Single point mode





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Trim objects: Trim vertex from ...





Cut objects

- Enables users to cut line, arc or circle objects for various purposes
- Two commands
 - Cut objects > By selection
 - Cut objects > Draw path
- Useful when layout portions need to be isolated before moving them to a new location







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Cut objects – Draw path





Options

General

Etch

Destination class/subclass:

_ 8 ×

Drafting Utilities

Ellipse

- Useful for pad shapes and RF applications
- Axis parameter **a** and **b**
- Geometry
 - Full
 - Partial (specify start, end angle)
- Type
 - Solid filled shape
 - Draw line path
- Number of segments





Drawing Designer

- Useful when creating manufacturing drawings
- Records the creation of scaled views (including mirroring and rotation)
- Automatic updates
- Configuration stored in database
- Configuration export and import





Drawing Designer





Drawing Designer

- Ministatus panel offers various options when creating new drawing items
 - Destination layer where data is written to
 - Scale, rotation, mirror of the item
 - Pad style: filled, unfilled
 - Shape: As defined, unfill all, hatched



Note: Hatch option only applies to solid filled shapes





Drawing Size

- Let's you change the design extents in a quick and easy way
- Useful if you want to reduce design extents to minimum values
- Settings can be applied to all or individual sides

Mode © Expand © Contract © Minimum extents © Drag window Options Offset 100.000 Side All sides ▼ Close Apply Help	对 Drawing Size		
 Expand Contract Minimum extents Drag window Options Offset 100.000 Side All sides Close Apply Help 	Mode		
Options Offset 100.000 Side All sides V Close Apply Help	Expand October Control	act 💿 Minimum extents	O Drag window
Offset 100.000 Side All sides Close Apply Help	Options		
Close Apply Help	Offset 100.000	Side All sides	
	Close	Apply	Help





Drawing View Manager

- Facilitates creation of manufacturing drawings
- Features

- Capture named drawing view items interactively
- Clipping capabilities using rectangular or circular boundaries
- Scale, mirror, rotate
- Retain object colors
- Automatic update
- Template support





Drawing View Manager

• Simple use model

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- Press New and enter a name
- Select item from the list
- Press Capture
- Adjust layer visibility and find filter ...
- Adjust mirror, scale, rotation ...
- Place item
- Use Update All once PCB was modified

PCB

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Drawing View Manager

• Template support

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- Significantly shortens setup time
- Eliminates the need to create drawing view items each time from scratch in a new project
- Information about visible layers, objects, source area, destination layer, scaling etc. is already pre-defined
- Default templates located in share/pcb/toolbox/config/drawingview
- SITE and pcbenv customizable
- Use model
 - RMB Choose Template and select an item
 - If necessary adjust scale etc.
 - Place item



Done

Oops

Cancel

Capture

Update

Delete

Info Selected

Snap pick to

PCB

Update All Delete All

Add/Edit Description

Choose Template

New





Scale 2:1


Edge Plating

- Edge plating is a plated conductive material on the edge of a PCB where in normal instances, only dielectric material is exposed
- This plated conductive material may be used for many functions
 - Improve current carrying across multiple layer of a PCB
 - Edge connection protection
 - Board to case grounding
 - EMC signal integrity
 - Heat management
- Two forms of Edge Plating
 - Wraparound (Side) Plating
 - Castellated Holes









Edge Plating: Wraparound (Side)

- Define plating sections interactively
- Net assignment
- Connectivity Check
- DRC Clearance Check
- Net Short support



GND_CHASSIS

Options		
Operation		
Wraparound Ed	lge Plating	
Offset outside	0.50	
Offset inside	0.30	
Clearance	0.70	
🗹 Display Dete	ected Nets	
Block	1	
O Castellated Hol	es Plating	
Spacing	3.00	
Quantity	5 - +	
Via/structure	VIA019 -	
Angle	0.00	
Angle type	Relative 👻	
Place offset	0.00	
General		
Guide	Vertical 🗸 🗹 Snap to grid	
Guide length	4.00	
Increment	10.00 - +	



Edge Plating: Castellated Holes

- Define locations interactively along outline supporting
 - Spacing

- Quantity
- Objects supported
 - Vias
 - Via structures
 - Symbols
 - Electrical components
- Placement parameters
 - Alignment with outline (relative, absolute)
 - Offset from outline

Options Operation OWraparound Edge Plating Offset outside 0.5000 Offset inside 0.3000 Clearance 0.7000 Clearance 0.7000 Clearance 0.7000	8 X
Operation Wraparound Edge Plating Offset outside 0.5000 Offset inside 0.3000 Clearance 0.7000 ICI Disclar Detected Nets	
Wraparound Edge Plating Offset outside 0.5000 Offset inside 0.3000 Clearance 0.7000 Zeinlaw Detected Nets	
Offset outside 0.5000 Offset inside 0.3000 Clearance 0.7000 Image: State of the state	
Offset inside 0.3000 Clearance 0.7000	
Clearance 0.7000	
Display Detected Nets	
Cospidy Detected Nets	
Block 1	
Castellated Holes Plating	
🗶 💦 🛛 🗸 📞 Spacing 3.0000	
Quantity 5 - +	
Via/structure VIA C500 D200	
Angle type Relative	
General	
Guide Vertical 🗸 Snap to grid	
Guide length 4.000	
Increment 10.0000 - +	
	2



FPGA Utilities

- Check and report any pin swapping which has been done in a PCB layout
- Export pin constraints to csv and vendor specific formats
 Altera, Xilinx, Actel, Lattice
- Works in both flows
 - Allegro Design Entry HDL
 - OrCAD Capture
- Various options

HFPGA Utilities 16.4 (C)2016	
Licensed for FlowCAD,Internal Use Only	FlowCAD
General	
Beference Designator: IC1	
Vendor Format: Altera Quartus 🔻	
Parameters	
Ose pin name as FPGA IO-Name	
🔘 Use net name as FPGA IO-Name	
Create unique names	
ECO Mode (LVL-Check)	
Original Connectivity Report:	
Filter Output	
Exclude pins connected to DC-Nets (Voltage Prop	erty)
Exclude pins with pinuse Power or Ground	
Exclude unconnected pins	
Exclude pins which didn't swap (ECO Mode only)	
Output Format	
Sort by pin number Sort by IO-Name	
Generate Close	Help
Generate Close	Help

FPGA Utilities

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											💥 Pin Con	straints fi	ile, Vendor format	
											@ ×	6	Search:	🚱 🕥 🕅 Match word 🔲 Match case
						A	ltera	Quartu	JS		#===== # Pin #	Const	craints for Xilinx XDC	
						2	Pin Cons	straints file, Ve	endor format			X	Apr 05 15:41:47 2018	
Differe	ences R	lepc	ort			1 #	Pin C		Search:	G 🕘 🗌 Match	word 📃 Mato	th case	y PACKAGE_PIN P14 v PACKAGE_PIN R16	[get_ports {AD[0]}] [get ports {AD[1]}]
Pin Swap I	Report: Text Format	Search:				G D	Match wo	_ D X	mo/placed.brd				Y PACKAGE_PIN N16 Y PACKAGE_PIN N13 Y PACKAGE_PIN L15 Y PACKAGE_PIN N15	[get_ports {AD[2]}] [get_ports {AD[3]}] [get_ports {AD[4]}] [get_ports {AD[5]}]
<pre>#======= # Pin Swa # Design: # compare # File: # # Date: #</pre>	ap Report : D:/demo/pl ed with D:/demo/in Apr 05 15:4	Laced.b nitial. 40:22 2	rd txt 018						gnment PIN_P14 gnment PIN_R16 gnment PIN_N16 gnment PIN_N13 gnment PIN_L15	-to AD[0] -to AD[1] -to AD[2] -to AD[3] -to AD[4]		-	Y PACKAGE_PIN P15 Y PACKAGE_PIN M15 Y PACKAGE_PIN L16 Y PACKAGE_PIN N14 Y PACKAGE_PIN M13 Y PACKAGE_PIN K14 Y PACKAGE_PIN L14	[get_ports {AD[6]}] [get_ports {AD[7]}] [get_ports {AD[8]}] [get_ports {AD[9]}] [get_ports {AD[10]}] [get_ports {AD[11]}] [get_ports {AD[12]}]
<pre># Ref #====================================</pre>	PinName AD[4] AD[6] AD[10] AD[15] AD[7] GPI0[1] AD[9] AD[2] GPI0[2] GPI0[2] GPI0[4] KB_KSOP_0[5] AD[6]	Slot G1 G1 G1 G1 G1 G1 G1 G1 G1 G1 G1 G1	OldPin N14 M14 M15 L16 M13 P7 L15 P15 P15 P6 P5 N6 N16	NewPin L15 L16 M13 M14 M15 N6 N14 N16 P5 P6 P7 P15	OldType BI BI BI BI BI BI BI BI BI BI BI BI	NewType BI BI BI BI BI BI BI BI BI BI BI BI	A9 BD14 A7 A8 A10 BD0 A4 A6 BD4 BD2 BD1 A2	NewNet A4 A8 A10 BD14 A7 BD1 A9 A2 BD2 BD4 BD0 A6	gnment PIN_N15 gnment PIN_P15 gnment PIN_M15 gnment PIN_L16 gnment PIN_N14 gnment PIN_M13 gnment PIN_K14	-to AD[5] -to AD[6] -to AD[7] -to AD[8] -to AD[9] -to AD[10] -to AD[11]		Ŧ		

Xilinx XDC



Highlight Dummy Pins

- Assigns a color to all pins in a design which are not connected to any net
- Including report and cross probe functionality
- Useful for review purposes

💵 Dummy Pin	Report		🛃 Highlight Dummy Pins 🛛 🗖 🗮 🔀		
File Close	Help				
<u></u>	Terb		Options		
01.13	(65.405 69.215)	A			براوا ويجاد المتعلمات المالية المالية المالية
01.16	(69.215 69.215)		V Dummy nets	2 2 2 2 2 2 2 2 2 2 1 2 2 2 2	
01.17	(69.215 78.74)				
0101.1	(73.66 69.215)				
0101.12	(87.63 69.215)		Single node nets		
0101.13	(88.9 69.215)				
0101.16	(92.71 69.215)				
0101.17	(92.71 78.74)		Clear		
0102.1	(73.66 82.55)				
0102.12	(87.63 82.55)		Benort Only		بهراجا والمتعاد المالية المتراج المتلج المحالية
0102.13	(88.9 82.55)		(topott only		
0102.16	(92.71 82.55)	=			
0102.17	(92.71 92.075)				
017.7	(28.575 50.8)		Close Apply Help		
018.6	(-1.905 96.52)				
019.13	(26.289 46.66)				
019.15	(23.749 46.66)				
019.17	(21.209 46.66)				
019.19	(18.669 46.66)		Assign Color		
02.1	(50.165 82.55)				2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
02.12	(64.135 82.55)				
02.13	(65.405 82.55)				
02.16	(69.215 82.55)				
02.17	(69.215 92.075)				
022.1	(60.833 48.768)				
022.3	(60.833 43.688)				
022.5	(68.453 41.148)				
022.6	(68.453 43.688)				
026.13	(166.405 86.438)	-	Nexta		
			Caller		



IBIS Prototype Modeler

- Creates scalable IBIS models for early stage signal integrity analysis
- Features include

- Ability to create Push / Pull, Open-Sink and Open-Source buffers
- Adjustable voltage levels
- Adjustable internal resistance including a calculator
- Adjustable slew rate dV / dt
- Ability to include saturation and clamping effects
- Support for single-ended as well as differential outputs
- Support for output only and bidirectional models
- Ability to view curves in Sigwave
- Generate DML models as well as native IBIS models

Licensed for Flow	CAD,Interna	l Use Only					FlowCAD
Model type		_			-		
Push/Pull c	lriver	🔘 Ореі	n sink driv	/er	\bigcirc	Open sa	urce driver
General							
Voltage levels:	VoH 3	.300 V	VoL	0.0	00 V	Vra	nge 3.300 V
Driver strength:	Rslope 1	2.500 Ohi	n	Calc	ulate		
Slew rate:	Trise 0	.250 ns	0	10/90]% ▼		
Options							
🔽 Include saturati	on						
Pullup curve:	lpu min	-110.000	mA Ip	ı max	55.000	mA	Set limits
Pulldown curv	e: Ipdimin	-80.000	mA Ip	d max	80.000	mA	Set limits
📝 Include clampir	g						
Power clamp:	Vpcl	4.100	V Rp	ocl	0.500	Ohm	
Ground clamp	: Vgcl	-0.800	V R <u>q</u>	cl	0.500	Ohm	
🔲 Model as differ	ential outpu	t					
🔲 Model as I/O (ty	/pe bidirect	ional)					
Output							
Model name: m	y_prototyp	e_model					
Close	View curve	s V	vrite DML		Write	lbis	Help

IBIS Prototype Modeler

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Pullup, Pulldown and Rload curves



Power, Ground clamp



Label Generator

- Creates signal name and pin labels for documentation purposes
- Selectable label content (e.g. signal same + pin number)
- Individual label origin (e.g. pin, or via origin, but also cursor intersecting cline)
- Aligned text rotation mode (text angle value follow cursor gesture)
- Supports three different object types (pin, via, cline)
- User defined text size, justification and rotation

Options	Find	Visibility
Options —		
License FlowCA	d for: — D,Intern	FlowCAD al Use Only
Display	Conten	t
NET_	NAME	▼
Manufa	cturing s	subclass:
FLW_	LABEL_	NOTE 🔻
Object f	Filter:	Cline 🔘 Via
Text Filt	ter:	
Text Blo	ock:	1
Text Ro	tation:	ALIGNED -
Text Ju	st.:	LEFT 🔻
Text Off	set X:	0.0000
Text Off	set Y:	0.0000
Text Mi	rror:	
[Cle	ar All



Label Generator

Procedure





Label Generator

Label Content







Label Tune

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- Adjusting component labels automatically
 - Better readability
 - Saves a lot of time when creating assembly drawings

• Features

- Label can be chosen (e.g. Refdes, Value, Part Number, …)
- Automatic rotate, center, fit
- Automatic mirroring
- Visibility control
- Various options
 - Max block size, max height
 - Boundary clearance

abel Tune	🐉 Label Tune
ain Advanced	Main Advanced
Objects	Text rotation
Label name Refdes 🔻	Longest side
Assembly a	TOP horizontal: 0 💌 deg
	TOP vertical: 90 💌 deg
Outline data Assembly 💌	BOTTOM horizontal: 0 💌 deg
	BOTTOM vertical: 270 💌 deg
Visibility control	○ Fixed angle 0
Limit layers	C Relative angle from symbol definition
Bottom On/Off	Text center
Components on bottom side	Offset correction: 0.00
✓ Label mirrored	Tayt fit
14- d-	Specify by height
Mode	Min 0.50 May 15.00
	 Specify by block
	Blocks 1-35
Dx 0.00 Dy 0.00	
✓ Fit text	Clearance to boundary: 0.000
Close Cancel Help	Close Cancel Help

?



Label Tune

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Typical situation in PCB Editor



Result after running Label Tune

Animation

Label Tune

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Another example





R28

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Mask Generator

- In some cases customers may want to oversize mask data (soldermask, pastemask) due to manufacturing requirements
- Data will be generated on manufacturing subclass. The original padstacks won't be touched
- Input parameters
 - Source data ("What to oversize") can be specified separately for vias and pins
 - Oversize values (positive and negative)
 - Side to process
 - Manufacturing subclass where data will be written to

🙀 Mask Generate	or			
Pin objects			Via objects	
Source	Etch pad	•	Source	Drill hole 💌
Oversize	0.010		Oversize	0.010
Options				
Process side	•	Both	•	
Manufacturin	g subclass	MSK_0	V10U 🔻	New
C	IK	Ge	nerate	Help

Pin objects	
Source	Etch pad 💌
Oversize	Soldermask Pastemask
00013120	Etch pad





Mask Generator

Pins and vias on TOP

Manufacturing subclass MSK_OV30U_TOP

Mask Generator Pin objects Source Etch pad Oversize 0.030 Options Process side Manufacturing subclass OK	▼ Via objects Source Oversize Both ▼ MSK_OV30U ▼ Generate	Etch pad 0.030 New Help	



- Toolset supporting various techniques for PCBs in a panel to be easily separated after they are manufactured and assembled
- Mill tab panels
 - Add mill contour
 - Split & Cut mill
 - Add mill tabs with or without perforation drills
- V-Score panels





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Add mill contour along the edge of the board

Create splits interactively

Markers

2

•

Done Oops

Cancel

Add mill contour

Create mill split

Delete mill path

Add mill tab

Delete mill tab

Add V-Score

Delete V-Score

Delete all data

Snap pick to

Cleanup NCRoute

Copy edits to design

Cut back mill along V-Score

Delete data by instance

Delete splits

Done

Oops

Cancel

RN

Guide

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- Mill tabs can be specified with respect to

 Tab size
 - Number of holes, diameter spacing and offset
- Application provides libraries from PCB fabricators – AT&S
 - Fineline
 - Alba PCB Group / Q-print electronic
- Interactive placement
 - Can be placed on any contour









- V-Score lines can be defined in horizontal or vertical directions by selection an appropriate side of the board
- Existing milling can be cut back
- V-Score fabrication details can be specified which creates an IPC-2581 Spec Definition entry in the database







Net Color View

- Allows saving and restoring net color and rat visibility settings
- Useful for floor planning and route feasibility studies
- Global visibility commands
 - Useful hands-on for configuring a view (display / blank rats and assign net colors)
 - Find By Name support
 - No need for jumping and travelling to standard commands from PCB Editor





General	
View name io_	_interface 🔻
Save	Restore Misc ->
Save options	Restore options
✓ Visible rats	Complete Incremental
Colored nets	C Toggle
Global visibility	
Show Rats ->	Highlight ->
Blank Rats ->	Dehighlight ->



Net Min Gap

- Measures the smallest gap between two nets without adjusting DRC spacing rules
- Features
 - Multiple nets selection
 - Filter by spacing class including wildcard
 - Restrict measurements to certain layers
 - N smallest gaps (e.g. Report 3 smallest values for a given net-net combination)
 - Output tab with cross probing
 - Export results to CSV



Filter Net A Net B



Padstack Finder

- Enables users to search and navigate for padstacks in the current design
 - Filter capabilities
 - Distinguish between pins and vias
 - Padstack name
 - Drill size

- Wildcard support
- Highlight and cross probe
- Color by group

Padstack Report			
<u>F</u> ile <u>C</u> lose <u>H</u> elp			
Name	Location	DrillSize	Start<->End
SHD0 75X0 65R	(164.3 81.0)	0.0	TOP<->TOP
SHDO_75X0_65R	(164.3 79.7)	0.0	TOP<->TOP
SHD0_75X0_65R	(164.3 52.0)	0.0	TOP<->TOP
SMD0_75X0_65R	(164.3 50.7)	0.0	TOP<->TOP
SMD0_75X0_65R	(163.3 81.0)	0.0	TOP<->TOP
SMD0_75X0_65R	(163.3 79.7)	0.0	TOP<->TOP
SMD0_75X0_65R	(163.3 52.0)	0.0	TOP<->TOP
SHD0_75X0_65R	(163.3 50.7)	0.0	TOP<->TOP
SHD0_75X0_65R	(130.6 19.0)	0.0	TOP<->TOP
5HDU_75XU_65R	(130.6.20.0)	0.0	TOP<->TOP
5MD0_75X0_65R	(90.3 26.7)	U.U	TOP<->TOP
		0.0	
SHDU_/SAU_65K	(48.0 47.5)	0.0	
SHD0_/SAU_05K	(47.0 47.3)	0.0	
SHDU_/SAU_0SK	(47.0 40.2)	0.0	
	(175 25 95 4)	0.0	TOP
	(175.25.82.0)	0.0	TOPC-STOP
	(175 25 78 6)	0.0	TOPC-STOP
SWD1 0X0 8R	(175 25 56 4)	0.0	TOP(-)TOP
SWD1 0X0 8R	(175 25 53 0)	ñ ñ	TOP(->TOP
SHD1 OXO 8R	(175.25 49.6)	0.0	TOP<->TOP
SHD1_0X0_8R	(173.55 85.4)	0.0	TOP<->TOP
SHD1_0X0_8R	(173.55 82.0)	0.0	TOP<->TOP
SMD1_OX0_8R	(173.55 78.6)	0.0	TOP<->TOP
•	111		





Filter			
Objects:	✓ Show pins	V Show v	ias
Pattern:	SMD*		
Drill size	•	•	
SMD0_45C SMD0_65S			-
SMD0_75X	0_65R		
SMD0_7X0	_3R		-11
SMD1_0X0	8R		=
SMD1_0X0	_95R		
SMD1_15X	0_75R		
SMD1_1X0	_3R		_
SMD1_25X	0_650		
SMD1_45A	40		
SMD1 5X1	4R		
SMD1_8X1	_15R		
SMD2_0X0	_60		-
Mode			
Highlig	nt		
Color			
Group	DEFAULT	▼ Cle	ear
Lioup		UN	
Beport	Only		
	,		
Close	Annhy	Не	aln
Cluse	Apply	пе	ah



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Padstack Finder

Objects: Stacked Vias

Filter

Padstack Finder

- Now supporting Vias Stacks
 - Display label formed by individual drill spans
 - Highlight and cross probe





Padstack Usage

- Generate padstack reports by extracting data from PCB Editor symbol libraries (*.dra). Different reports are available:
- Report types

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- Where-Used
 Lists all footprints that use a given padstack
- Padstack Standard
 Lists the padstack definitions for a given footprint
- Padstack Detailed

Lists detailed information for a given footprint. This information includes number of pins, vias and mechanical pins, pin numbers, xy coordinates, etc.

- Report format
 - -HTML
 - -Excel
 - Text

	eters v Help
C:\Libraries\pcb_symbols Process all libraries specified by psmpath Options Type Where-Used Report Close Run B Bearbeiten Ansicht Chronik Leszerichen Egtras Hilfe KB Editor Pad Usage Report * +	eters V
Process all libraries specified by psmpath Options Type Where-Used Report Close Run B Bearbeiten Ansicht Chronik Leszerichen Egtras Hilfe KB Editor Pad Usage Report * +	eters v Help
Options Type Where-Used Report Close Run H Bearbeiten Ansicht Chronik Lesezeichen Egtras Hilfe CB Editor Pad Usage Report +	eters V
Type Where-Used Report	eters v
Close Run Bearbeiten Ansicht Chronik Lesezeichen Egtras Hilfe CB Editor Pad Usage Report × +	Help
Close Run Bearbeiten Ansicht Chronik Lesezeichen Egtras Hilfe CB Editor Pad Usage Report × +	Help
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pad93cir51d 1 inductor	
smd25_481lcc48	
smd25 50 1 lcc32	
smd25_94 1 lcc48	
smd2_25x1_8r 1 ind_ihlp-1616	
smd2_45x2_35r 1 ind_s4924	
smd30_115 1 lcc24	
smd30_55 4 lcc20 lcc24 lcc28 lcc44	
smd30_55 4 lcc20 lcc24 lcc28 lcc44 smd30_57 2 lcc52 lcc68	
smd30_55 4 lcc20 lcc24 lcc28 lcc44 smd30_57 2 lcc52 lcc68 smd30_94 3 lcc28 lcc44	
smd30_55 4 lcc20 lcc28 lcc44 smd30_57 2 lcc52 lcc68 smd30_94 3 lcc20 lcc44 smd30_96 1 lcc52	

Padstack Usage

Report examples

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Datei Bearbeiten Ans	iicht <u>C</u> hronik L e Report ×	esezeichen Extras	∐ilfe				_ 🗆 🗙														
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						cāde	n c e°														
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smd25_48	1	lcc48									u u	c ii c									
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smd25_94	1	lcc48		FCB Eultor	raustav	K OSAGE IN	eport														
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smd30_55	4	lcc20		ind \$4924	1	smd2_25x1_0															ľ
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		lcc44		inductor	1	pad93cir51d		I													
smd30_57	2	lcc52 lcc68		lcc20	2	smd30_55 smd30_94		PCB	Editor	Padstack U	Isag	e Rep	ort								
smd30_94	3	lcc20		lcc24	2	smd30 115		For	otprint	Pins/Vias/Mech	Туре	Number	Padstack	X	Y	-					
		lcc28				smd30_55		hei	ader30	30/0/0	Pin	1	sqb0_37d	2.540	0.000	-					
smd30_96	1	lec52		lcc28	2	smd30_55					Pin	3	cir60_37d	5.080	0.000	1					
smd4_0x3_0r	1	ind ccm063		10032	1	smu30_54					Pin	4	cir60_37d	7.620	0.000	1					
sa60_27d	1	hoador20		lcc44	2	smd30_55	-				Pin	5	cir60_37d	10.160	0.000	1					
3400_370	1	Treader50		10044	-	smd30_94					Pin	6	cir60_37d	12.700	0.000						
				lcc48	2	smd25_48					Pin	7	cir60_37d	15.240	0.000						
						smd25_94	-				Pin	8	cir60_37d	17.780	0.000						
				lcc52	2	smd30_57 smd30_96					Pin	9	cir60_37d	20.320	0.000	-					
				lcc68	1	smd30_57					Pin	10	cir60_37d	22.860	0.000	-					
							1				Pin	12	cir60_37d	25.400	0.000	-					
				L							Pin	13	cir60 37d	30.480	0.000	1					
											Pin	14	cir60_37d	33.020	0.000	1					
											Pin	15	cir60_37d	35.560	0.000	1					

Pin 16 Pin 17

Pin 18

Pin 19

cir60_37d

cir60_37d

cir60_37d

cir60_37d

0.000 -2.540 2.540 -2.540

5.080 -2.540

7.620 -2.540

Datei Start Einfügen	Seitenlavout Formeln	Daten Überprüfen Ansicht Add	-Ins Acrobat	\$	2 - 6
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A	В	С	D	E	F
1 Padstack	References	Footprint(s)			
2 cir60_37d	1	header30			
3 pad93cir51d	1	inductor			
4 smd25_48	1	lcc48			
5 smd25_50	1	lcc32			
6 smd25_94	1	lcc48			
7 smd2_25x1_8r	1	ind_ihlp-1616			
8 smd2_45x2_35r	1	ind_s4924			
9 smd30_115	1	lcc24			
10 smd30_55	4	lcc20			
11		lcc24			
12		lcc28			
13		lcc44			
14 smd30_57	2	lcc52			
15	-	Icc68			
16 smd30_94	3	Icc20			
17					
18 10 amd20 06	1				
19 sma30_96	1	ICCD2			
20 sma4_0x3_0r	1	Ing_ssm003			
21 SUDU_370	1	Tieduerso			
73					
	longet /				

— 🗆 🗙



- Simplifies panel documentation process
- Boards can be stepped individually or by array
- Boards can be rotated and / or mirrored individually
- Automatic update
- Automatic notification if boards have been modified
- Based on proven mdd-Technology (Design Reuse, Place Replicate)
- Supports standard panels as well as family panels
- Configuration stored in database

😻 Allegro PCB	B Designer: pane	l.brd Proje	ct: D:/panel_demo						_ D X
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ile	Panel	list							C 0
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	5	PS	AMPLIFIER	161.000	16.000	0.000	No	17 11	
	6	P6	AMPLIFIER	161,000	116.000	0.000	No	-	
	7	P7	AMPLIFIER	161.000	216.000	0.000	No	•	
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- Setting up a new panel
 - Open a new database or panel template
 - Launch FloWare > Panelization
 - Link your boards
 - Create modules
 - Place a single instance or an array of your board
 - Done
- Updating an existing panel (e.g. original layouts have been modified)
 - Open the panel database
 - Launch FloWare > Panelization
 - Choose Update panel
 - Done
 - Create manufacturing data as usual ...

🦆 Paneliza	ation							
Main Desigr	Setup ns							
	Name	Design loc	ation					
	AMP	d A						
	<							
	📝 Use relative de	esign path						
Desigr Laye Anno Pr Se	n contents rs to include All Artwo ntate refdes rimary Refdes econdary (None	Design processing Exclude routing Load artwork Clear nets						
Synchi	ronize stackup	Import	Placement					
Desi	Design AMP Tech file Create modules Unify layer names Wirebond profiles Place							
ОК	Update	panel Status	Cleanup Help					





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- Interactive placement
 - Place single instances or array
 - Dynamic preview attached to cursor (board size, orientation, rotation, mirror)
 - Display design bounding box or actual outline
 - Snap to grid option

P P P	
P P P	

Display bounding box



对 Panelization			
Manual placement	t		
Board AMPLIF	IER 💌	Columms	1
Extents 110.00x	90.00	Rows	1
Rotation 0.000		Offset X	0.000
Mirror No	•	Offset Y	0.000
Mode		Options	
Place single	instance	🔽 Displa	y actual outline y module extents
O Place instance	e array	🔽 Snap t	o grid
Close			Help



- Panel modifications
 - Change parameters (e.g. x, y) of instance to be changed
 - Fields become yellow
 - Choose context menu Update changes to confirm



Panel li	ist			
	ld	Design	×	Y
1	P1	AMPLIFIER	76.000	220.000
2	P2	AMPLIFIER	76.000	82.000
3	P3		353.000	223.000
4	P4	Delete Item	350.000	82.000
5	P5	Update changes	200.000	84.000
6	P6	- Teblight	200.000	149.000
7	P7	ighlight	200.000	214.000
8	P8	Dehighlight all	200.000	279.000
		Denighight an		







- - X

Panelization

• Family panels

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- Contain more than one board layout
- Simply link the board databases
- Make your placement





Panelization

Main Setup

Panel list



- Panel status
 - Automatic notification when board databases have been modified
 - Status report gives details about time stamps

	list										
	Id	Design	×	X Y Rotation		Mirror		Mirror		ſ.,	
1	P1	AMPLIFIER	76.000	220.000	90.000	No	-				
2	P2	AMPLIFIER	76.000	82.000	90.000	No					
3	P3	AMPLIFIER	353.000	223.000	90.000	No					
4	P4	AMPLIFIER	350.000	82.000	90.000	No	•				
5	P5	CONTROL	200.000	84.000	90.000	No	•				
6	P6	CONTROL	200.000	149.000	90.000	No	•				
7	P7	CONTROL	200.000	214.000	90.000	No	•				
8	P8	CONTROL	200.000	279.000	90.000	No	•				
							•	•			



<u>File</u> <u>C</u> lose	<u>H</u> elp		
Inotanco	Decign	Tact II	
		Last U	
P1	AMPLIFIER	Oct 12	11.27.55 2012
P2	AMPLIFIER	0ct 12	11:27:55 2012
P3	AMPLIFIER	Oct 12	11:27:55 2012
P4	AMPLIFIER	Oct 12	11:27:55 2012
P5	CONTROL	Oct 12	11:27:55 2012
P6	CONTROL	Oct 12	11:27:55 2012
P7	CONTROL	Oct 12	11:27:55 2012
P8	CONTROL	0ct 12	11:27:55 2012
Design	Last Modifie	d 	Path
ANPLIFIER	Oct 12 11:45	·21 2012	D:/namel_demo/boards/project1/amplifier_brd
CONTROL	Oct 12 11:23	:00 2012	D:/panel_demo/boards/project3/control.brd

- Documentation of PCB footprints within a selected library
 - Includes graphical representation of footprint graphics
 - Graphics will be scaled into dedicated areas for better readability
 - Additional attributes (size, pitch, padstacks used etc.) are automatically extracted and written to the document
 - Frame templates are provided
 - Customizable contents and drawing styles including drill holes
 - One single PDF document for all footprints





Default Mode

- Basic information
- More footprints per page

Detailed Mode

- Additional information
- Less footprints
 per page



PLCC28_10_9X10_9

Attributes:				
Size	13.300 x	13.300	MM	(visible)
Height PitchX PitchY ConnPinCnt ConnPads MechPinCnt MechPads	13.800 x 4.6 MM 1.270 MM 1.270 MM 28 SMD2_4X0 0 NA	_650	MM	(PlaceBound)



• Templates

- Define the areas to be used for plotting which correlates to the number of footprints per page
- Metadata support for title blocks (page number, date, user, library name)
- Default templates provided
- Customer can define his own templates





Examples

 \bigcirc



6 footprints on A3

Detailed attributes



DIN64 Pins 64 Size 19.050 x 93.980 MM (visible)

7

DIP8 Pins 8 Size 9.195 x 10.160 MM (visible)

 $\exists \oplus$

FlowCAD


PCB Library Plot

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Customizable content including drill holes and various drawing styles



Assembly TOP including etch and drill holes

Placebound as hatch shape including etch and drill holes

Scale 5:1

USB3A FEMALE

Pins 1T Size 16.600 x 16.700 MM (visible)



- Useful for boards where circular placement and routing is required
- Providing a set of functions
 - Defining and editing a polar grid
 - Polar placement
 - Polar routing

- Polar shape editing including voids
- Snap control
 - Coarse and fine grid
 - System grid
- Polar grid can be also used in conjunction with standard PCB Editor commands using
 RMB > Snap pick to > Intersection

Tools	Flo	<u>W</u> are <u>H</u> elp					
Q		Setup Display Edit	+ +	•	# 🔡 🗃 🍰	📓 🛈 😭	123
		Draft Shapes Check/Review Documentation	> > > >		Change Width Coil Designer Cross Copy Label Tune		
		Manufacture Signal Integrity Custom Miscellaneous	> > >		Polar Grid Push to Grid Replace Via Shield Generator	Setup Grid Place Route Shape	
		Overview			Shield Kouting	Shape Void	





- Polar Grid Setup
 - Define a new grid
 - Edit an existing grid
 - Fully parameterized
 - Coarse and fine grid settings
 - Line and dot style support
 - Stored as format symbol in database
 - Visibility control











- Polar placement
 - Special mode for placing component in circular or radial fashion
 - Snap to fine or coarse grid
 - Various alignment and rotation capabilities
 - Spinning on polar grid basis (e.g. Polar lock)



puons		4
Mode		
Place		
O Place	and Spin	
🔿 Spin o	nly	
Snap option:	s	
🗸 Coarse	Show	Lines 🔻
🔽 Fine	Show	Dots 🔻
System	Show	
Options — Botation		
riotation		
Туре	Radial lon	g side 🔻
Type Angle	Radial Ion 90.0	g side 💌
Type Angle Symbol pic	Radial Ion 90.0 :k	g side 💌



• Polar routing

- Special mode for drafting or routing in a circular or radial fashion
- Snap to fine or coarse grid
- Ability to follow radial and angular contour
- Alternate path options (e.g. Arc smart)



Etch		
		<u> </u>
		•
Line width 0	.200	
Add connect	options (etch only)
🔲 Snap to	o connect	point
Via VIA		•
Snap options	Show	
	Ohawa	
	Snow	Lines
System	Show	1
Style		
Follow po	lar conto	ur
Angular	Small a	arc 🔻
Radial	Straigh	t line 🔻
Diagonal	Straigh	t line 🔻
Regular	,	
	Line	45 👻
Line lock		



- Polar shape and void editing
 - Special mode for creating shapes and voids in a polar grid
 - Snap to fine or coarse grid
 - Ability to follow radial and angular contour
 - Alternate path options (e.g. **Arc smart**)







Post Processing

- Central cockpit from which manufacturing output can be configured and generated
- Hit Button solution many users are asking for
- Tasks can be enabled / disabled, added and removed individually
 - Standard functions from PCB Editor
 - Skill procedures (e.g. FloWare)
 - User defined scripts
- Jobs can be defined which contain a collection of tasks
- Configuration stored in database
- Import and Export capabilities for the purpose of standardization

Post Proces	sing nfiguration				X
	default Update Shapes Cross Section Clean Data: ./m Standard BOM Variant BOM: co Variant Assemb NC Drill Legend NC Drill Legend NC Drill Data NC Route Data Artwork Data Standard Plot Batch Plot: all Mfg Collector Zip Data: output	• Add	new	Delet	8
All C	On All Off	Save	e	Load	
Rur		Close		Help	



Post Processing

- Context menu provides task editing

 Info
 - Tasks can be added (appended or inserted)
 - User tasks

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- Predefined tasks including arguments
- Tasks can be removed if not needed at all

对 New Task			
New task			
Add use	er task		
Name	dxfout	Title MyDXF Output	
Script	C:\Cadence\scr	ipts\dxfout.scr	
🔘 Predefii	ned task		
	•	Arg	
Info			
0	ĸ	Cancel	Help

b: default 💌	Add new Delete	🥦 New Task	٢
✓ Vpdate shapes ✓ Update shapes ✓ Custom variables (*) ✓ Cross section (*) ✓ Clean data: ./mfg/*.* ✓ Standard BOM ✓ Variant BOM: core (*) ✓ Variant Assembly: co	re (*)	New task C Add user task Name dxfout Title MyDXF Output Script C:\Cadence\scripts\dxfout.scr Predefined task	
 ♥ Drawing designer (*) ♥ NC drill legend ♥ NC drill data ♥ Artwork data ♥ Standard plot ♥ Batch plot: all (*) ♥ Rename files 	Info Insert task Append task Delete task	Update Shapes Arg all_variants Artwork Data Batch Plot Batch Plot Batch Plot Clean Data Cross Section Custom Variables Mig Collector NC Drill Data NC Boute Data Standard BOM Cancel Update Shapes Variables	
		Variant ROM	

Job:

Zip Data



Post Processing

• Additional built-in functions

- Clean Data

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Performs file delete operations based on arguments provided including wildcards

- Standard BOM

Generates standard BOM in text and csv format

- Standard Plot

Plots all artwork film control records into one PDF file artwork.pdf

– Rename Files

Provides powerful automated file renaming mechanism (wildcards, variables and pattern tags) for PLM purposes

۲	Predefined task			
	Clean data	*	Arg	./mfg/*.*
Info Spe "mfg curr curr	cify argument for data g/*.art" or "./*.log". Us ent working directory s ent working directory y	to be se rela are not you ha	cleane tive pa t accep ve to s	ed in wildcard format, e.g. "mfg/*", athes only. Directories outside the oted. When deleting files in the pecify an extention. (e.g. "./*.log")

Dir	Ext.		Match	Rename to	Move to
mfg	art	*		<project_no>_<file>.gbr</file></project_no>	fab 4
mfg	drl	routed-*		<project_no>_<1>.drl</project_no>	fab
plot	pdf	*		<file>_assembly.pdf</file>	fab
	csv	*BOM*		<file>.bom</file>	fab
•					
Advance	ed Define va	riables	Exp	ort/Import Save config Load (▶



Push to Grid

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- Placement application featuring
 - Highlight off grid symbols
 - Option to move / push symbols to the nearest grid point
 - Regular placement mode for standard placement operations
 - Single and multiple selected symbols
 - Including mirror and spin support



Options	ф т (
General	
All grids 1.0	
Mode	
Highlight only	
O Move to grid	
Place regular	
 Exclude mechanical symbols Exclude fixed symbols Rotation increment 	
Display Highlight color	

122



Quick Symbol Edit

- Opens symbol editor out of a layout database for viewing or editing purposes
- Three modes
 - Edit same session
 - Acts similar to Tools > Modify Design Padstack (next slide)
 - Edit new session
 - Launches a new session and open the symbol dra file
 - Export only
 - Only exports symbol data (dra, psm, pad, etc.) for the selected symbol to a specified directory





Quick Symbol Edit

- Edit same session
 - Seamless edit and update of a symbol definition in board context
 - Acts like Tools > Modify Design Padstack

- Steps:

- 1. Launch Quick Symbol Edit in layout context
- 2. Select a symbol
- 3. Current database closes, symbol dra file will be opened
- 4. Make your modifications
- 5. Finally choose File > Update board database
- 6. Specify update settings
- 7. The layout database from which the command was launched opens again and the footprints will be updated





Replace Via

()

- More flexibility while replacing vias in the design
 - Specify padstack names
 - Restrict replacement to selection area
 - Include and exclude vias from the specified area through interactive commands
 - Additional filter options, e.g. distinguish between
 - Vias with or without testpoint status
 - Mirrored or unmirrored vias
 - Processing options
 - Allow DRC
 - Ignore Fixed
 - Retain Mirror Status





Shape Utilities

- Includes useful functions when editing shapes
 - Boolean operations
 - Size operations (Expand, Contract, Size)
 - Rectangular shapes with rounded corners
 - Advanced boundary edit functions
 - Stretch
 - Cut

- Round off vertices
- Change round off radius
- Modify individual arc parameters
- Modify shape priorities
- Check status

<u>T</u> ools	Flo <u>W</u> are <u>H</u> elp			
	Setup Display Edit Draft	* * *	▼ # # # # \$ ₩ ₩	
	Shapes Check/Review Documentation Manufacture Signal Integrity Custom Miscellaneous Overview	• • • •	Boolean Size Rounded Rectangle Advanced Boundary Edit Change Priority Check Status	



Shape Utilities – Boolean Operations

- Features
 - OR, AND, ANDNOT, XOR
 - Supports shape-shape operations as well as shape-line and shape-text operations
 - Shape attributes (shape type, fill style, net name etc.) are retained and applied to the resulting shape
 - Ability to split shapes across voids

ANDNOT

Expand / contract capabilities

Etching negative texts into copper

– Useful for general editing and basic RF-applications

NEGATIVE TEXT

Cutting a dynamic shape

ANDNOT





Shape Utilities – Boolean Operations

- Let's you also split shapes across voids
- Useful when working on non-voidable layers such as KEEPOUT, NO_PROBE etc.





Shape Utilities – Size Operations

 Expand / Contract similar to Edit > ZCopy but directly acts on selected shape. No copies remain. Additional options for void handling



Options	
Shape Options Mode:	
Expand	
Offset: 0.000	
🔘 Scale	
Value: 1.000	
Voids:	
Ignore voids 🔹 🔻	



Shape Utilities – Rounded Rectangular Shapes

- Useful when defining pad shapes
- Size can be specified exactly

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• Reference point can be chosen by using negative values for width and height



- Supports several modes
 - Stretching of shapes
 - Cutting of shapes

- Rounding off vertices
- Changing existing round off radius
- Modifying individual arc segments of a shape
- All modes within one command
 Including Oops support
- Additional features
 - Can also edit voids (Find Filter)
 - Supports single pick as well as window selection (several vertices)
 - Snap to grid, Trim to selection window
 - Display control (e.g. handle size)

ptions	д т
	FlowCAD
Licensed for:	
FlowCAD, Inte	rnal Use Only
Stretch/Cut m	ode
Stretch bo	undary
🔘 Cut bounda	ary
Snap to	arid
	selection window
	Selection #Indo#
Round Off mo	de
Round off	vertex
Change ro	und off radius
Badius	1 000
r (dalas	
Change arc m	node
🔘 Mofify indiv	vidual arc
CentX	- 1.000 +
CentY	- 1.000 +
Badius	- 1 000 +
Display contro	ol
Display contro Handle size	ol 0.500



Round Off mode Round off vertex

Radius

Change round off radius

8.000

- Use model
 - 1. Select the shape or void to be modified
 - 2. Select an action, e.g. Round off vertex
 - 3. Pick a vertex or drag a window to select the vertices
 - 4. Switch to other modes if necessary and continue
 - 5. RMB > Done







- Stretching of shapes
 - Specify offset if accurate stretch distance is needed



- Trim to selection window let's vou control stretch point origin





- Cutting of shapes
 - Adjacent segments of selected vertices will be deleted



- Trim to selection window simply cuts at the window boundary





• Round off vertex





- Change round off radius
 - Let's you change existing rounded off corners



- Can also restore original vertices by specifying a radius of 0.0





- Change arc mode
 - Parameters of existing arcs can be changed in Options panel. End points of adjacent segments will be adjusted automatically. Tuning possible by using +/- buttons





- Other highlights
 - Stretch / Cut on arc segments in conjunction with Trim option



- Round Off with adjacent arc segments





Shape Utilities – Priority

- Interactive application to modify the priority of a dynamic shape
- Use model

- Select shapes by subsequent picks
- Choose RMB > Complete selection to enter priority edit mode
- Use one of the options and select a shape to modify the priority
 - Highest
 - Increase one level
 - Decrease one level
 - Lowest
- Priority numbers are displayed dynamically

Change priority	
O Highest	
🔘 Increase one level	
🔘 Decrease one level	
🔘 Lowest	
Display control	
Text block 2	
Compact view	
Vpdate dvnamic shapes	





....

Shape Utilities – Check Status

- Utility to check and highlight island and dangling shapes
 - Islands: 0 connections

- Dangling shapes: Only 1 connection
- Such shapes can act as antennas and cause EMI issues

Options	
Layer	
📕 🔳 Тор 🗸 🔻	
—	
Island shapes	
Dangling shapes	
Limit view	
Check shapes	





Shield Generator

- Facilitates the generation of shape and via pattern for shielding purposes
- Includes shield rings along board outline (e.g. for ESD protection) as well as the generation of shield boxes for RF circuits

Shield Generator Shield Creation Mode Select Boundary Vidth 50.0000 Height 50.0000 Height 50.0000 Shield Settings Direction Inside Offset 2.5400 Yea Misc Create Symbol Yea Side Top
Ok Apply Help



Shield Generator

- Different modes for shield generation
 - Select Boundary
 - Draw Rectangle
 - Place Rectangle
 - Derive from Line
 - ...

- Shape parameters
 - Direction, offset, width, layers, ...
- Via parameters
 - Via gap, offset inside ring, initial offset, ...
- Mask generation and cutting capabilities for solder mask and paste mask
- Ability to create groups or symbols









Shield Generator

• Derive from Line

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 This mode allows you to use construction lines as template and derive shield structure. Useful if shield box has partitions with arbitrary segmentations

Shield Genera	tor
Shield Creation	in
Mode (Derive from Line 🔹 ?
Width	50.0000 Height 50.0000
Shield Setting	S
Direction	Inside 🔻
Offset	2.5400
Net	DGND
V Create SH	napes
Width	2.0000
Туре	Static -
Layers	Specify
🔽 Create Vi	28
Via Gap	2.5400 ?
Center Of	fset 0.0000 ?
Initial Offs	set 0.0000 ?
Padstack	Via0_3C0_7C
Croate M	ask
Side	
Misc	
Create Sy	
Suah Pure	2.040
	Annly Help
UK	стриу стер





 $(\)$

- Creates shield for critical signals in a semiautomatic way
 - Through interactive routing including dynamic preview
 - By selecting existing clines
- Support for side and tandem shields including parameters for gap and width and net name
- Support for dynamic or static shapes as well
 as route keepouts
- Advanced parameters can be used to control layers
 individually
- Parameters stored in database for each shield structure separately
 - Existing shields can be updated at any time without reentering information





- Default shield parameters
 - For regular applications
 - Side shielding (width and gap)
 - Tandem shielding (width) on adjacent layers only
 - Shape style and net name
- Advanced parameters
 - Can be used to define parameters for several layers individually
 - Export / Import settings for reuse purposes

	Shield O D C St St St V V V V V V	ing parameters efault Tandem shield Gap NA • Side shield Width 1.0000 Gap 1.0000 • yle Dynamic Shape et GND dvanced Param did all pads in keepon did static shapes	? ? ? eters					
Shieldro	oute Advan	ced Settings						
Side shielding Global Image: Create side shield Dynamic Shape • Width 3.0000 Gap 1.0000 • Image: Comparison of the state sta								
	Enable	Layer	Style		Width	Gap		_
1 2		SOLDERMASK_TOP	Static Shape	*	2.000	NA	•	-
3	×	L2	Dynamic Shape	•	4.000	NA	•	
4	×	L3	Dynamic Shape	•	5.000	NA	•	
6		L5	Dynamic Shape	•	2.000	NA	Ŧ	
7		воттом	Dynamic Shape	*	2.000	NA	•	
8	4	SOLDERMASK_BOTTOM	Static Shape		2.000	NA	-	T
/ia patt Name	ern	Padstack(s)	Param Add Ring o Del Via vii Up Initial Down Via st Aligan	neto offs a g off: ack	et 1.00 ap 1.00 set 0.00 coffset nt Con	00 00 00 tour ·		? ?
Angle 90.000 ? Ok Cancel Save settings Load settings Help								







• Routing shields interactively



Final structure once snapping to pin or via



- Updating existing shield structures due to routing modifications
 - Seamless update since parameters are stored in the database for each shield structure





- Creating combined shields for several contiguous clines
 - Through Temp Group command

- Parameter probe
 - Simply copy parameters from one structure to another
 - Parameters will be extracted and can be applied to other clines




Shield Routing

- Via pattern generation
 - Use Advanced Parameters form to specify
 - Multiple rings can be specified
 - Settings which apply to padstacks, offsets, alignment, angles, etc.





Shield Routing

- Advanced via pattern settings
 - Multiple padstacks (e.g. microvias)
 - Parameter for main stitching gap and gaps within in the stack
 - Staggering option





Shield Routing

• Microvia stacking within ring







45 deg inwards









Silkscreen

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- Powerful silkscreen utility
- Configuration

Objects to silk e.g. lines and labels can be configured as well as obstacles which require silk objects to be cut e.g. soldermask, keepout areas

Rules

Clearances and minimum segment length can be defined

🔀 Silkscreen	
General Elements: Constant Lines Source Specify Obstacles Specify Side Ton	ParametersMinimum line length0.25Min clearance0.10Undefined line width0.10Ignore text blocks?
Miscellaneous DRC -> Configuration -> Clear all data OK	Display control Global All off Limit ? Source T B Obstacle T B Drc Result T B Run Help







Silkscreen

• DRC

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Before generating silkscreen data, a DRC check can be performed, indicating all violations helping users to identify problems and fix them before actual data is generated





Snap Generator

- Creates persistent markers for snapping operations
 in PCB Editor
 - Reducing amount of travelling through context menus or using shortcuts
 - Using Snap pick to Persistent snap (Shape Center) then increases efficiency
- Basic markers
 - Origin, Center, Vertices, Midpoints
 - Intersections
- Advanced step markers
 - Divide / Incremental path stepping
 - Angular stepping for arc segments
- Derive path from objects for further processing
 - E.g. pad boundary, slot holes





SVG Export

- Generates SVG data out of PCB Editor
- Export SVG from current drawing
- Export SVGs for a complete footprint library including HTM report generation
- Profile support
 - Content (layers) and styles (e.g. colors, opacity, non-vectorized texts, etc.) can be specified using predefined profiles

VG Export	X
General	
Current drawing	
C Library	
Generate HTML report Portable (Standalone)	
Export directory	
D:/SVGExport	
Options	
Profile Current Visibility	
V Non-vectorized text	?
Preserve zoom level	
Apply Close Help	





SVG Export

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• Example for HTML library report

💱 SVG Export						
General						
Current drawing						
 Library 						
C:\Cadence\symbols						
Generate HTML report 📃 Po	rtable (Standalone)					
Export directory						
./SVGExport						
Options						
Profile symbol	•					
Non-vectorized text	nter labels ?					
Preserve zoom level						
Apply Close	Help					





Synchronize Testprep

- Automates the testpoint assignment in PCB Editor when dummy testpoint symbols (one-pin components with Refdes TP*) have been used in the schematic
- Generates testpoint on corresponding pin in PCB
- Post processing can then be done using PCB Editor Testprep functionality









Variant 3D

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- Application that supports 3D variants
 - Based on data from variants.lst
 - Single boards
 - Regular panels
 - Multi board panels

Name	Variant	P
DESIGN	CORE 🔻	D:/Demo/Variant3D/variants.lst
	CORE	
	ALL	
	SMT_ONLY	
	THT_ONLY	1
Close	Launch	3D Help



SMT_ONLY





Variant 3D

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• Multi board panels

🎛 Variant 3[) View	
Name	Variant	Path (variants.lst)
AMPLIFIER	V2	D:/Demo/Variant3D/AMP_variants.lst
2 SENSOR	V3 🔻	D:/Demo/Variant3D/SEN_variants.lst
	CORE V1 V2 V3	
Close	Launch	3D Help







- Gives customers even more flexibility when creating variant assembly views
- Features

- Automatic generation of all assembly variant views in one step
- Customizable label content, e.g. Refdes, Value, Part_Number with the ability to annotate two labels per component
- Customizable component outline, e.g. Assembly, Place_Bound, Silkscreen, ...
- Customizable style for DNI components, e.g. remove all or draw a thick cross through the label, ...
- Customizable style for Alternate components by using label prefix / suffix, changing colors or hatching component outline
- Supports rule based coloring of objects, e.g. all SMT in green
- Automatic mirroring of bottom view for better readability
- Settings stored in database



User interface

General	Drawing Options	Group Color	Advanced	
Generate	e Assembly View for			
Variant	ASIA	-		
File	D:/demo/variants.	lst		Load
DNI Part	s ify Style Remove	e All 🔻	Alternate Parts	Prefix Suffix
Mod	ify Color		📝 Modify Color	
Rem	nove second label		Modify Graphics	Hatch Shape 💌
OK	Conoreto	Cancol	Save to	Lond from Holn

对 Variant Ass	embly					
General	Drawing Options	Group Color	Advanced			
	Property		Value		Color	
1 REF	DES EC TYPE	 U5;U1 *0603 	1			
< []	1					7
Enable group color Variant color wins over group color OK Generate Cancel Save to Load from Help						



General	Drawing Options	Group	Color	Advanc	ed			
Bottom View			Addition	al layers				
Mode	Mirror to top	•	🔽 Inclue	de additic	inal lay	ers to varia	nt view	
Side	Right -		Top s	side	5	pecify]	
Space	10.000		Botto	m side	5	pecify]	
Misc			Gene	ral	5	pecify]	
🔽 Upda	te custom variables							
Ca	py labels to variant v	iew						
🔲 Full c	lean before update							
Write	view files (*.color)							



Customizable label content to be displayed (default is Refdes)



Customizable component outline to be displayed (default is Assembly)

Component Outline		
Annotate Assembly Assembly		
Use fixed out Place_Bound Silkscreen		
DISplay DNI Cross line V DFA_Bound	C64	C64
DNI Cross scale 1.0		
Hatch shape line width 0.100		
Hatch shape spacing 1.000		
	Assembly outline	Placebound outline



Available styles for DNI parts

Style "Remove All"



Style "Cross Graphics"

υ4

U 1

U 5

U 6

DNI Parts		
Modify Style	Remove All	-
Modify Color	Remove All Remove Label Cross Label	
Remove second	Cross Graphics	

Style "Remove Label"



Style "Cross Label"





Module: Variant Assembly

Available styles for alternate parts

Alternate Parts	Prefix [Suffix]
Modify Color	
✓ Modify Graphics	Hatch Shape 💌

Style "Modify Colors"



Style "Modify Labels"



Style "Modify Graphics"





Module: Variant Assembly

Rule based coloring of components



Variant	Assembly				
General	Seneral Drawing Options Group Color Advanced				
	Property	[Value	Ca	lor
	1 REFDES - U5;U11				🔺
2 J	EDEC_TYPE	*060	3*;*0805*		
					+
	III				•
	Enable group color	Var	iant color wins over	aroup color	
	2			9.040 00.01	
ОК	Generate	Cancel	Save to	Load from	Help

- Color rules can be linked to individual properties
- Several match pattern per rule
- Wildcard support



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Automatic mirroring of bottom view e.g. side by side to top view





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- Creates various reports (BOM) from layout database taking variant information into account
 - Generates reports (e.g. pick & place) data for a variant
 - Can be used for reports on core design also

Configurable content

- Any database attribute
- Ability to distinguish between common and variant parts
- Exclude BOM non-relevant parts (e.g. dummy testpoints)
- Header information, order of columns, column width
- Hierarchical sorting up to three levels
- Option to split output files
- Settings stored in database, export and import capabilities
- Output format
 - HTML, ASCII, CSV

User Interface

🙀 Variant BOM															
General Part Specif	ication Advanced														
Content		Report Format	t												
Variant name	ASIA 🔻	V Text	📝 Show Report												
Report name	Core Design Common All Variants	CSV	📝 Show Report	对 Variar	nt BOM						X				
Output directory	ASIA EUROPE	V HTML	📝 Show Report	Genera	al Part Specificat	on Advance	ed					-			
	USA			Nr	Paramet	er	Туре	Acc.	Width	Name					
Header Setup		Variant Option	s		1 ROWNUM	- Int	teger	0 -	-1	POS					
📃 Insert external	file	🗸 Report Un	ichanged		2 REFDES	- St	tring	0 -	-1	REF	Ħ	Variant BOM			
📝 Insert column n	ames	Report Alt	ternates		3 DEVICE_TYPE	- St	tring	0 -	-1	DEVICE					
		Benort DN	II		4 X	. ▼ Fl	loat	2 -	-1	SYM_X	G	Seneral Part Specification Advanced			
		- Report Dr			5 Y	- FI	loat	2 -	-1	SYM_Y		Miscellaneous	Sort Orde	er	
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	Di Jaharia Arrasia eta Int			/ MIRROR String U -1 MIRROR								Soperato by powling			
Variants File	D./demo/variants.ist			8 MOUNT_TYPE String U -1 MOUNTING					Decimal point dot 🔻 Units mm 🔻						
E									VIIFL			Split output files			
External Header												Text report			
												Extension bom	Level 2 <no sort=""></no>		
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OK Ge	nerate Cancel	Save to	Load from									CSV report		Split output files	
					Fueleda anda har	DOM ION			. ī	TD*			F F		
					<pre>Exclude parts by BOM_GNORE Value TP*</pre>					Separator 2	Level 3	<no sort=""></no>			
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				0	K Genera	ite (Cancel	Sav	ve to	Load from H	le	Use transformation rules Specify	Syr	mbol origin	
												JEDEC_TYPE rotation offset ?	🔘 Syr	mbol center	
											ſ	OK Generate Cancel	Save to	Load from Help	

File: D:/floware_demo/variant_assembly_bom/worklib/root/physical/master.html

Match word Match case

C1 CAP_805-120PF550V805 114.94 108.33 90.00

C2 CAP_805-120PF550V805 88.01 121.03 90.00

C3 CAP_805-120PF550V805 88.01 117.48 90.00

C4 CAP_805-120PF550V805 88.01 113.16 90.00

C5 CAP_805-120PF550V805 88.01 104.01 90.00

C6 CAP 805-120PF550V805 88.01 108.58 90.00

C7 CAP 805-120PF550V805 103.51 124.59 0.00

C8 CAP 805-120PF550V805 114.94 120.78 90.00

C9 CAP_805-120PF550V805 114.94 116.46 90.00

10 C10 CAP_805-120PF550V805 114.94 112.40 90.00 11 C11 CAP_805-120PF550V805 114.94 103.76 90.00

12 C12 CAP_805-120PF550V805 109.58 124.56 0.00

13 C13 CAP 805-120PF550V805 95.38 98.68 0.00

14 C14 CAP 805-120PF550V805 99.70 98.68 0.00

15 C15 CAP 805-120PF550V805 103.76 98.68 0.00

16 C16 CAP 805-120PF550V805 108.08 98.68 0.00

Text

SYM_X SYM_Y ROTATION MIRROR MOUNTING VI

NO

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Report Formats

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POS REF DEVICE



						É 🔳 F	ile: D:/flowa	re_demo/varian	t_assembly_bo	m/\	worklib/root/physical/master.csv	<u> </u>
						File	Close H	lelp				
Тех	t					POS 1;C 2;C 3;C 4;C 5;C	; REF; DEV 1; CAP_80 2; CAP_80 3; CAP_80 4; CAP_80 5; CAP_80 5; CAP_80	ICE; SYM_X; 5-120PF550 5-120PF550 5-120PF550 5-120PF550 5-120PF550 5-120PF550	SYH_Y; ROT V805;114. V805;88.0 V805;88.0 V805;88.0 V805;88.0 V805;88.0	<pre>FAT 94 11; 11; 11; 11; 11; 11; 11; 11; 11; 11</pre>	TION; MIRROR; MOUNTING; VTYPE 1; 108.33; 90.00; NO; SMT; BASE 121.03; 90.00; NO; SMT; BASE 117.48; 90.00; NO; SMT; BASE 113.16; 90.00; NO; SMT; BASE 104.01; 90.00; NO; SMT; BASE 104.01; 90.00; NO; SMT; BASE	× III
🔳 File	: D:/floware_dem	o/variant_as	ssembly_bom/worklib/root/pl	ysical/master.bo	m						;124.59;0.00;NO;SHT;BASE	
File	Close Help										:116.46:90.00;NO;SHT;BASE	
H++++ POS	REF DEV]	+++++++ [CE		SYM_X	SYM_Y	ROTATION	MIRROR	MOUNTING	******* VTYPE	^	94;112.40;90.00;NO;SMT;BASE 94;103.76;90.00;NO;SMT;BASE	
1 2 3 4 5 6 7 7	C1 CAP C2 CAP C3 CAP C4 CAP C5 CAP C6 CAP C7 CAP MOUNTING SMT	VTYPE BASE	PFF550¥805 PFF550¥805 PFF550¥805 PFF550¥805 PFF550¥805 PFF550¥805 PFF550¥805 PFF550¥805 PFF550¥805	114.94 88.01 88.01 88.01 103.51 114.94 114.94 114.94 109.58 99.70 103.76 108.08 121.79	108.33 121.03 117.48 113.16 104.01 108.58 124.59 120.78 116.46 103.76 98.68 98.68 98.68 98.68 98.68	$\begin{array}{c} \begin{array}{c} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 $	NO NO NO NO NO NO NO NO NO NO NO NO NO N	SHT SHT SHT SHT SHT SHT SHT SHT SHT SHT	HITHTH BASE BASE BASE BASE BASE BASE BASE BASE		58;124.56;0.00;NO;SMT;BASE 8;98.68;0.00;NO;SMT;BASE 76;98.68;0.00;NO;SMT;BASE 98;98.68;0.00;NO;SMT;BASE 79;123.06;0.00;NO;SMT;BASE 63;93.60;90.00;NO;SMT;BASE 5;124.59;0.00;NO;SMT;BASE 1;113.16;270.00;YCS;SMT;BASE 1;108.58;270.00;YES;SMT;BASE 1;108.58;270.00;YES;SMT;BASE 1;104.01;270.00;YES;SMT;BASE 1;104.01;270.00;YES;SMT;BASE 51;124.59;180.00;YES;SMT;BASE 1;104.01;270.00;YES;SMT;BASE 51;124.59;180.00;YES;SMT;BASE 51;124.59;180.00;YES;SMT;BASE 51;124.59;180.00;YES;SMT;BASE 51;124.59;180.00;YES;SMT;BASE	
)	SMT	BASE		127.63 93.85	93.60 124.59	90.00 0.00	NO NO	SHT	BASE BASE		94;120.78;270.00;YES;SMT;BASE 94.116.46:270.00;YES;SMT;BASE	
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)	SMT	BASE		95.38	98.68	180.00	YES	SHT	BASE	ŀ	0;98.68;180.00;YES;SHT;BASE 0;98.68;180.00;YES;SHT;BASE	-
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)	SMT	BASE										



- Hierarchical sorting
 - Up to three levels
 - Options to add newline for level 1 and level 2
 - Options to split output files for level 1 and level 2

-Sort Ord	ler
Level	1 VARTYPE -
	📝 Separate by newline
	Split output files
Level	2 MIRROR 🔻
	Separate by newline
	Split output files
Level	3 REFDES
Level	2 MIRROR ▼ Separate by newline Split output files 3 REFDES ▼

ł	🕻 VARI_4.bom (D:\vari_demo\mfg) - GVIM									x										
	Da	te	i Edit	tiere	n Werkz	euge Syr	ntax P	uffer	Ansicht	Н	ilfe									
E	3 6	3 (88	9 6) X 🗈 🖻	🗟 원 원	1	\$ T	a 🗆 🧿	2										
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P	05	I	REFDE	S I	DEVICE				I VTYPE	Т	MIRROR	Т	х		I	Y		I	ROT	
+	+++	++	+++++	++++	+++++++++++++++++++++++++++++++++++++++	*******	+++++	+++++	++++++	++•	++++++	+++	++++	+++++	+++	+++++	++++	++	++++++	
1		L	C1	- 1	CAPACITO	R_EL-10UF	, 20%, 1	6,4MM	I BASE	1	NO	1	-127	.000	Т	317.	500	L	0.000	
2		L	C2	- 1	CAPACITO	R_EL-10UF	, 20%, 1	6,4MM	I BASE	1	NO	I.	-119	. 380	T	317.	500	L	0.000	
3		I	C3	1	CAPACITO	R_EL-10UF	, 20%, 1	6,4MM	I BASE	1	NO 🥄	L	-111	. 760	L	317.	500	L	0.000	
4		L	UR3	1	MBZ5232B	_SOT23-BA	SE		I BASE	1	NO	I.	-101	. 600	Т	317.	500	L	0.000	
5		Т	UR1	<u>ا</u>	MBZ5232B	SOT23-BA	SE		I BASE	1	YES	1	-101	. 600	Т	325.	120	L	0.000	
6		L	UR2	1	MBZ5232B	SOT23-BA	SE		I BASE	1	YES 💌	V	-101	. 600	T	309.	880	L	0.000	
7		I	UR4	L	MBZ5232B	SOT23-BA	SE		I BASE	Т	YES	<u> </u>	-101	. 600	I	335.	280	L	0.000	
				.(3	0	-	6	D				\mathcal{C}	り							
8		L	R1 /	<u>۲</u>	RESISTOR	-22.1/2W.	5%		I CHANGE	1	NO	~~	-109	. 220	Т	307.	340	L	0.000	
9		i	R4 🧖	/i	RESISTOR	-56.1/2W.	5%		I CHANGE	÷ i	NO	i.	-109	. 220	Ì.	299.	720	Í.	0.000	
1	0	i	R6 /	í í	RESISTOR	-110.1/20	. 5%	\	I CHANGE	i i	NO	i	-101	600	i	302.	260	i	0.000	
1	1	i	R2	ī i	RESISTOR	-33.1/2W.	5%		I CHANGE	: È	YES	i.	-109	. 220	i.	335.	280	i	0.000	
1	2	i	R3	i	RESISTOR	-47.1/20	5%		I CHANGE	i i	YES	i	-109	220	i	325.	120	i	0.000	
li.	3	i	R5	i	RESISTOR	-68.1/2	5%		CHANGE	i i	YES	i	-111	760	i	330	200	i	0.000	
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																21,0	-1		Alles	5



- Transformation rules
 - Sometimes users need to transform x, y and rotation due to Pick & Place requirements from manufactory
 - E.g. always subtract 360 from angles given by PCB Editor for components on BOTTOM side
 - Formulas can be specified for TOP and BOTTOM separately
 - Unit specifiers such as MM, MILS etc. are supported

	Footprint location							
	XY at	Symbol or	rigin 🔘	Symbol ce	enter			
	V Tra	insform X,Y,an	gle	Spec	ify			
🔰 Varia	nt BOM					x		
-Top s	ide		Botton	n side				
X =	x		X =	(100 MM) - x			
Y =	У		Y =	У				
Rot	= rot		Rot =	- 360 - rot				
Info				(200 (=		
Note: greate Note: value:	Variant BC er than 360 You may a s are um, n	DM always subtra degrees Ilso use unit spe nm, mil, inch and	acts multiple cifiers in you I cm.	of 360 for a	angles equal (. possible	or		
	Close		Cancel		Help			



Z-DRC

- Checks clearances along the Z-axis
- Useful for applications which have to meet safety and explosion requirements
- Objects to be checked can be specified on net or netclass basis in any combination
- Spacing value can be specified manually or derived from DRC system (Constraint Manager)
- Graphical DRC: Markers & Overlapping
- Cross probing and filter capabilities



🛃 ZDRC								
Main Output								
Spacing value	Group A [Class/Nets]	Group B [Class/Nets]						
DRC system	ALL CLASS -	ALL CLASS -						
Fix 13.000	ANALOG_SPACE CLS1 CLS2	ANALOG_SPACE CLS1 CLS2						
Layer distance calculation	NO_TYPE	NO_TYPE						
🔘 Include all Cu layers								
Exclude external Cu								
C Exclude all Cu								
All dielectric thicknesses within current ZDRC layer	Limit coloction to:	Limit coloction to:						
from layers **between** the	Start TOP -	Start TOP V						
	End BOTTOM -	End BOTTOM -						
OK ZDRC Update -> Clear All Help								



Z-DRC

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• The negative margins (amount of overlapping) can be displayed once a DRC has been selected in the Output tab



ZDRC		
Main Output DRC List 1 (5371.247 2422.238) N12V ↔ 2 (5339.376 2700.0) N12V ↔ 3 (5338.876 2700.0) N12V ↔ 4 (5338.876 2700.0) N12V ↔ 5 (5851.501 3132.001) N12V ↔ 6 (5944.0 3199.6) N12V ↔ 7 (6174.376 3375.0) N12V ↔	P24V IS1 ↔ IS2 L-L req: 13 24V VCC ↔ BOTTOM L-V re 24V VCC ↔ IS2 L-V req: 13. 24V IS1 ↔ IS2 L-V req: 13. 24V IS2 ↔ IS1 L-L req: 13.000 12V BOTTOM ↔ VCC L-P re	.000000 2q: 13.000000 00000 00000 .000000 000 2q: 13.000000
DRC Filter Layer: ALL Type: ALL Net: *	DRC Visit V Zoom 25 % Limit layers Display overlap	Reports DRC Errors Layer distances
OK ZDRC Up	odate -> Clear Al	l Help



FloWare Modules Schematic Entry

OrCAD X Capture / Allegro X Design Entry CIS



FloWare Modules Schematic Entry

- Flat Net Utilities
- Smart Aliases
- Split Wire

- <u>Testpoint Check</u>
- <u>Tortoise SVN Integration</u>
- Update Titleblock



- TCL applications with features to report and display the complete physical net (flat net) over all pages
- Very useful for review purposes when working with hierarchical designs
- Fully integrated into standard operations (e.g. select)
- Features

- Report the physical net name in the command window while selecting wires in the canvas
- Display the physical net name in tooltip
- RMB > Highlight / De-highlight physical net over the full hierarchy



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Physical net name report





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Tooltip reporting physical net name





• Highlight / De-highlight physical net on all pages / hierarchies





Analog subblock





- TCL application with smart editing and highlight capabilities when working with user defined signal names (aliases)
- Features

- Dynamic highlighting of unnamed wires
- Dynamic highlighting of wires with multiple different signal names
- Smart rename when editing a signal name





• Dynamic Highlight



Different signal names on same "wire"



e.g. Rename MY OUT to OUT1

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Smart Rename: Keeps signal names in sync even if signal names have been assigned at multiple locations





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• Smart Rename: Even helps resolving conflicts when different signals names were present



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Split Wire

- Provides automatic wire split when components (e.g. resistors) are placed / dropped on wires
- Enable / Disable through context menu




Testpoint Check

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- Check testpoint coverage for whole design
- Based on user-defined testpoint components (e.g. One-pin components TP*)
- Configurable search criteria
 - Reference = TP*
 - Value = Testpoint
- Status report

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Datei Editieren Werkzeuge Syntax Puffer Ansicht Hilfe		
m tag.tcl + (c./cadence/s-b_10.0//capinoware/coning/theneck) - Gviw		



	flw_tpcheck.txt - Editor	_ Ο Σ	3					
	Datei Bearbeiten Format Ansicht ?							
	Testpoint Check Report		•					
	Design: FLOWCAD_CIS.DSN							
	Date: April 02 10:51:56 2015							
	Untested nets: 4 +15V -15V 0.75VREF 0.75VTT 0.9VREF 0.9VTT							
	Testet nets: 382 DB0 TP10 DB1 TP23 DB10 TP47 DB11 TP58 GND TP30, TP31, TP345							
-			Ŧ					



Features

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- Import a project to a SVN directory
- Committing your project to the server
- Load the latest project version from the server
- View the log-file
- Checkout a directory
- Lock / unlock a project
- Compare only with CIS license
- Each command is directly available in Capture
- This module always use your entire project directory

Prerequisites

- Tortoise SVN (Open Source)
- SVN Server (Open Source)



Use model: Creating a new project



* Commands launched from the Capture TortoiseSVN interface

Use model: During the daily use

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* Commands launched from the Capture TortoiseSVN interface

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• When committing a project, you can add messages which will be stored on your server, for example:

TortoiseSVN Interface	
Copyright FlowCAD Licensed for: FlowCAD Sch	nweiz
COMMIT	
UPDATE	
IMPORT	
CHECKOUT	
SHOW LOG	
REPO-BROWSER	
LOCK	
UNLCOK	
COMPARE	
HELP	



• View the log messages on your project history

A Log Messages - TESTCDNLIVE.DSN	×	
From: 06.05.2011 🔽 To: 06.05.2011 💌 🔎 Messages, authors and paths		3
Revision Actions Author Date Message		
S7 Marco 13:47:50, rreitag, 6. Mai 2011 Monneo L 3: 54 Marco 13:45:27, Freitag, 6. Mai 2011 Added R3! 53 Marco 13:35:27, Freitag, 6. Mai 2011 Added R3!		TortoiseSVN Interface
52 A Marco 13:34:45, Freitag, 6. Mai 2011 51 A Marco 13:30:42, Freitag, 6. Mai 2011		Copyright FlowCAD
For complete history deselect 'Stop on copy/rename'		Licensed for: FlowCAD Schweiz
		COMMIT
Modified C3!		UPDATE
		IMPORT
		CHECKOUT
Adding [Bulk] [Constant [Bulking]]		SHOW LOG
Action Path Copy from path Revision Modified (CDNLTVE/TESTCDNLTVE.DSN Modified (CDNLTVE/TESTCDNLTVE.op)		REPO-BROWSER
Modified (CDNLIVE/TESTCDNLIVE_0.DBK		LOCK
		UNLCOK
Showing 5 revision(s), from revision 51 to revision 57 - 1 revision(s) selected. Image: Hide unrelated changed paths Statistics		COMPARE
Stop on copy/rename		HELP
Show All V Next 100 Refresh		



• Design Compare:

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The latest version from the SVN Server will be compared with your local version

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🖧 -6 🖻					
Object	Object Type/Value	Object	Object Type/Value		
Objects from E:/TEMP/TESTDIFF/PROJECTI	LDSN	Objects from E:/TEMP/TESTDIFF/Diff/PROJECT.	Objects from E:/TEMP/TESTDIFF/Diff/PROJECT1.DSN		
E:\TEMP\TESTDIFF\PROJECT1.DSN	Design View	E:\TEMP\TESTDIFF\DIFF\PROJECT1.DSN	Design View		
SCHEMATIC1	SCHEMATIC_VIEW	SCHEMATIC1	SCHEMATIC_VIEW		
PAGE1	SCHMATIC_PAGE	PAGE1	SCHMATIC_PAGE		
⇒ TitleBlock	Schematic_Title_Block	TitleBlock	Schematic_Title_Block		
⊳ <mark>U1</mark>	COMP_INSTANCE	⊳ <mark>U1</mark>	COMP_INSTANCE		
▶ U2	COMP_INSTANCE	b U2	COMP_INSTANCE		
Þ U?	COMP_INSTANCE	NOT_PRESENT			
Local	version	Version from t	Version from the SVN Server		

• This command works only when you have a CIS license



Update Titleblock

- Automatic update of titleblock properties
- Driven by external configuration file customvar.cfg
- Variant aware

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