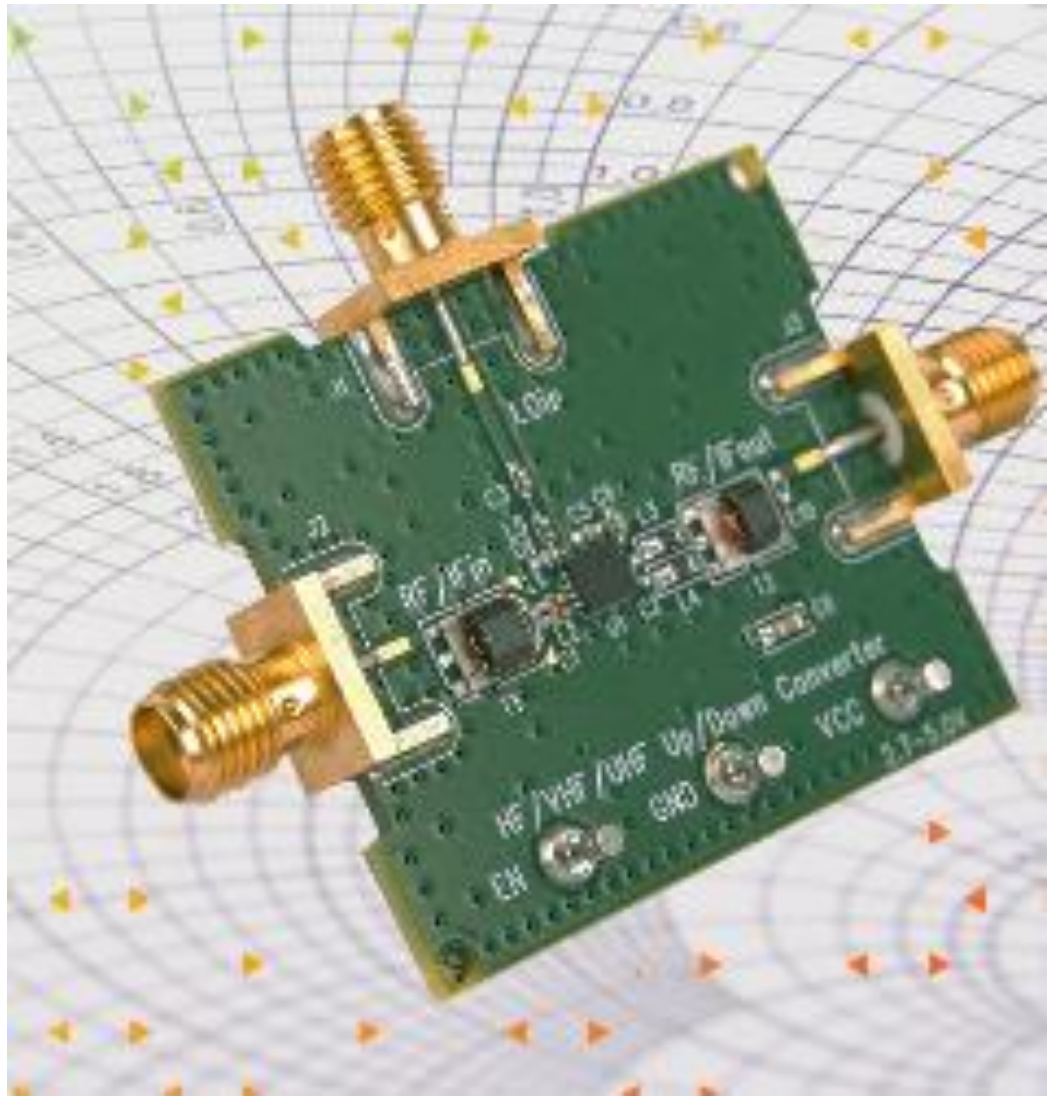
RF Design Techniques

Design and Manufacturing



Today's Speakers

Ernie Frohring
Field Application Engineer, EMA Design Automation

Ernie has worked with various PCB layouts, schematic capture, analog simulation, and signal integrity analysis tools and is especially interested in integrating these tools into a design environment.

He is currently specializing in RF and digital simulation, doing presentations, and working one-on-one with customers using EDA tools from Cadence and EMA Design Automation.

He graduated from the Massachusetts Institute of Technology with a Bachelor's and master's degree in Electrical Engineering. His hobbies include chasing total solar eclipses to interesting parts of the world.

Amit Bahl
Chief Revenue Officer, Sierra Circuits

Amit, widely recognized as the PCB Guy, serves as the Chief Revenue Officer at Sierra Circuits. He earned his Bachelor of Science in Engineering from UCLA in 1997.

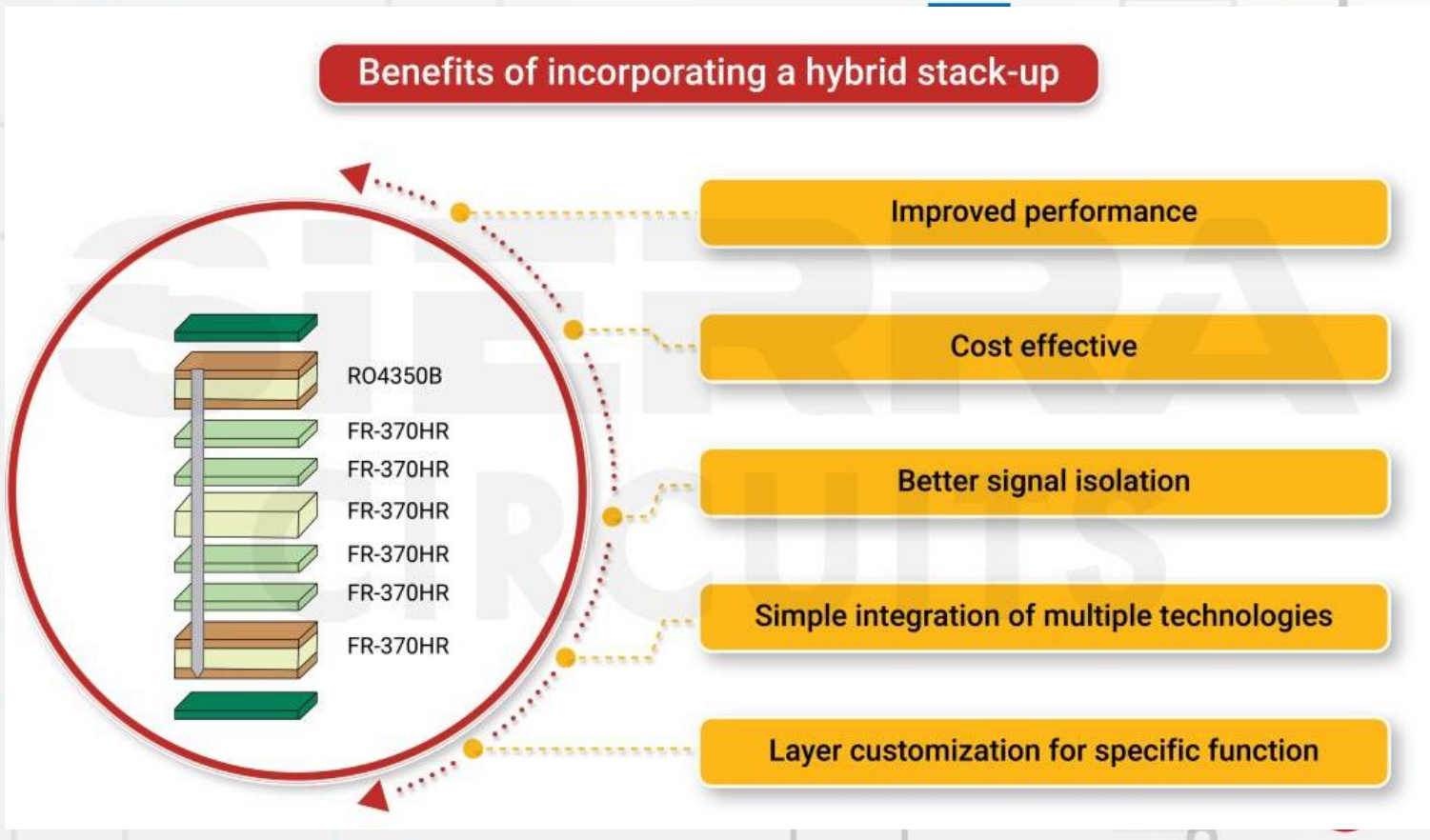
As the CRO since 2022, Amit successfully propelled Sierra Circuits to become a leading educational platform for all aspects of PCBs. Under his leadership, Sierra expanded to offer blogs, design guides, webinars, calculators, design tools, and a vibrant forum, SierraConnect.

What you'll learn

1. PCB Stack-up Materials
2. Impedance Matching
3. Types of RF Traces
4. Via-stitching and Ground Planes
5. Power Supply Decoupling

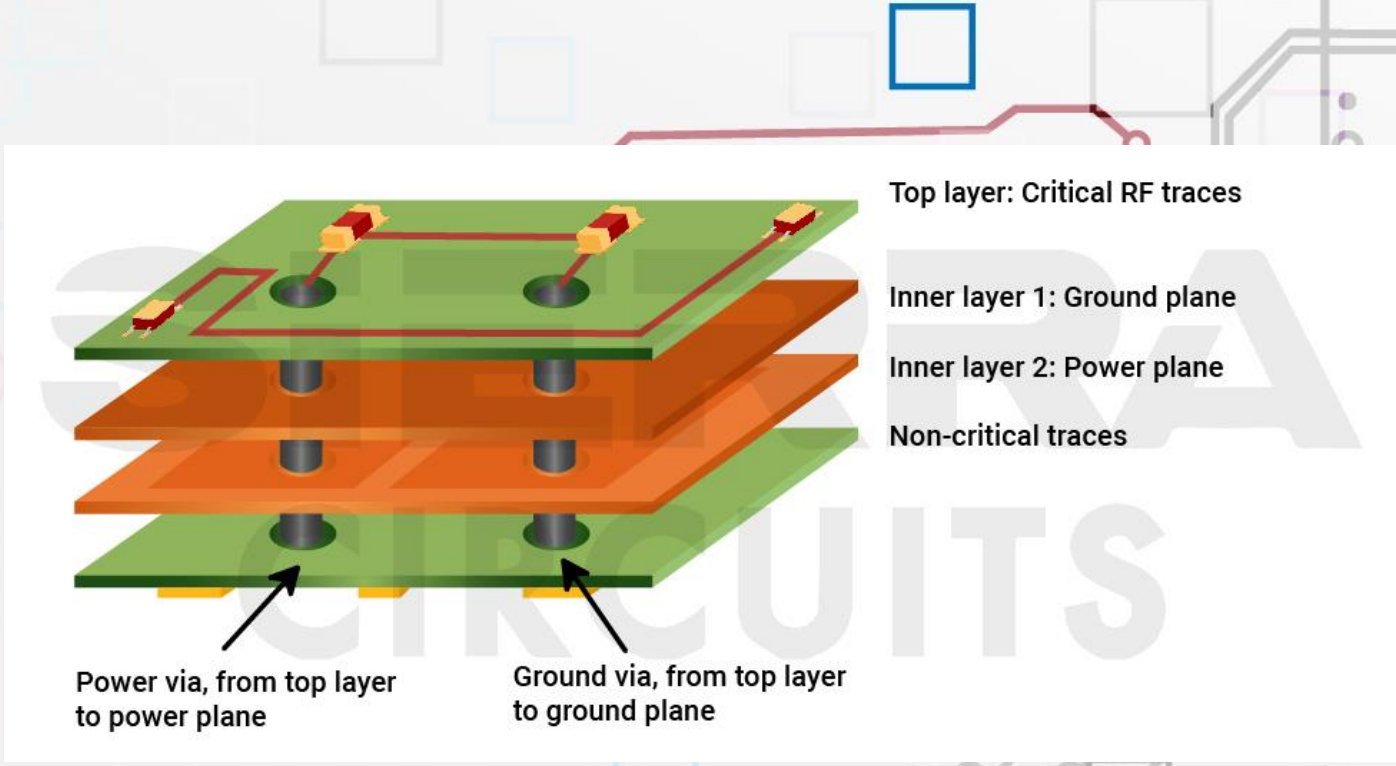
How hybrid stack-up benefits RF designs

- Ensures controlled impedance and solid return path for RF signals
- Allows you to incorporate low D_k materials exclusive to RF layers to reduce signal loss and attenuation
- Isolates sensitive RF circuits and noisy digital components by using high-D_k materials in specific layers
- Easily integrates analog and digital circuitry, RF components, sensors, and microcontrollers. This reduces board complexity and cost



5 design tips to build an efficient hybrid stack-up

1. Choose materials with a low dielectric constant (3 to 3.5) and a low loss tangent (0.0022 to 0.0095 for 10-30 GHz frequency)
2. Make sure the CTE of the dielectric material matches the CTE of your copper foil
3. Ensure optimum dielectric spacing (3 to 10 mil) between the signal, power, and ground layers to manage impedance mismatches, crosstalk, and EMI
4. Group the signal layers based on their operating frequencies for efficient signal transmission
5. Place the RF signals on external layers with adjacent ground planes



Route RF traces on the external layer of your hybrid stack-up

Suitable materials for hybrid stack-ups

FR4

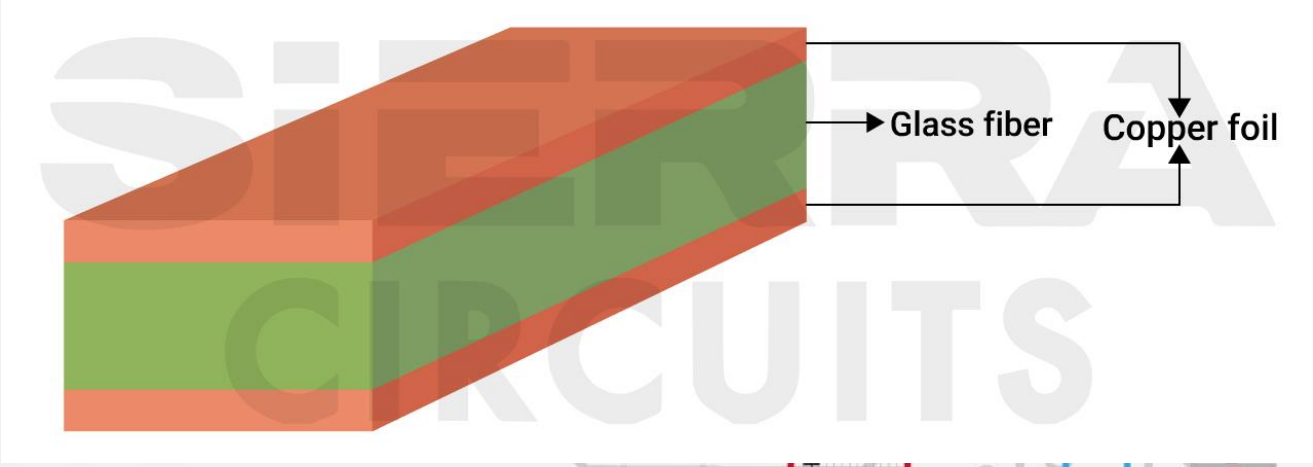
- These materials are combined with low-D_k laminates to build RF boards
- Preferred for high-frequency operations since they offer:
  - Uniform impedance control
  - Better heat conductivity
  - Consistent D_k and D_f over a wide frequency range
- Typical example: FR370HR, FR408HR

PTFE (Teflon)

- Offers better impedance control and low signal loss
- Undergoes dimensional changes as it is a softer material
- Requires a plasma treatment process
- Expensive compared to FR4
- Typical example: Rogers, AGC, Ventec materials

Ceramic-filled PTFE

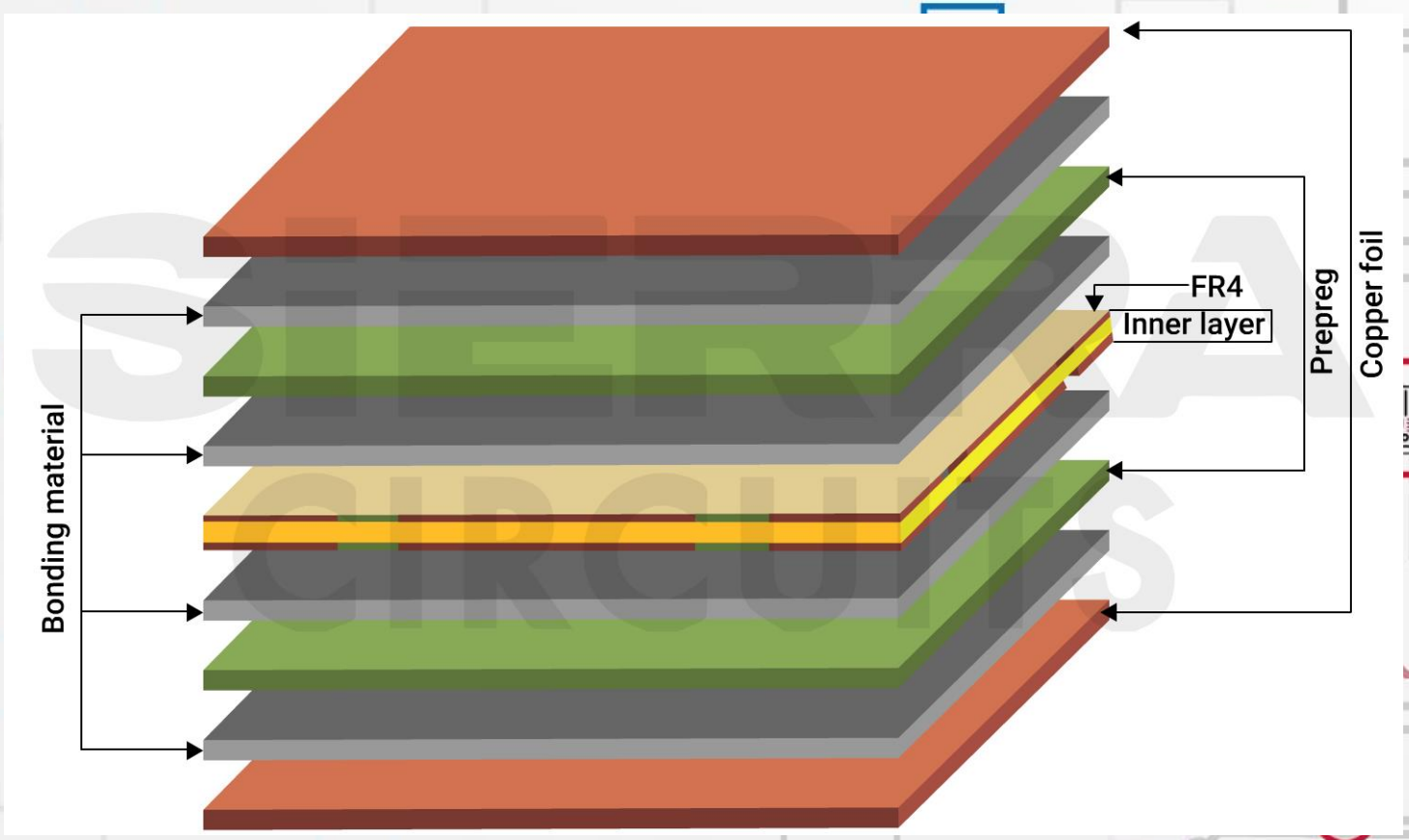
- Exhibits lower signal losses
- Offers a stable D_k and better structural stability
- Typical example: RT/duroid (5870, 5880, 5880LZ, and 6002) and RO3000 (RO3003, RP3003G2, RO3006, RO3010)



FR4 has reinforced glass fiber cloth with copper foils on both sides

Bonding materials used for hybrid stack-ups

- Standard adhesives cannot bond dissimilar materials in hybrid stack-ups
- Choose a bonding material with low lamination and re-melt temperatures
- Typical bond plies include:
  - Fluorinated ethylene propylene (FEP)
  - Ceramic-filled PTFE
  - Liquid crystal polymer (LCP)
- Check with your manufacturer before finalizing the type and thickness of adhesive material
- Hybrid stack-ups are cost-effective only when one type of prepreg is used to bond hybrid cores. For example, Roger 4350 and 370HR cores are bonded with 370HR prepreg



Bonding material helps securely bond copper foils and insulating substrates, creating a single integrated PCB structure.

4 fabrication challenges in building a hybrid stack-up

1. Incomplete laser ablation

FR4 materials generally pose no obstacles for laser drilling. However, PTFE is UV transparent, so it won't absorb the laser energy required for ablation, causing inaccurate drilling

2. Inconsistent scaling

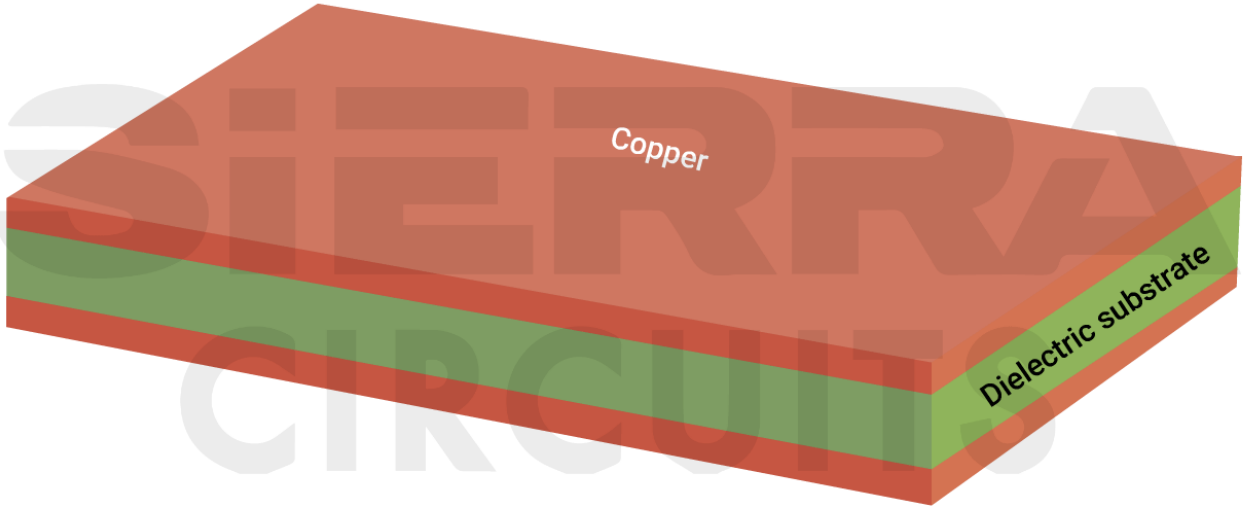
Scaling becomes challenging as each material in hybrid stack-up has different movement characteristics during lamination

3. Material misalignment in sub-assembly lamination

Sub-assembly integration increases complexity during multiple lamination cycles. The material might shift slightly with each press

4. Weak bonding during lamination

Achieving a solid bond during lamination can be difficult as different materials have distinct melt/flow characteristics and respond differently to temperature fluctuations

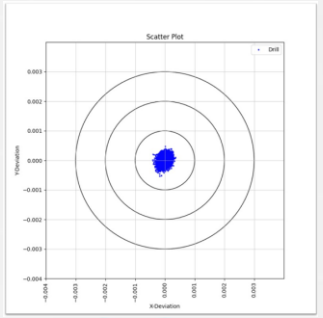


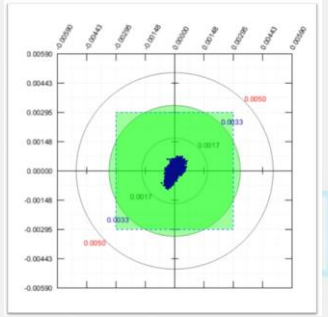
Weak bonding between copper plating and dielectric substrate causes delamination

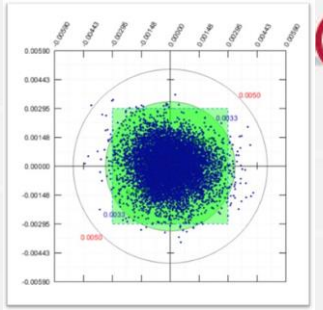
How Sierra Circuits can help you create a reliable hybrid stack-up

- Carbide or diamond-coated drill bits for precision drilling
- CO_2 lasers to avoid incomplete laser ablation in PTFE materials
- Laser parameter monitoring (wavelength and pulse duration) to enhance absorption on smooth PTFE surfaces
- XACT software simulation to predict scale values and adjust drill parameters for hybrid stack-up
- X-ray inspection to detect voids and weak spots
- Appropriate metallization of the exposed dielectric to eliminate voids and hole-wall detachment
- Substrate surface preparation with plasma etching techniques for improved adhesion

CO_2 laser drilling, XACT software simulation, and X-ray inspection at our shop floor to fabricate an efficient hybrid RF stack-up





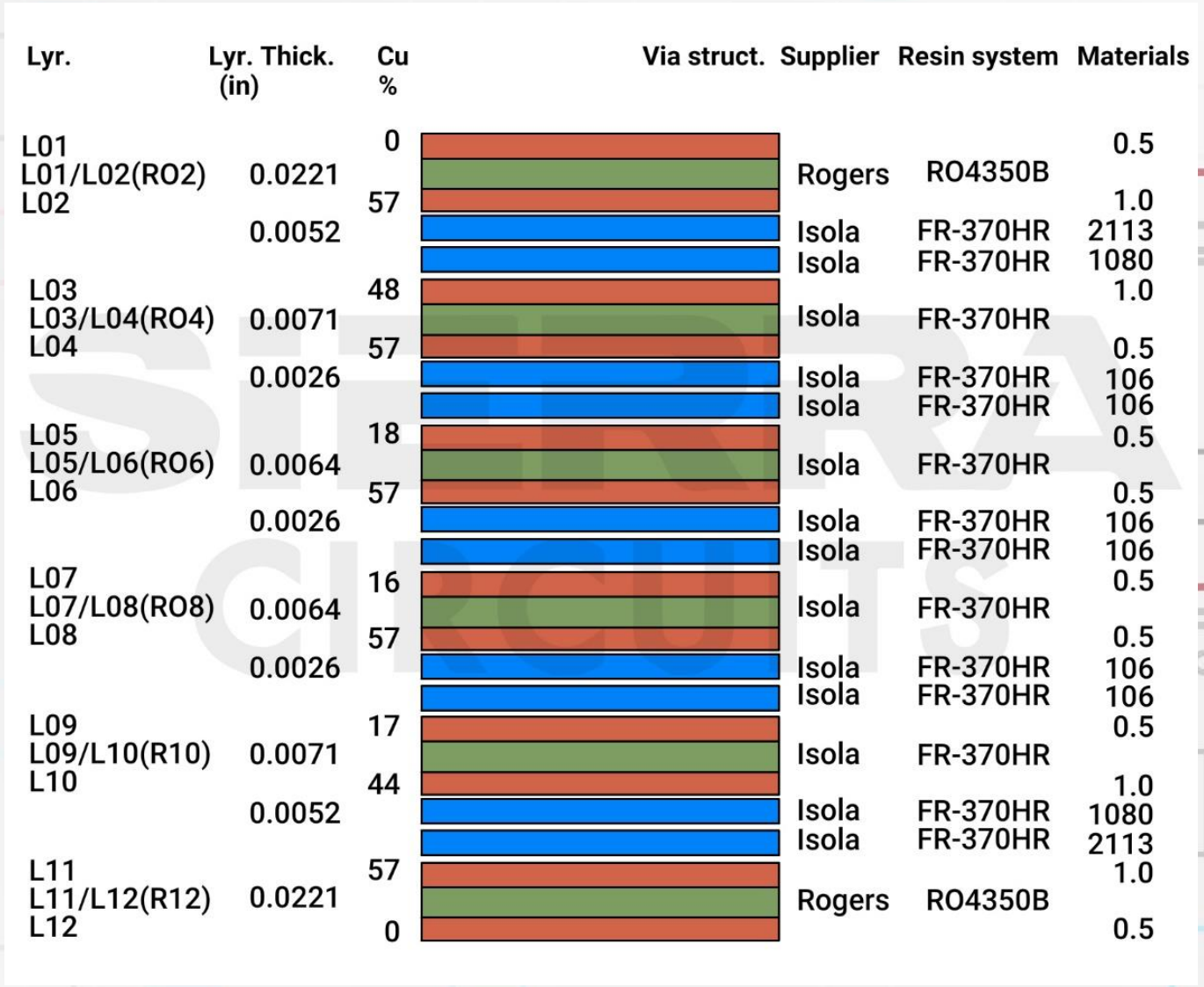


Examples of mixed material/hybrid stack-ups

Lyr.	Lyr. Thick. (in)	Cu %	Via struct.	Supplier	Resin system	Materials
L01		50				0.5
L01/L02(RO2)	0.0221			Rogers	RO4350B	
L02		54				1.0
	0.0026			Isola	FR-370HR	106
				Isola	FR-370HR	106
L03		51				1.0
L03/L04(RO4)	0.0058			Isola	FR-370HR	
L04		51				1.0
	0.0026			Isola	FR-370HR	106
				Isola	FR-370HR	106
L05		19				1.0
L05/L06(RO6)	0.0058			Isola	FR-370HR	
L06		54				1.0
	0.0000			Rogers	RO4350B	4450T
--/L07(RO8)	0.0054			Rogers	RO4350B	
L07		18				1.0
	0.0000			Rogers	RO4350B	4450T
				Rogers	RO4350B	4450T
L08		54				1.0
L09/L09(R10)	0.0221			Rogers	RO4350B	
L09		50				0.5

9-layer board with two sub-assemblies and 5 layers of PTFE (RO4350 B)

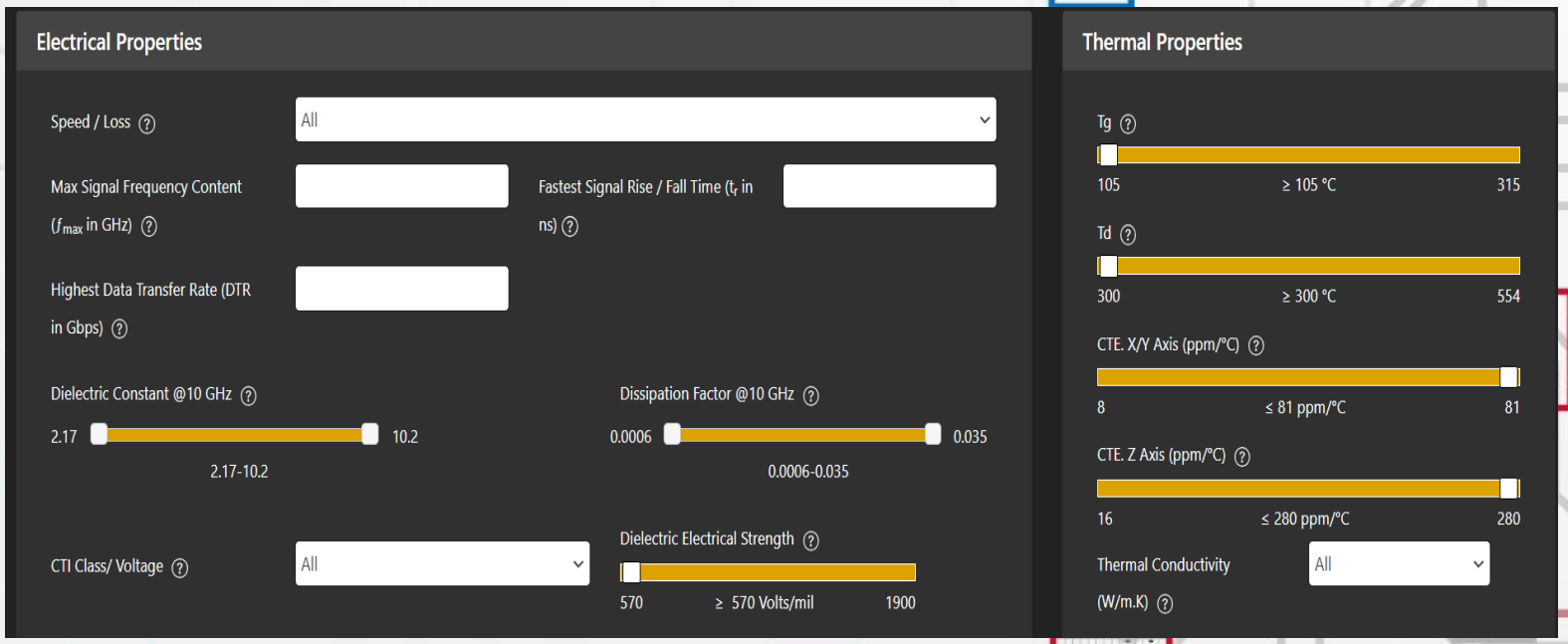
Examples of mixed material/hybrid stack-ups



12-layer board with PTFE (RO4350B) on the outer layers

Sierra Circuits' PCB Material Selector

- It features 50+ rigid materials and 10+ flex materials
- The tool can quickly find the materials (rigid or flex) suitable to your application
- Provides datasheet for any given material instantaneously
- Allows you to compare materials that fit your application criteria such as IPC revisions, slash numbers, T_g, D_k, and lead-free compatibility

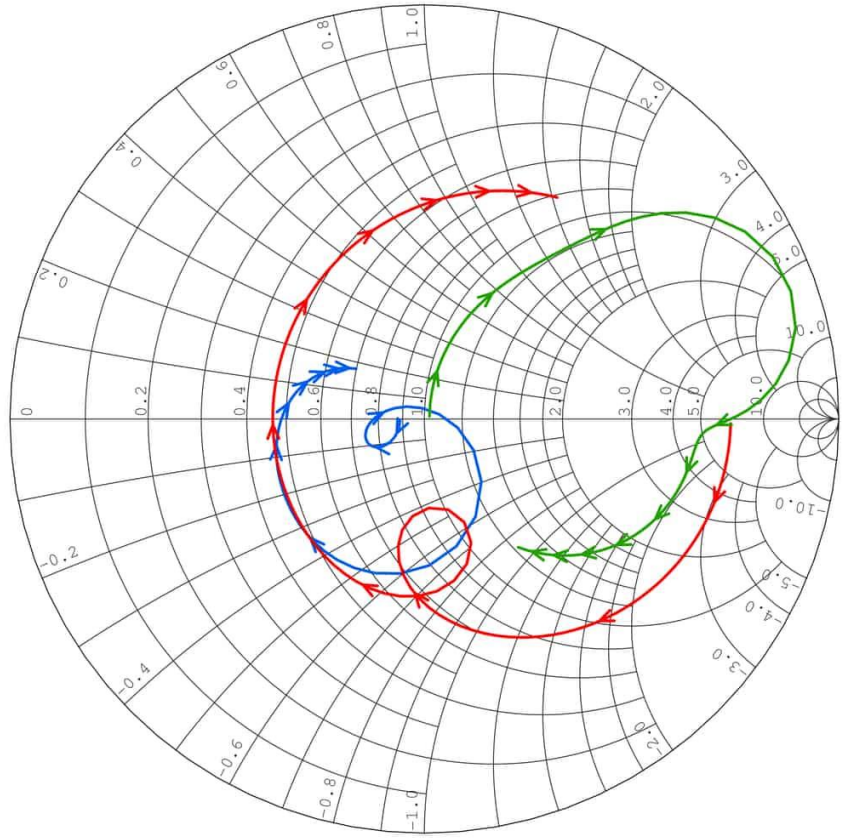


Sierra Circuits' PCB Material Selector

5/21/2024

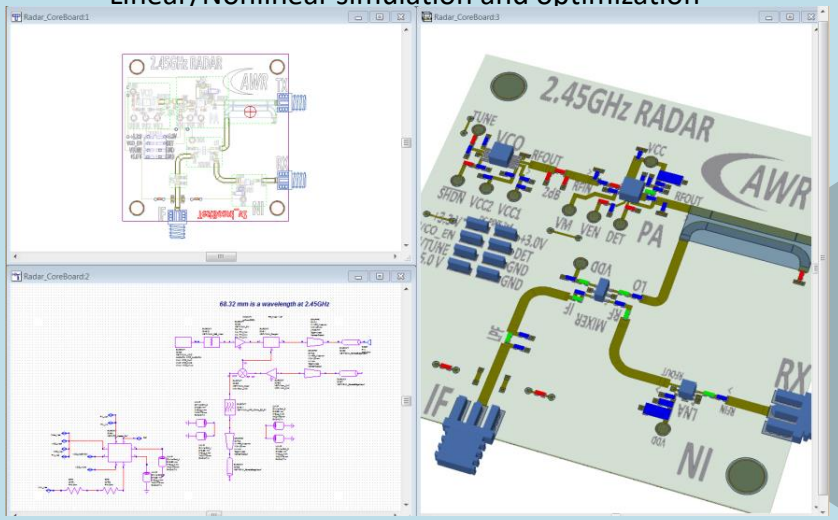
Impedance Matching

- For digital signals impedance matching is important in order to avoid reflections and signal distortion
- Controlled impedance (Z_0) depends on geometry of the traces, the dielectric constant of the PCB material, and height from the reference ground plane.
- In a controlled impedance RF circuit characteristic impedance (Z_0) matching enables the maximum power transmission and minimizes distortion
  - For example, matching the input impedance of an antenna

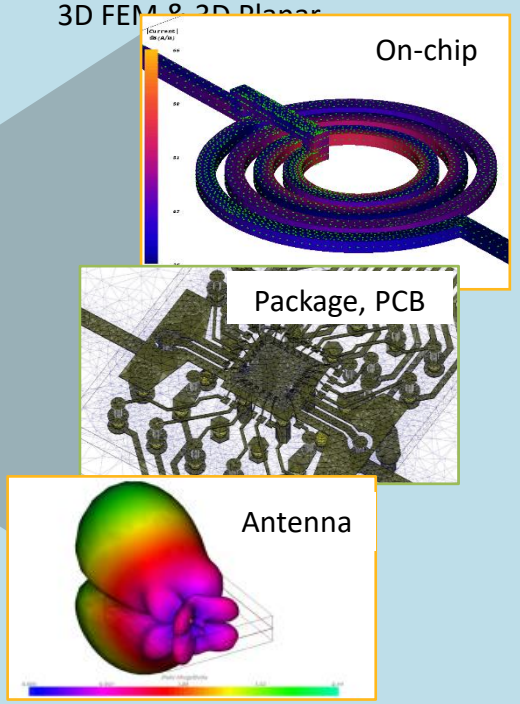


RF Design with Fully Integrated EM Analysis - Demonstration

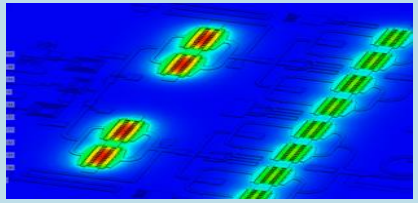
RF Circuit Design & Analysis
for Front-end Component Development
(Microwave Office)
Linear/Nonlinear simulation and optimization



EM Analysis
for S-parameter Extraction & Antenna Design
(Clarity, Analyst, AXIEM, EMX)
3D FEM & 2D Planar



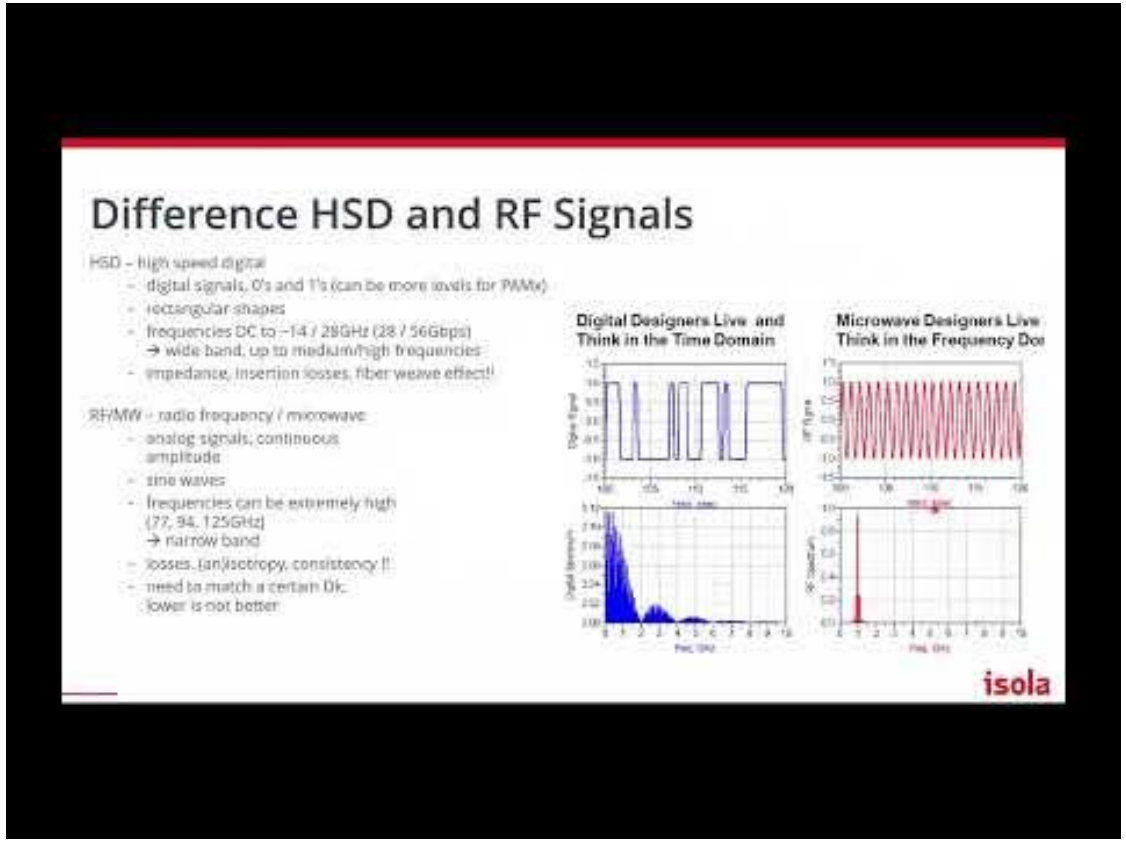
Thermal Analysis
For power dissipation
(Celsius)
FEA Solver



Cadence AWR Design Environment

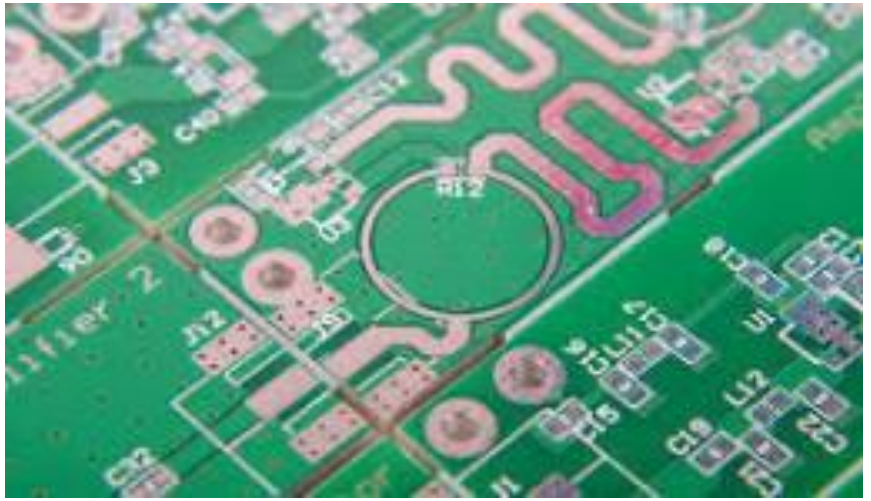
Material Selection - Webinar

- For more information on stack-up materials go to the Sierra Circuits on-demand webinar “Choosing the Right Material for Your RF PCB Designs” with Alexander Ippich from Isola Group.
- https://www.protoexpress.com/webinars/choosing-the-right-material-for-your-rf-pcb-designs



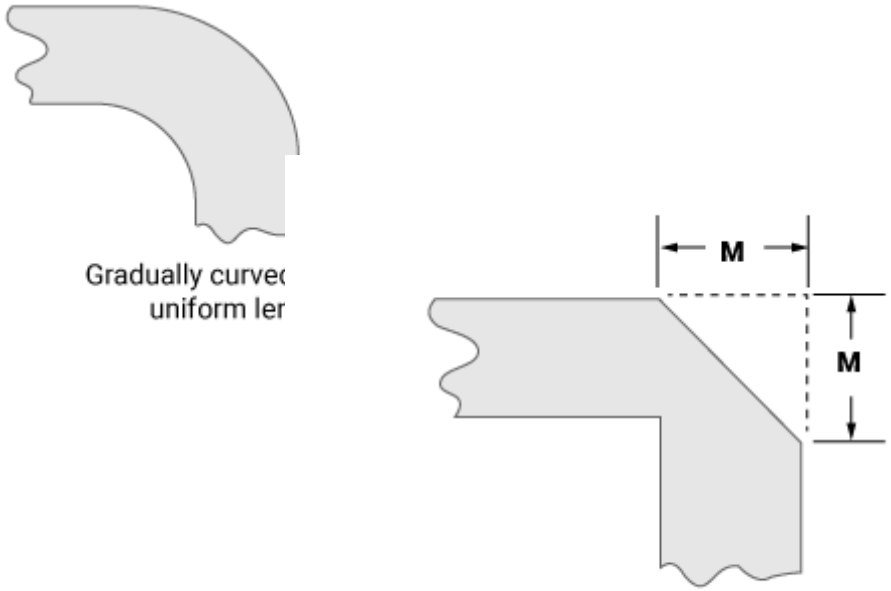
RF Trace Design

- The length of the trace should be as short as possible to reduce attenuation.
- In the layout, never place an RF trace and a normal trace parallel to each other.
- Ground planes are required to provide return paths for signals.
- The test points are not supposed to be placed on the traces. It will interrupt the impedance matching values of the trace.



Types of Transmission Lines

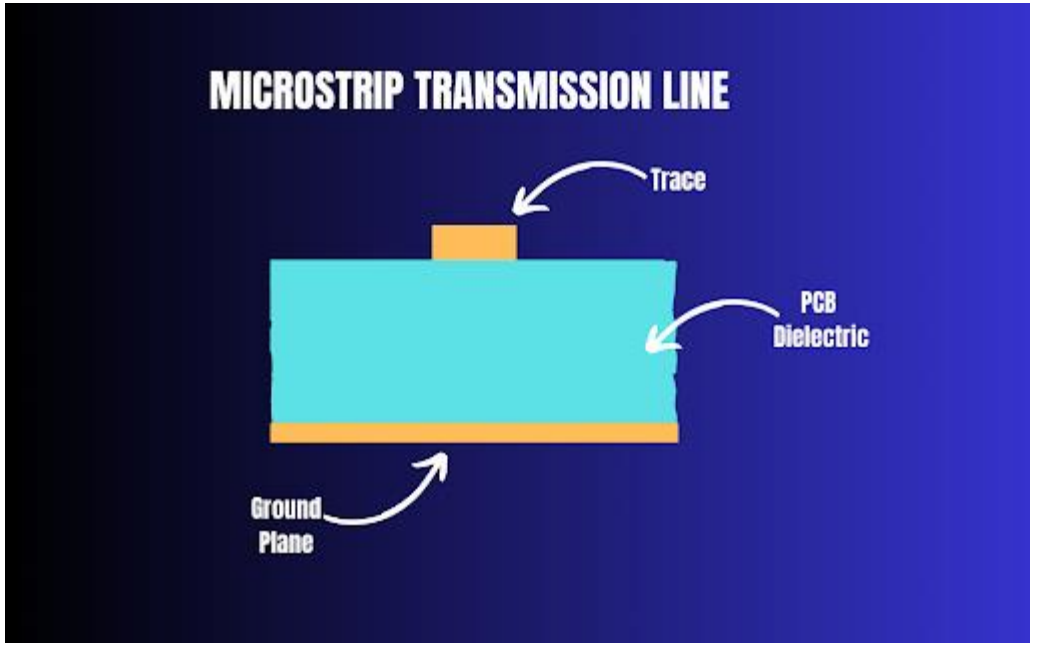
- The most common types of transmission lines designed are coplanar waveguide (CPWG), microstrip and stripline.
- Instead of keeping sharp right turns, gradually curved bends are better for trace performances.
- In cases where right-hand bends are unavoidable, a process called metering is used.



$$M = W\,(1.04 + 1.3 \times e^{\left(-1.35\,\frac{W}{H}\right)})$$

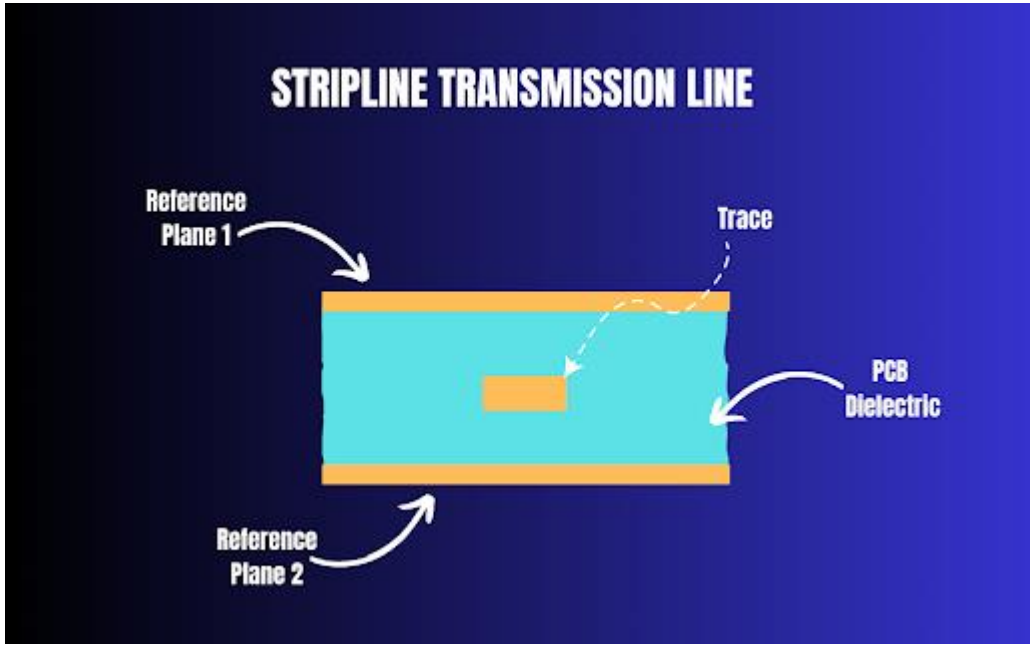
Microstrip Transmission Line

- Microstrip transmission lines are popular in RF PCB design due to their simplicity and ease of fabrication.
- They consist of a signal trace on top and a ground plane at the bottom, separated by a dielectric material.
- Trace width, spacing, and the dielectric constant of the substrate are critical for achieving the desired characteristic impedance.



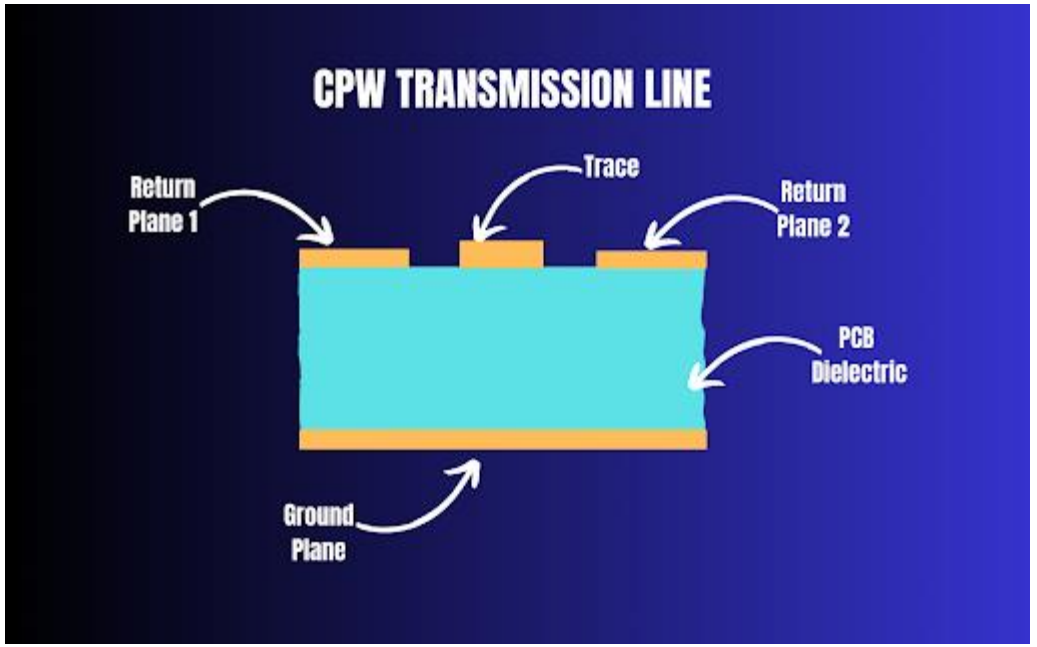
Stripline Transmission Line

- The signal trace is embedded between two parallel ground planes.
- The signal trace is routed on the inner layer of the board, surrounded by dielectric layers.
- Stripline transmission lines offer two return paths for the signal.
- They enhance signal integrity and are commonly used in RF PCB designs where better isolation or impedance control is crucial.



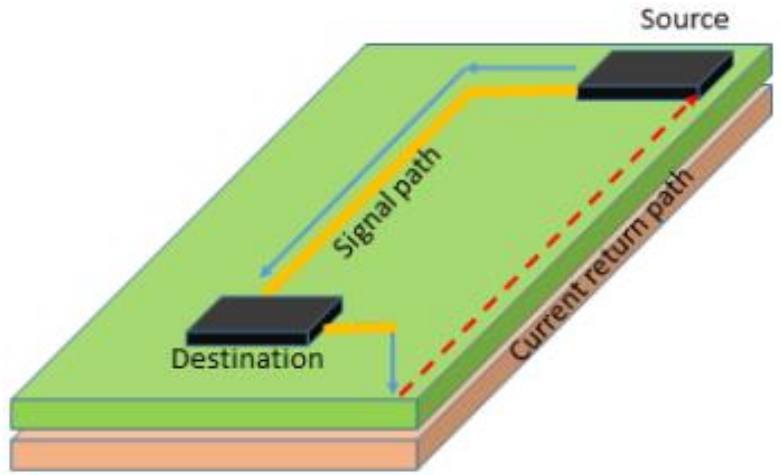
Coplanar Waveguide (CPW) Transmission Line

- CPW transmission lines have the signal trace and two return planes on the same layer.
- The dielectric material isolates the trace signal from the return planes, providing excellent isolation between adjacent transmission lines.
- EMI (Electromagnetic Interference) effects are minimized.
- Wider trace widths for lower losses.
- Frequently used in RF PCB designs where low insertion loss, good isolation, and ease of fabrication are crucial.



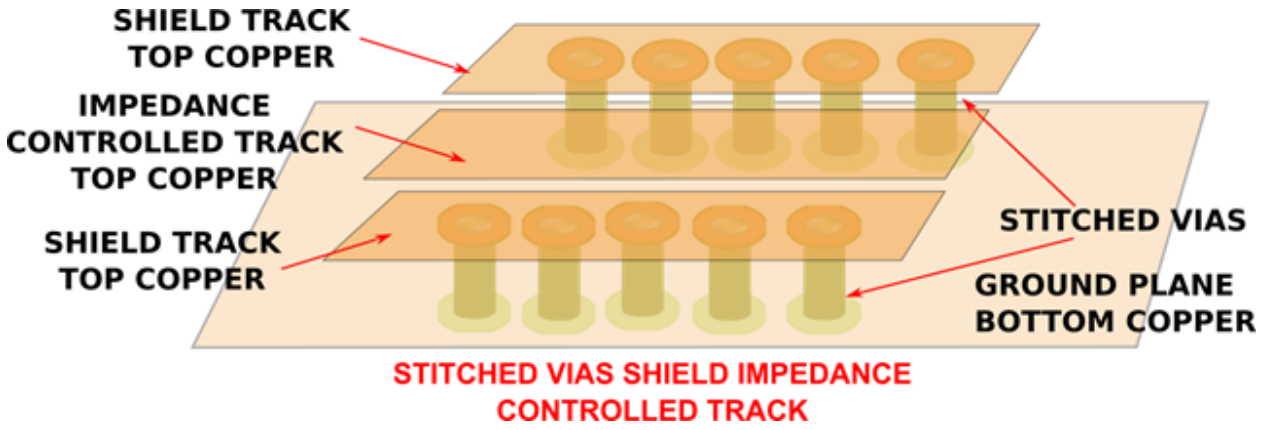
Ground Planes

- Place a dedicated ground plane immediately below each RF layer.
- This reduces electrical noise and interference through ground loops, and prevents crosstalk.
- Ground plane should be solid except sometimes under connectors or antennas.
- Separate planes for digital and analog.



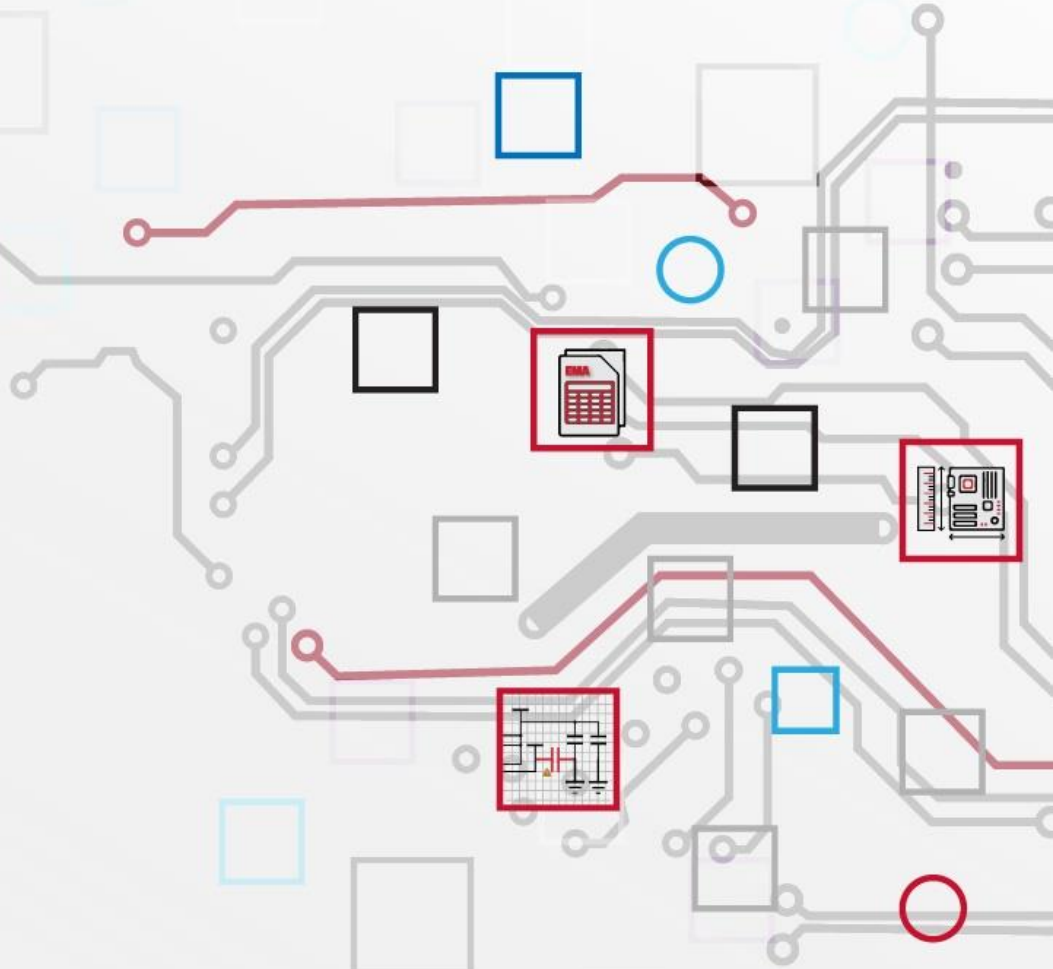
Stitching vias

- Implement ground plane via stitching wherever applicable.
- Via “fences” are important for coplanar designs



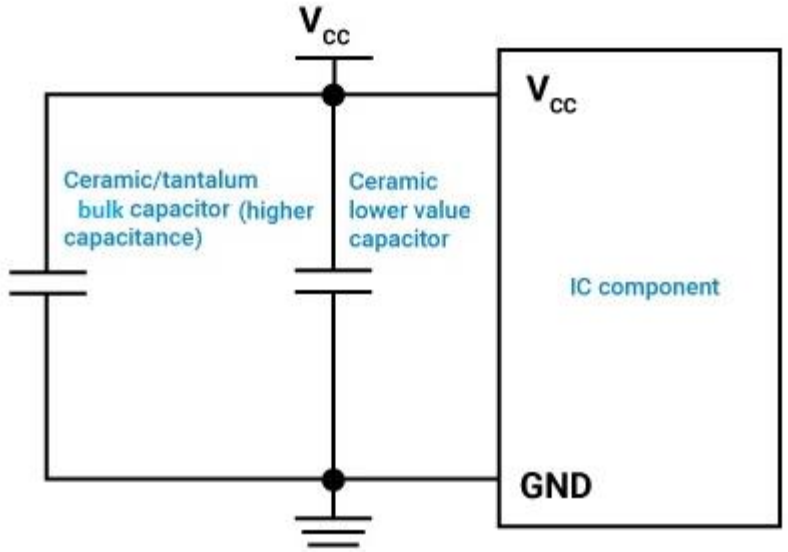
- Reduce routing of RF traces from one layer to another through vias.
- Use the maximum number of vias between the top layer ground plane and inner layer plane.
- These vias should be placed at a distance not exceeding 1/20th of the signal wavelength.

Demonstration



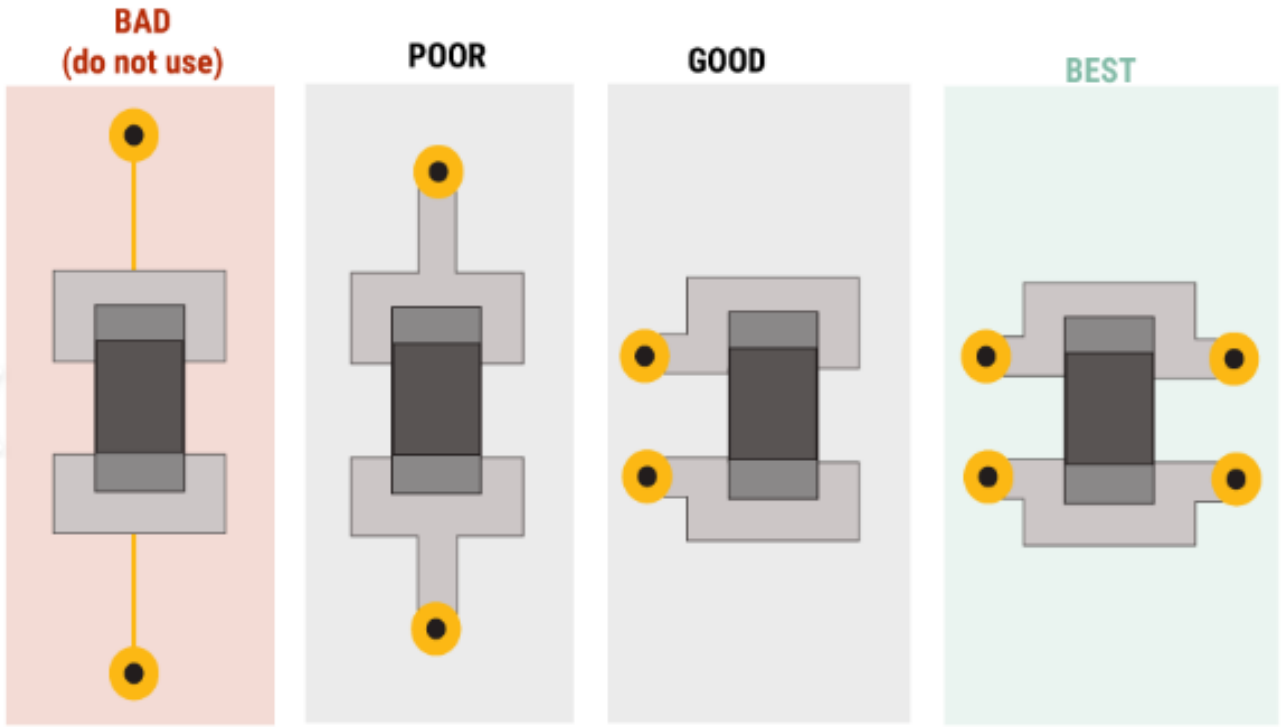
Power Supply Decoupling

- The higher capacitor is meant to filter the low-frequency noise in the system and store the energy.
- The high-frequency noise is filtered out by the lower capacitor.
- Operate the capacitors at the self-resonant frequency (SRF) to yield minimum impedance.
- Choose capacitors whose SRF is close to the noise frequency



Routing of Decoupling Capacitors

- Vias should be placed to minimize inductive return current ground loops
- Duplicate vias will reduce the inductance even further.



References

- 7 Factors that Impact RF PCB Design
  - http://protoexpress.com/blog/factors-impact-rf-pcb-design
- RF PCB Design – The Ultimate Guidelines
  - https://morepcb.com/rf-pcb-design
- 20 Factors that Impact RF PCB Design
  - https://artist-3d.com/rf-pcb-design

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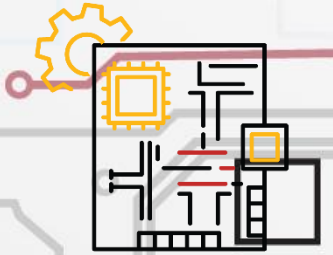

Knowledge base

Sierra Circuits PCB design services

- **Seamless interaction with manufacturing**
- **In-house stack-up design and material selection**
- **Component purchase for faster assembly**

Our areas of PCB design support and layout service and expertise include:

- High-speed (HDMI, DDR)
- HDI with blind and buried vias
- Fine pitch BGAs 0.4 mm and 0.5 mm
- RF, Bluetooth, Wi-Fi
- Flex and rigid-flex design
- Chip evaluation and chip characterization
- IPC class 2 and class 3/ES
- DFM/DFA layout validation included

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EMA Design Automation

Questions ?