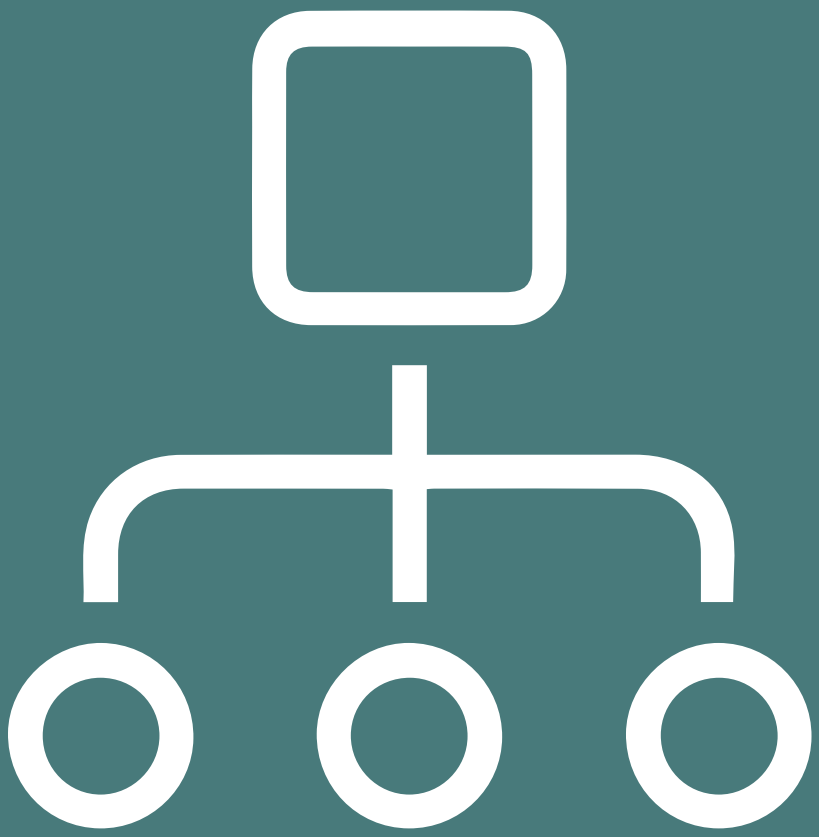
PDN
GIVES YOUR BOARD LIFE



EMA Design Automation®

POWER DELIVERY NETWORK

AN ESSENTIAL DESIGN CONSIDERATION

Ensuring a thorough power integrity analysis process is more important than ever in an engineer's PCB design flow.

Product trends continue to demand reduced form factor, while requiring even more power to support our always-on, always-connected lives. Design with confidence knowing your PDN is up to the task and keep your products humming smoothly with better PDN design practices.

From uncontrolled voltage ripples to EMI failure, we will discuss common issues engineers experience with their PDN, and how to fix them.

There are many nuances to the components necessary to create a PC board, and leveraging the impacts they make on the overall circuit design is a key part of the process. While it is one thing to know what a decoupling capacitor is, it is another to understand why one would use a certain kind over another. Having knowledge of how your circuit works is just as important as understanding the context in which it is used. Creating the perfect mixture of both will put you on the fast track to design success.

INDUSTRY TRENDS

KEEPING UP WITH THE JONESES

Industry design trends and product requirements are driving the need for early and comprehensive PDN analysis.

The biggest factor that places the most pressure on efficiency is the need to regularly handle high-speed signals. Operating frequency ranges are higher, creating faster signals and increasing the likeliness of power integrity issues.

Higher-speed signals result in increased PI concerns

Need to address decoupling at system level, not device by device

Important to catch issues early. Re-spins cost time and money.

Finding and fixing PDN problems at the end of the design process would be a large detriment to a carefully laid out, time-to-market schedule.

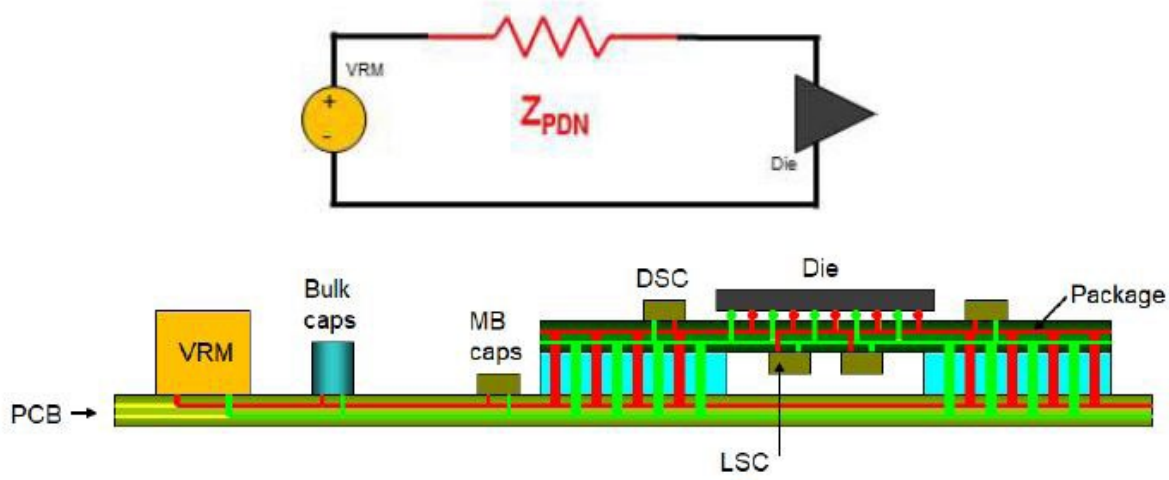
As such, it is imperative to catch any issues at the design stage, as early as possible in the project life cycle. Considering the board design at the systemic level will save untold amounts of time and money in reducing re-spins and shortening your projected launch date. Not to mention, your newfound knowledge will carry forward into future projects, propelling you into a much more comfortable space in the ever-changing industry trends. Ideally, this will keep you ahead of the curve and lead to business growth.

WHAT IS POWER INTEGRITY?

WITH GREAT POWER COMES GREAT RESPONSIBILITY

Every interconnect from a power supply on a board must reach its destination with as little interference as possible.

Power integrity is essential for a PCB design to function properly; you must be able to bring the appropriate and desired power to a load. With every addition or subtraction of a component, the overall impedance values will change. Analyzing whether the proper values and conditions are met will play a major role in the success or failure of a product.



The idea of power integrity can be illustrated through the Power Distribution Network (PDN).

This is the path the power takes to deliver it from the source to the loads. Within the path, there are several key requirements necessary, including maintaining a steady DC voltage at loads and creating minimal impedance between power and ground at the desired frequency range. It is a monumentally difficult task for a designer to create a PCB with thousands of interconnections that do not interfere with each other. The best products on the market have found the optimal performance values within their PC boards, ensuring a smooth-running device with longevity.

GOOD VS. BAD PDN

WHY DOES IT MATTER?

This chart gives a good idea of what results you are trying to achieve with good PDN, as well as the consequences of bad decisions in your project workflow.

There is nothing worse than getting a project months into its life cycle, only to find there are severe flaws or errors in the design upon release to manufacture. Therefore, it is important to set up proper constraints and test your PDN status as you work. Striving for the best results out of a power delivery network from the beginning will accelerate your entire design process and prevent costly rework down the line.

Good PDN	Bad PDN
Low voltage ripple	Uncontrolled voltage ripple
High frequency or no resonance	Huge impedance peaks due to power plane resonance
Reduced EMI	EMI failure
Lowest cost for acceptable performance	Unnecessary board costs due to “spray-n-pray” cap placement
On-time manufacturing	Re-spins
More board space with minimal caps & vias	Congested power planes/nets, causing power loss/impedance

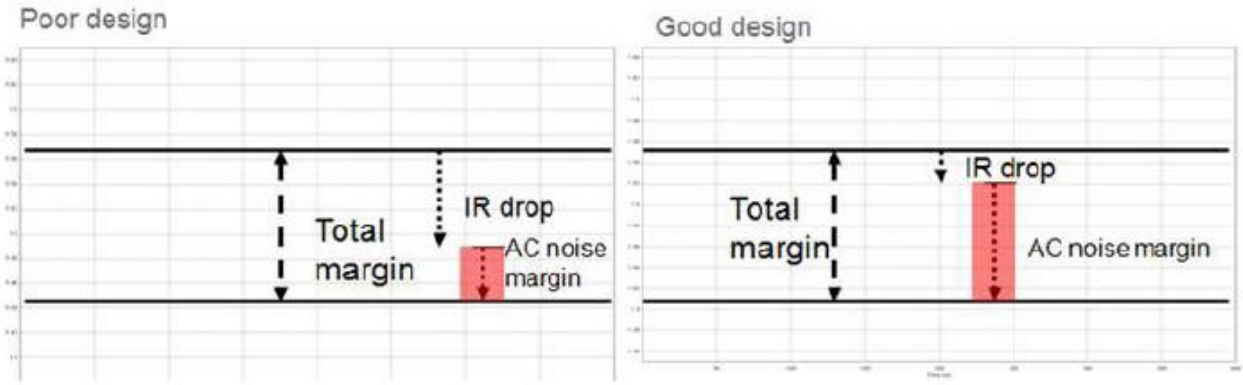
DC & AC POWER LOSS

FILLING IN THE BLANKS

Objectively, “power integrity” can be measured in the loss of power over a given distance.

The goal is to keep your power loss to a minimum, with the overall noise budget measuring within a specific tolerance. This budget is comprised of DC power (voltage losses before frequency), and AC noise within the frequency domain.

Often, AC noise is considered the primary power loss, while voltage drops are considered secondary. However, it may make more sense to figure out a lower DC loss first, as it will give you a greater AC noise margin to work with in your overall noise budget.



Here, we have included a poor design and a good design which take these factors into account.

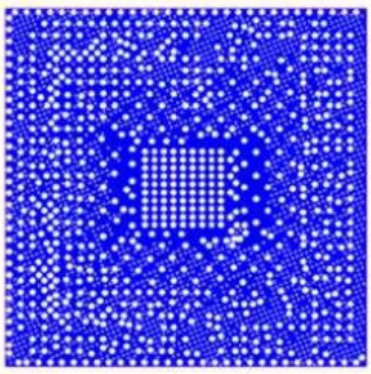
As you can see, the better design has the same total margin, but a much larger available AC noise margin by optimizing IR drop and DC loss. Working smarter in this way will ultimately save time later, as you will have a greater ability to make changes and compromises should the design require it. Let’s look at some ways to reduce DC loss in your design.

FURTHER INSIGHTS
ON DC ANALYSIS

Before we can understand issues within our frequency domain, let's focus on problems commonly found in DC Analysis.

Performing a DC PDN analysis can be useful in identifying voltage and current distribution issues. As boards get smaller and denser, there is a greater demand for a constant, stable voltage supply. There are less areas for power nets in smaller boards and too many antipads around vias can cause a "swiss cheese" effect on your board.

Neck-down



Swiss Cheese on solid plane

Dynamic trace routing can cut off the PDS

Additionally, dense board designs will require more complex shapes and pathways for current to travel.

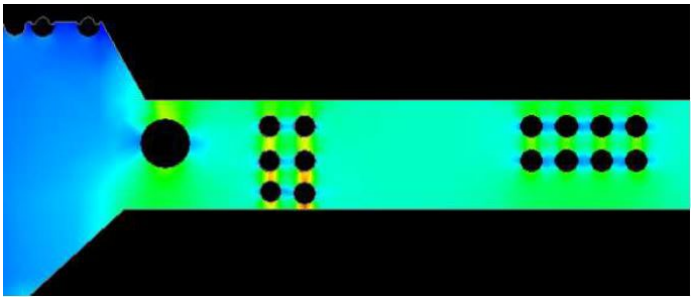
This leaves your board vulnerable to numerous errors which can unintentionally cut off the power delivery network. These are best identified as early in the design cycle as possible. Performing DC loss analysis as you design is an invaluable asset to saving time and costs associated with re-spins later in the product life cycle.

DC ANALYSIS ISSUES

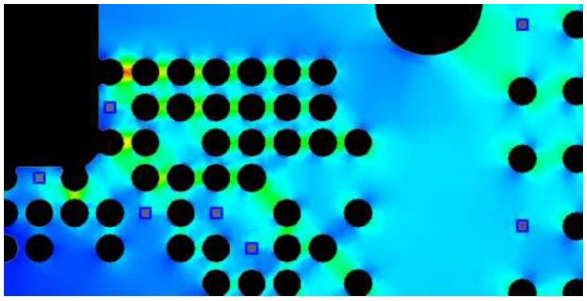
BOTTLENECKING & THE "SWISS CHEESE" EFFECT

Power plane paths can experience issues when vias create a *bottleneck.*

Bottlenecks occur when shapes are voided in such a way that the paths are funneled through a small area. The via patterns can overload the path through the shape, leaving little to no room for current to pass through. This issue may be remedied simply by rotating the via pattern 90 degrees, voiding the longer side of the shape rather than the shorter. The adjustment will open the bottleneck and allow current to flow seamlessly.



The vertical placement of the via pattern creates a bottleneck. Rotating the pattern opens the pathway for current to easily pass through.



Clustered clearance holes may cause a constricted current flow, and a 90-degree angle in a power plane shape may result in a current spike.

The *Swiss Cheese Effect* is most commonly found in BGAs, with a high density of clearance holes in a plane.

While sometimes unavoidable, with DC analysis we can identify if this occurrence is the source of an issue. Identified by a constriction of the current flowing through the area, you can avoid this effect by making sure any antipads around vias do not overlap. More variables to try are leaving unused pins without a via or reducing the number of capacitors used. Additionally, avoiding sharp corners or right angles on power plane shapes will negate current spikes, and using 45-degree corner angles is preferable.

FREQUENCY RESPONSE

AC IS MORE COMPLICATED

Understanding the frequency domain takes several layers of knowledge.

First, know that *decoupling capacitors* are the primary tool to reduce AC switching noise, and selecting the proper scheme of decaps is not simple. Critical questions to consider are what kind, how many, and where to place them, as all will affect your frequency response.

Oftentimes, too many decaps are added onto the board, which increases BOM (bill of materials) costs and takes up board space. Adding more decaps will also introduce more impedance at a higher frequency due to the inductive and capacitative behaviors of the decap. Analyzing the design for where decoupling capacitors are most needed and optimizing their placement will aid in these issues.

On a higher level, how can we measure if a board will achieve the desired low voltage ripple? There is an equation to define your target impedance, which is the impedance at which the ripple created by the dynamic current of the specific consumer is within the specified range. The allowed ripple is typically around 5%, and the current refers to the total allowable current switching at the same time.

$$Z_{target} = \frac{(Power\ Supply\ Voltage) \times (Ripple\ Voltage)}{Dynamic\ Current}$$

Using this method, we can achieve what is called *flat PDN impedance.* This means that, for every point on the board across the frequency range, our PDN impedance is lower than the target impedance. In this equation, *x* and *y* are points on the board, while *f* represents the frequency.

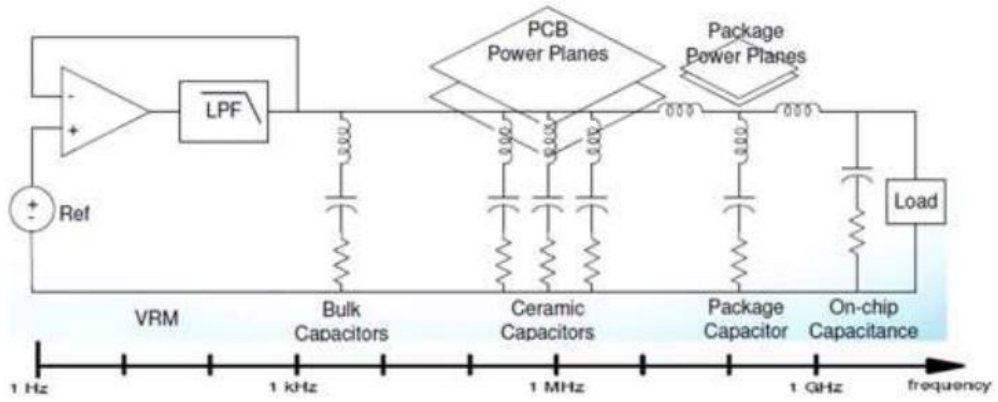
$$Z_{PDN}(x, y, f) = \frac{Node\ Voltage}{Total\ Injected\ Current}$$

It is important to note, while your IC datasheet specifications may not fit the exact equation, you can often come up with the necessary variables by assuming the dynamic current is half of the worst-case current. In this way, we can calculate backwards and use the relation of the worst-case current to the worst-case power to find the target impedance.

FUNDAMENTAL CONCEPTS
FOR FREQUENCY RESPONSE

Now that we've calculated our goal, how exactly are we able to control the impedance in the frequency domain?

Within your ideal model, you will have a target impedance you must keep below. Each component you add to your board will either raise or lower your impedance and it is a delicate balancing act to combine them in the optimal way. In addition, we must introduce *L, R,* and *C* as your virtual equation values. Here, *L* represents the *inductance*, which must be kept low for minimizing the drop and AC impedance. *C* represents *capacitance* and must be high to store charge and lower AC impedance. Lastly, *R* represents *resistance*, which must be low to minimize DC loss. Note that *L* and *C* are inversely related for impedance.



Once we understand the relation of the components, the circuit layout can begin to take shape.

As you design, lay out your components in order of increasing frequency to see what other components (besides the decoupling capacitors) may affect the impedance on AC noise. These will include VRMs (voltage regulator modules), planes, and in-package or on-chip capacitors.

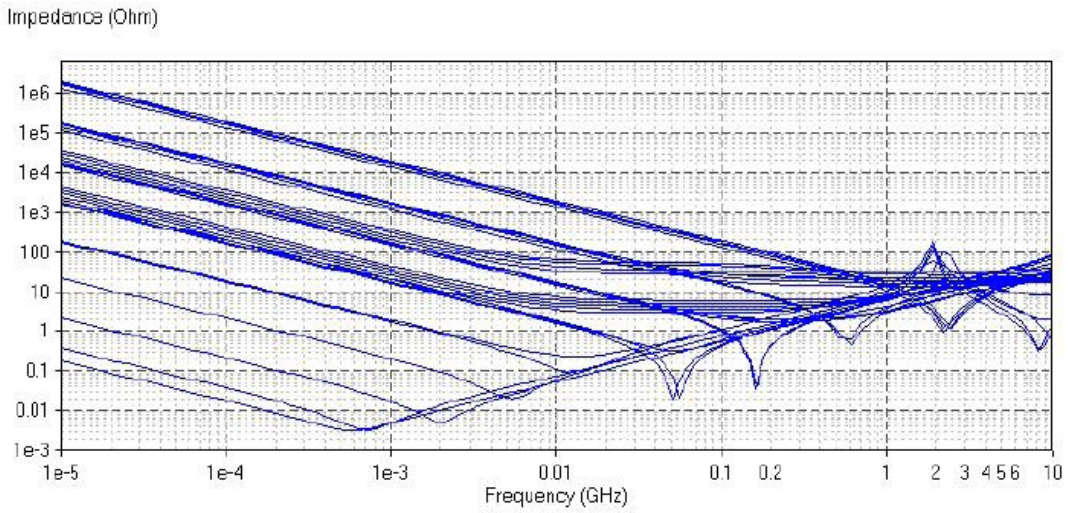
In particular, the VRM is responsible for maintaining a low impedance at the low end of the frequency spectrum. As such, it is a critical starting point for power integrity before choosing the decoupling capacitors.

DECOUPLING CAPACITORS

WHY ARE THEY SO IMPORTANT AGAIN?

In design, decaps are the primary tool used to reduce AC switching noise.

Decaps are capacitors used to decouple one part of a circuit from another. They also supply current and support the voltage needed until the VRM can respond. The way they work is to demonstrate parasitic resistance and inductance, behaving as a resistor, inductor, and capacitor in series. This graph shows a variety of decaps which can cover a wide range of frequencies.



Note that each decap has a specific effective range, with an optimal "sweet spot" to lower impedance.

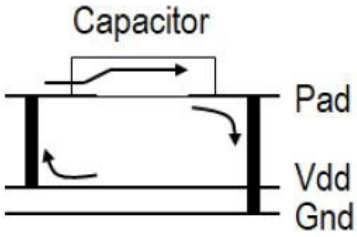
The lowest impedance points are at the south end of the frequency of the decap, illustrating what we call *equivalent series resistance* (ESR), otherwise known as self-resonance. The broad range of frequencies you see here is why it is important to choose the correct decap: the wrong one may not have the lowest impedance for your board, and as a result, is not fully optimizing its potential. When selecting decaps, you must first find which frequency range to work within, and then pick the appropriate decaps to coincide.

CURRENT LOOPS,
POWER PLANES, AND INDUCTANCE...OH MY.

The amount and placement of decaps becomes more important when taking current loops into account.

These loops are formed due to the capacitor height from the pad that creates a "loop" inductance which ultimately increases impedance at higher frequencies. The measure of inductance depends on the capacitor style and how it connects to the power plane. Ideally, we want to keep the inductance as low as possible, which can be achieved by carefully placing our vias in relation to our capacitors. Minimizing the via-to-pad distance, shortening the fan-out, and reducing cap height will all aid in this goal.

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$



The last common issue in PDN comes in the relationship of decaps to power planes.

On a board, power planes can show resonances in frequency response due to parasitic capacitances and inductances. This degrades the power plane and can be destructive to a signal by sending out harmful amounts of common-mode electromagnetic interference (EMI). To resolve this issue, decoupling capacitors are used to push resonances of power planes to very high frequencies beyond our operating range, effectively rendering them moot.

A SUMMARY

POWER DELIVERY IS THE CORE DRIVING SOURCE OF A BOARD

When it comes to PDN, there is a total noise budget to work within.

This budget must cover voltage drops and AC noise, and both pose challenges in providing stable power from source to load. While we have illustrated these issues in detail and given tips on how to best avoid them, it is no mean feat to accomplish everything smoothly. A typical PCB design includes hundreds— if not thousands— of components, layers, and relationships between them all. It can take weeks or months of round robin communication to resolve every PI issue at hand.

But what if we could catch and analyze problems right on the board in the design phase? If there was a way to visualize our voltage and current density plots on the board, wouldn't that save so much time? Furthermore, what if you could compare decap schemes with varying numbers, types, and placement options without having to spend hours digging through the internet searching for answers?

Improve Productivity

Reduce Costs

Prevent Field Failures

Employing solid PDN design principles has become a key driver in design success. Our Cadence® Sigrity™ Power Integrity tools allows users to predict AC noise issues, DC voltage drops, correct impedance issues, and run multi-board electrical and thermal co-simulations. Having a design-driven PDN approach can save you time, prevent errors, and keep your designs running smoothly. Ensure a solid PDN built to deliver power efficiency at the lowest possible cost with Allegro Sigrity™ today.

Want more information? Contact us at info@ema-eda.com for inquiries.

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