ENGINEER'S GUIDE TO PCIe

HOW TO ACHIEVE PCIe COMPLIANCE UPFRONT

PCI EXPRESS®

PCIe 4 | PCIe 5 | PCIe 6

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ENGINEER'S GUIDE TO PCIe COMPLIANCE

HOW TO ACHIEVE PCIe COMPLIANCE UPFRONT

In today's computers, multiple PCIe slots are typically present to provide vital connectivity with foundational components. Additionally, they allow users to add peripherals, enhancing the computer's capabilities and improving performance beyond the initial factory specifications. Adherence to PCIe compliance is mandatory for these products to ensure seamless integration with the motherboard.

This eBook aims to explore the requirements of PCIe compliance and simulation tools that can assist you in verifying whether your design will achieve PCIe compliance before moving forward with manufacturing. By doing so, you can save valuable time, avoid unnecessary costs, and optimize the return on investment (ROI) of your development process.

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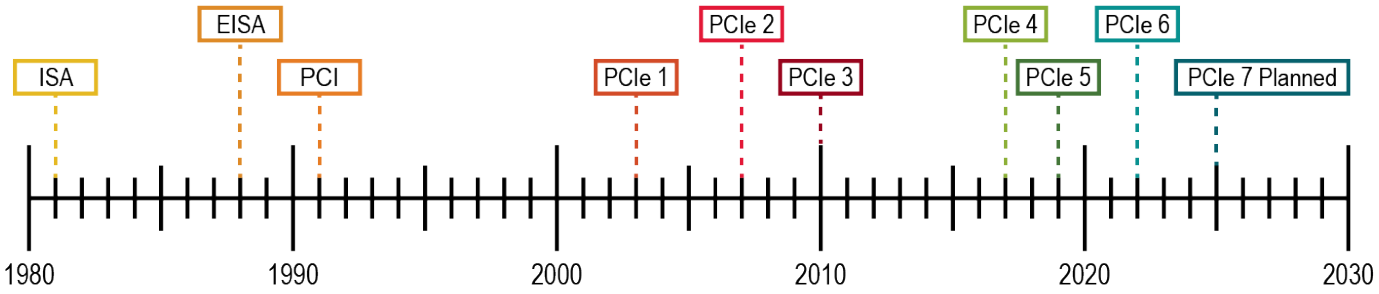
HISTORY OF PCIe

When you glimpse inside a computer, you'll notice that everything connects to the motherboard. This includes components such as the power supply, hard drives, USB ports, RAM memory modules, and various peripheral devices, whether located inside or outside the computer case. Many of these peripherals connect to the motherboard through expansion slots.

Computer expansion slots made their debut in the early 1970s, with IBM introducing the PC Bus technology or Industry Standard Architecture (ISA) in 1981. This was followed by the development of Extended Industry Standard Architecture (EISA), a 32-bit version of the bus protocol, which was used until 2000. The PC/104 standard for embedded computers was also based on ISA, but it was eventually replaced by PCI in 1991.

PCIe Development Timeline



While some computers still feature PCI slots today, most manufacturers have embraced the newer PCIe serial bus standard. Peripheral Component Interconnect Express (PCIe) slots are among the most commonly found components inside a computer. These slots, which extend from the motherboard, are crucial to the computer's overall functionality. They serve as connection points for various essential devices, including:

- Central Processing Units (CPUs)
- Memory Modules, like DDR4 and DDR5
- Graphics cards
- Network Interface Cards (NICs)
- Sound Cards
- Wi-Fi Cards
- USB Expansion Cards
- Other Peripherals

PCIe enables the components and peripherals to communicate with the computer through data transfer channels.

OVERVIEW OF PCIe

PCIe EVOLUTION

Introduced by Peripheral Component Interconnect Special Interest Group or PCI-SIG in 2003, PCIe has gained widespread adoption. Since its introduction, PCIe has undergone several revisions each with significant technological advancements:

PCIe COMPLIANCE STANDARD SPECIFICATIONS								
REVISIONS	ENCODING (DATA-TO-SYMBOL)	TRANSFER RATE (GT/S)	THROUGHPUT (GB/S)					YEAR OF RELEASE
			x1	x2	x4	x8	x16	
PCIe 1.0	8b/10b	2.5	0.250	0.500	1.000	2.000	4.000	2003
PCIe 2.0		5.0	0.500	1.000	2.000	4.000	8.000	2007
PCIe 3.0	128b/130b	8.0	0.985	1.969	3.938	7.877	15.754	2010
PCIe 4.0		16.0	1.969	3.938	7.877	15.754	31.508	2017
PCIe 5.0		32.0	3.938	7.877	15.754	31.508	63.015	2019
PCIe 6.0	242b/256b	64.0	7.563	15.125	30.250	60.500	121.000	2022

*Transfer rates are endcoded per lane parameters and throughput values are the unencoded bandwidth.

Each PCIe evolution has approximately doubled the transfer rate and throughput for x1, x2, x4, x8, and x16 PCIe data transfer. The jump from PCIe 4 to PCIe 5 is significant because the increased bandwidth promotes the development of more compact computing systems. The PCIe 6 evolution has pushed the performance envelope to heights that were unimaginable when PCIe was first introduced. Manufacturers are now actively designing and building products to leverage the remarkable capabilities of PCIe 6 including:

- 64 GT/s transfer rate
- Wider lane bandwidths
- Improved encoding

With each iteration of PCIe (and a new revision, PCIe 7.0, already under development and planned to release in 2025), it's imperative to first understand the differing requirements to guarantee PCIe performance. To address this, PCI-SIG, an electronics industry membership organization, publishes standards that promote the use of the PCI protocol.

PCIe COMPLIANCE TESTING

PCI-SIG SPECIFICATIONS

PCIe standards are intended to provide sufficient information, guidance, and performance metrics to build devices that reliably transfer data across peripheral component interconnects and adhere to PCIe compliance specifications. For PCIe revisions, standards may include:

- Interconnect Attributes
- Physical and Signal Architecture
- Protocols
- Electrical and Software Requirements
- Testing Directives

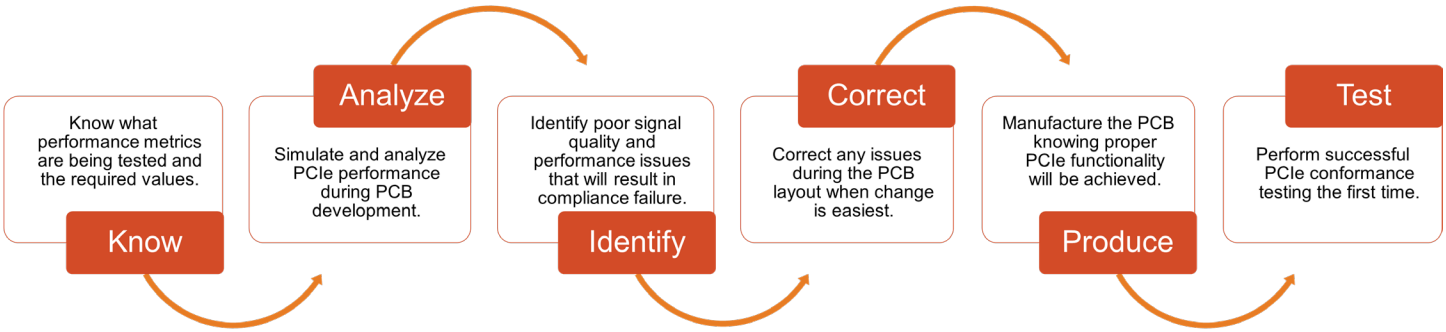
Additionally, PCI-SIG standards are written to ensure backward compatibility with previous PCIe versions. The following table outlines the available PCIe specifications:

PCIe 4 SPECIFICATION (REVISION 4.0)	FOCUS
PCI Express® Base Specification	Describes interface, architecture, and interconnect attributes.
PCI Express Architecture Link Layer and Transaction Layer Test Specification	Testing requirements for ports and devices.
PCI Express Architecture PHY Test Specification Versions: 1.0, 1.01 (Clean), 1.01A (Change Bar), 1.2	System board and add-in card electrical testing.
PCIe 5 SPECIFICATION (REVISION 5.0)	**FOCUS**
PCI Express® Base Specification	Describes attributes, programming interface, architecture, & fabric management.
PCI Express Card Electromechanical Specification	Electrical and mechanical server and desktop specifications evolution.
PCI Express Architecture Link Layer and Transaction Layer Test Specification	Testing specifications for transaction and link layers.
PCI Express Architecture Configuration Space Test Specification	Testing specifications for all devices and Root Complex Register Blocks (RCRBs).
PCI Express Architecture PHY Test Specification	Descriptions of electrical tests.
PCI Express M.2® Specification	Specification for smaller form factor mobile adapters.
PCIe 6 SPECIFICATION (REVISION 6.0)	**FOCUS**
PCI Express® Base Specification	Describes the architecture, programming, electrical and mechanical protocols.
PCI Express Base Specification (Change Bar Versions)	Includes comparison notes for PCI 5 vs PCI 6 and between PCI 6 versions 0.9 and 1.0.

Neglecting to ensure PCIe performance complies with industry standards would significantly restrict marketability and potential usage of your new design. These specifications should be referenced to determine the performance metrics required to ensure reliable and accurate data transmission with PCIe devices.

PCIe COMPLIANCE TESTING
REQUIREMENTS

PCIe operation must be analyzed through conformance testing before product release, where rigorous testing is performed to compare the PCIe performance and reliability with the PCI-SIG defined specifications. PCIe conformance testing is costly and failure to comply with PCIe standards often results in post-fabrication design modifications or complete redesigns. To keep your project on budget and minimize design respins, it's important to incorporate PCIe compliance analysis throughout the PCB design process:



To ensure first-pass PCIe compliance success and adherence to the defined standards, electrical performance and interconnect attributes should be analyzed during the PCB layout. Regardless of the PCIe version (4, 5 or 6), the following performance metrics must be evaluated:

- Eye Height
- Eye Width at Zero Crossing
- Differential Insertion Loss
- Differential Return Loss
- Stressed/Swept Jitter

Additional performance metrics are required based on the PCIe device version:

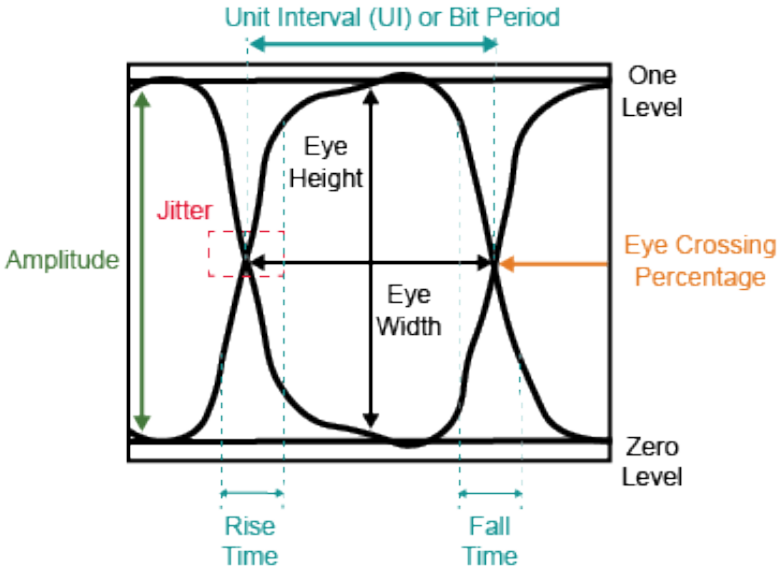
PCIe 4	PCIe 5	PCIe 6
Peak EH Offset	Peak EH Offset	Lane-to-Lane Skew
Range for DFE d1 Coefficient	Eye Mask	Intra-Pair Skew
Range for DFE d2 Coefficient	Lane-to-Lane Skew	
Eye Mask	Intra-Pair Skew	

While the types of measurements are similar for PCIe devices, the acceptable values vary based on the defined PCIe standard.

PCI-SIG hosts Compliance Workshops. Similar to a USB Plugfest, these events allow developers to check PCIe compliance and interoperability with known working devices. Products must score 80 or above for interoperability and pass all tests for compliance including electrical testing, configuration testing, link protocol testing, and transaction protocol testing.

PCIe COMPLIANCE TESTING
CHANNEL TOLERANCING

Eye metrics and eye diagrams are excellent tools for visually inspecting signal integrity parameters as they provide a graphical perspective that aids in quickly identifying potential problems. Eye diagrams display a long sequence of data bits by chopping the stream into 2 Unit Intervals (UI) and overlaying each one on top of each other.



Eye diagrams offer a more convenient and meaningful way to analyze large amounts of data which can be used to obtain essential channel and signal information. The following eye characteristics should be measured using the eye diagram and evaluated to ensure PCIe compliance:

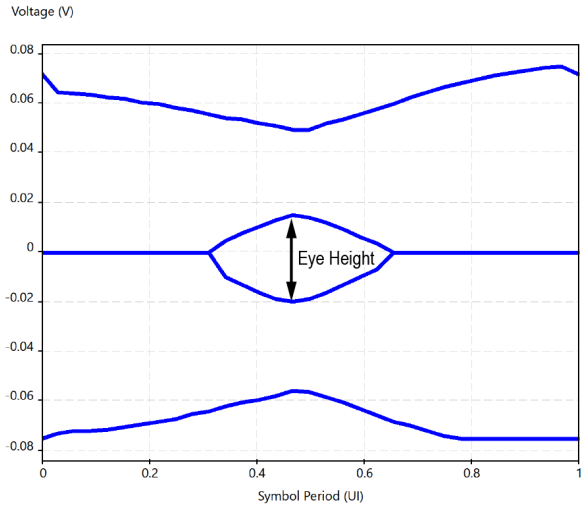
- Eye Height
- Eye Width
- Eye Mask
- Peak EH Offset from UI Center
- Range of DFE d1 and d2 Coefficients
- Lane-to-Lane Skew
- Intra-Pair Skew

Determining how to measure these key performance metrics and the appropriate values is key to PCIe compliance success.

PCIe COMPLIANCE TESTING
EYE HEIGHT

EYE HEIGHT

The eye height measures the vertical opening of the eye or the maximum difference between the innermost 0 bit and 1 bit voltage representations during PCIe signal transmission.



WHY IS IT IMPORTANT?

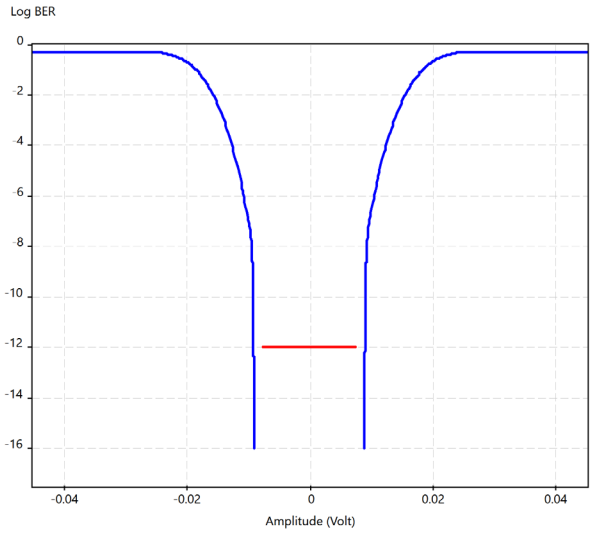
Analyzing the eye height provides a good indication of signal quality during PCIe transmission. Poor signal quality can result in:

- Unreliable Data Identification
- Data Loss
- Erroneous System Behavior
- Product Shut Down

Jitter, noise, and signal attenuation directly affect eye height.

HOW DO YOU MEASURE IT?

When analyzing the eye diagram at the BER of interest (1e-12 for PCIe 4 or 5 and 1e-6 for PCIe 6), the eye height value can be obtained by measuring the maximum distance between the innermost '1' bit representation and the inner most '0' bit representation. This measurement should be taken in the +/-10% vicinity of the center of the bit interval or unit interval.



Eye height is often analyzed by graphing the Log BER values against the amplitude in Volts. This generates a bathtub curve and allows you to easily assess the eye height.

WHAT IS AN ACCEPTABLE VALUE?

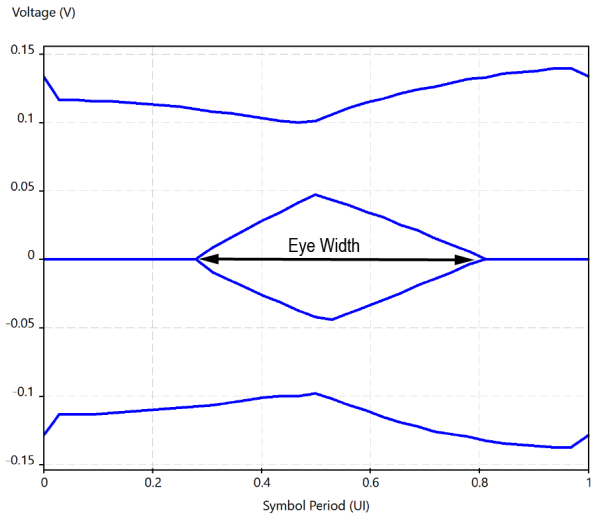
Acceptable values for eye height vary based on the PCIe device:

PCIe 4 and **PCIe 5**: Greater than 15mV
PCIe 6: Greater than 6mV

PCIe COMPLIANCE TESTING
EYE WIDTH AT ZERO CROSSING

EYE WIDTH AT ZERO CROSSING

Eye width measures the horizontal opening of the eye and provides the offset between the unit interval and where the signal peaks.

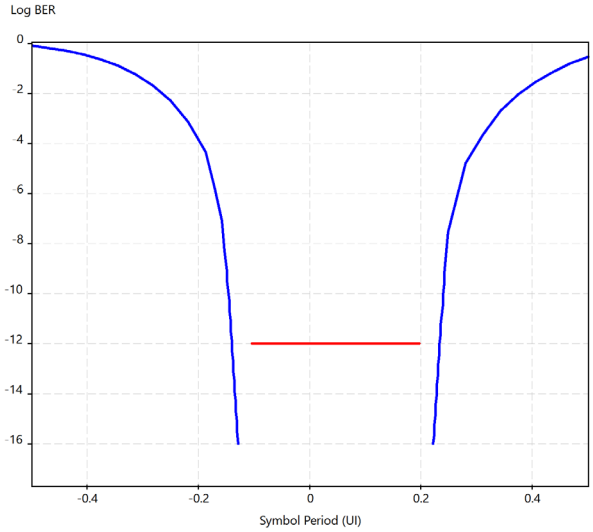


WHY IS IT IMPORTANT?

Eye width provides an indication of the quality of timing for signal transmission. If the eye width is too small, it can indicate that your signal is out of phase or there is too much timing jitter. This can lead to inaccurate differentiation between sequential signals.

HOW DO YOU MEASURE IT?

When analyzing the eye diagram, identify the time at which the signals cross zero and measure the distance between instances.



Eye width is often analyzed by graphing the Log BER values against the symbol period (UI). This generates a bathtub curve and allows you to easily assess the eye width.

WHAT IS AN ACCEPTABLE VALUE?

Acceptable values for eye width vary based on the PCIe device:

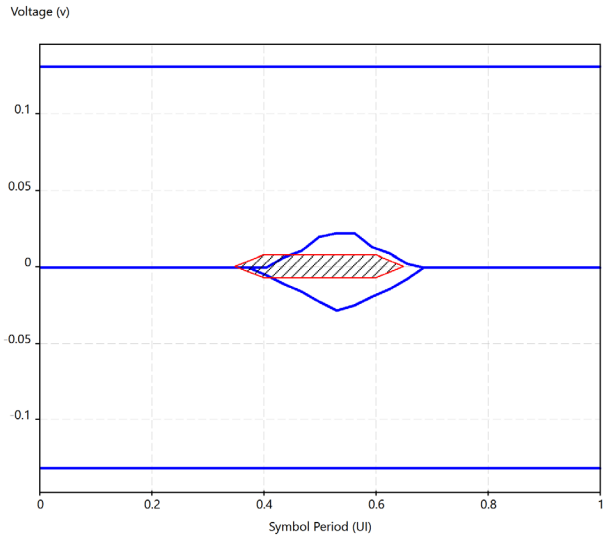
PCIe 4 and **PCIe 5**: Greater than 0.3UI

PCIe 6: Greater than 0.1UI

PCIe COMPLIANCE TESTING
EYE MASK

EYE MASK

The eye mask graphically identifies the boundaries for signal voltages and timing data within the eye diagram.



WHY IS IT IMPORTANT?

The eye mask analyzes conformance to the required specifications through quick visual inspection. Confirming that the eye mask fits fully within the eye of the signal will ensure an error-free data transmission.

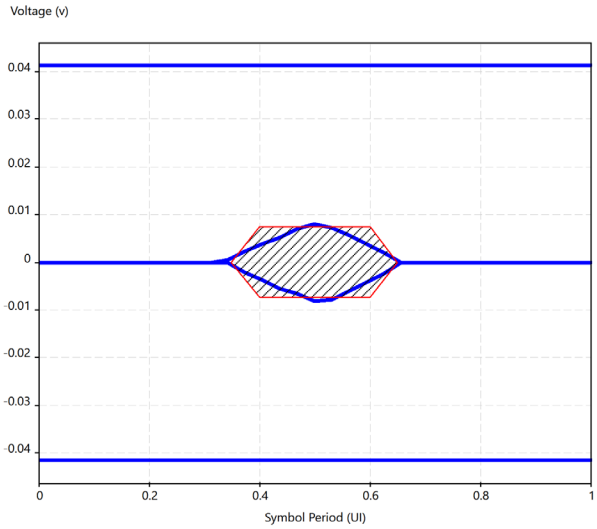
HOW DO YOU MEASURE IT?

Create a template by plotting the values for the specified eye mask within the eye. To achieve the required functionality and performance, the eye mask must fit fully within the constraints of the eye.

It is important to identify and correct potential issues during the PCB design as correcting eye mask issues can be difficult or impossible once the board is built. To correct eye mask issues, avoid all situations that may result in stubs and thoroughly analyze signal timing.

WHAT IS AN ACCEPTABLE VALUE?

For **PCIe 4** and **PCIe 5** a hexagonal mask should fit within the constraints of the signal eye. A compliance failure will occur if any part of the eye mask is outside of the signal eye, as shown below.



PCIe standards should be referenced for the required mask values; however, typical mask values are as follows:

SYMBOL PERIOD (UI)	VOLTS (mV)
0.35	0
0.4	7.5
0.4	-7.5
0.6	7.5
0.6	-7.5
0.65	0

PCIe COMPLIANCE TESTING
PEAK EH OFFSET FROM UI CENTER

PEAK EH OFFSET FROM UI CENTER

The peak EH Offset from UI center is the time between the maximum eye height and middle of the Unit Interval (UI).

WHY IS IT IMPORTANT?

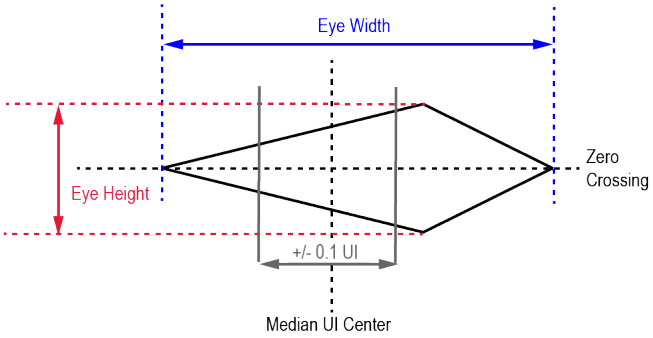
The Peak EH offset from UI center allows you to analyze the amount of distortion due to:

- Unequal attenuation characteristics of the channel
- Noise Characteristics
- Jitter Characteristics

Too much offset can result in phase and timing issues as it minimizes the time available for the receiver to respond between bits.

HOW DO YOU MEASURE IT?

Identify the time in which the eye height peaks, often referred to as $T_{RX\text{-}DS\text{-}OFFSET}$.



Measure the distance between this time and the center of the unit interval.

WHAT IS AN ACCEPTABLE VALUE?

Ideally the eye height should peak at the center of the unit interval; however, it is common for the peak to be offset due to physical limits of the channel.

For **PCIe 4** and **PCIe 5**, the acceptable offset is +/-0.1UI.

PCIe COMPLIANCE TESTING
RANGE FOR DFE COEFFICIENTS

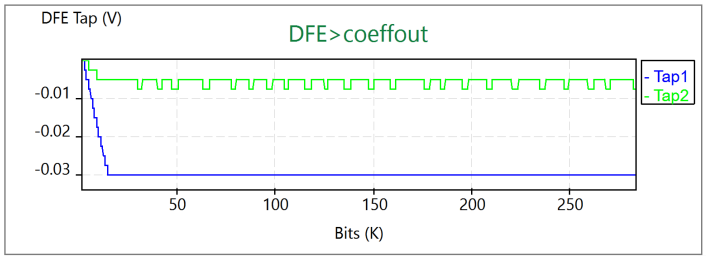
Equalization filtering of both the transmitter and receiver data streams is employed to compensate for hardware channel deficiencies and help achieve performance requirements. For PCIe compliance, the receiver equalization process is known as Decision Feedback Equalization (DFE) and is used to reduce the effects of intersymbol interference (ISI). DFE provides a high frequency boost which compensates for dispersive, frequency-dependent, channel loss and removes scaled interference from four previous bits based on the channel impulse response. This is achieved with a feedforward filter and a feedback filter which attempt to estimate the channel response and cancel out ISI respectively:

Feedforward Filter	Feedback Filter
Uses decisions made by the receiver to update the coefficients of the filter. (Decision-Directed Approach)	Uses the error signals obtained from the decision-directed approach to update the filter coefficients.

To ensure PCIe compliance, a range of values is provided for these DFE coefficients.

RANGE FOR DFE COEFFICIENTS

DFE coefficient values control how much attenuation is applied and at what frequency. The range for DFE coefficients ensures equalization can be achieved and successful.



WHY IS IT IMPORTANT?

Equalization filter performance is limited. Assessing the signal quality of the PCIe channel design without equalization will determine if the amount of equalization required falls within the available range for DFE coefficients. This will provide the best chance at compliance when DFE is incorporated.

HOW DO YOU MEASURE IT?

A range of DFE coefficients are provided for both the feedforward filter and feedback filter.

For the feedforward filter, the DFE coefficient is defined as $V_{RX\text{-}DFE\text{-}D1\text{-}COEFF}$ or Tap 1. For the feedback filter, the DFE coefficient is defined as $V_{RX\text{-}DFE\text{-}D2\text{-}COEFF}$ or Tap 2. Both coefficients should be measured and monitored throughout the PCIe operation.

WHAT IS AN ACCEPTABLE VALUE?

The acceptable range for d1 and d2 coefficients for **PCIe 4** are outlined below:

DFE d1 coefficient: +/- 30mV
DFE d2 coefficient: +/- 20mV

PCIe COMPLIANCE TESTING
SKEW

For PCIe 5 and 6, it is critical to analyze skew as faster transfer rates reduce the allowable timing margin for accurate data transfer. Both lane-to-lane skew and intra-pair skew should be analyzed to ensure adequate timing and performance.

LANE-TO-LANE SKEW

Lane-to-lane skew is the variation in timing for signals on adjacent lanes.

WHY IS IT IMPORTANT?

Lane-to-Lane skew is critical to ensure data is received in the proper order. If lane-to-lane skew is too large, the data can be misinterpreted.

HOW DO YOU MEASURE IT?

Analyze the difference in arrival time at the receiver for PCIe lanes. To do this, measure the delay present between the transmitter and receiver of each lane and compare the delays between the lanes to determine the skew.

WHAT IS AN ACCEPTABLE VALUE?

Lane-to-lane skew should be evaluated for both **PCIe 5** and **PCIe 6**. For both device versions, lane-to-lane skew should be less than 5ns.

INTRA-PAIR SKEW

The intra-pair skew is the difference in arrival time between the positive (P) and negative (N) sides of the differential pair signal transmission.

WHY IS IT IMPORTANT?

Synchronization within differential pairs is critical. Depending on the amount of variation, data transmission may degrade to levels that make identifying signal strength impossible. High levels of skew can also increase susceptibility to EMI and crosstalk.

HOW DO YOU MEASURE IT?

Intra-pair skew is determined by correlating the eye opening and the common-mode noise (CMN) of the lane.

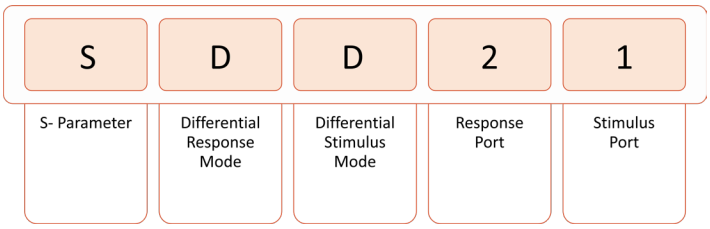
WHAT IS AN ACCEPTABLE VALUE?

The intra-pair skew for differential pairs must be evaluated for both PCIe 5 and PCIe 6. During analysis, this parameter is customizable based on the design. For proper functionality, skew should be below 10% of the Unit Interval. For **PCIe 5** and **PCIe 6**, generally the skew should be less than 10ps.

PCIe COMPLIANCE TESTING
DIFFERENTIAL INSERTION LOSS

DIFFERENTIAL INSERTION LOSS

Differential Insertion Loss is the amount of attenuation or loss the signal will experience as it travels along a channel, in this case a differential pair net. This is also known as SDD_{21} which represents the following:



S: S-Parameter
D: Differential Response Mode (Differential receiver)
D: Differential Stimulus Mode (Differential transmitter)
2: Response Port (Port 2 or the output of receiver)
1: Stimulus Port (Port 1 or the input of transmitter)

WHY IS IT IMPORTANT?

Every data channel will result in some degree of loss due to signal attenuation; however, if the loss is too high it can lead to incorrect interpretation and unrecognizable signals at the receiver.

HOW DO YOU MEASURE IT?

Differential insertion loss is calculated by dividing the input signal at the receiver by the output signal at the transmitter. Simulate and analyze the ratio of energy at the receiving end of the channel (S-parameter port '2') to the energy introduced to the channel at the transmitter end (S-parameter port '1') over the desired frequency range.

WHAT IS AN ACCEPTABLE VALUE?

For differential signal transmission, 0.1dB/in per GHz can be expected. The acceptable value depends on the cable length and frequency in the design and can be calculated by:

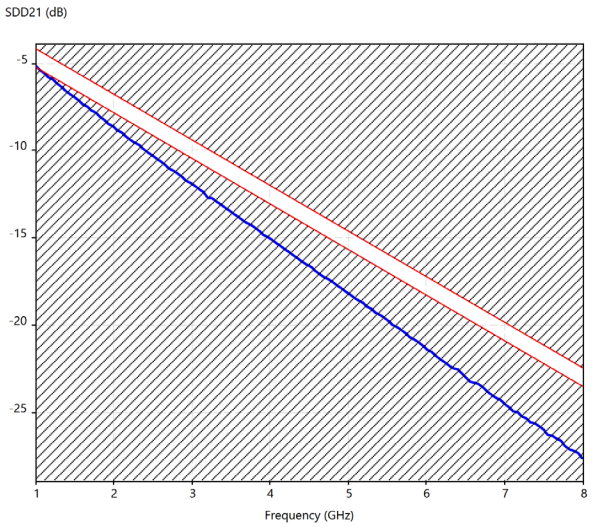
0.1dB x cable length (inches) x Frequency (GHz)

A mask can be created to visually compare the SDD_{21} measurement against the PCIe standard values. Below are examples of typical insertion loss mask parameters for PCIe devices.

For **PCIe 4**, the insertion loss should be the following bounds:

FREQUENCY	SDD_{21}
1 GHz	-4.2 dB
8 GHz	-22.5 dB

FREQUENCY	SDD_{21}
1 GHz	-5.2 dB
8 GHz	-23.5 dB



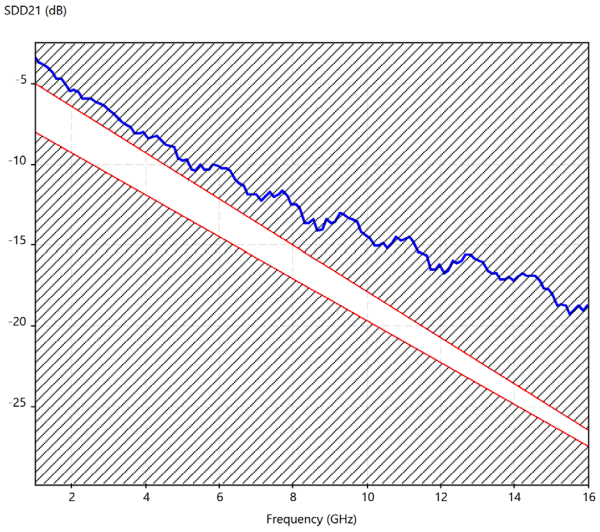
PCIe COMPLIANCE TESTING

DIFFERENTIAL INSERTION LOSS

For **PCIe 5**, the insertion loss should be the following bounds:

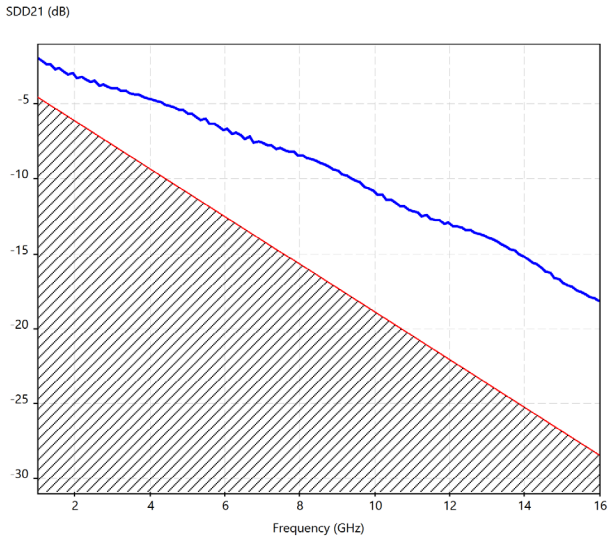
FREQUENCY	SDD_{21}
1 GHz	-5 dB
16 GHz	-26.5 dB

FREQUENCY	SDD_{21}
1 GHz	-8 dB
16 GHz	-27.5 dB



For **PCIe 6**, the insertion loss should be the following bounds:

FREQUENCY	SDD_{21}
1 GHz	-4.6 dB
16 GHz	-28.5 dB



If design characteristics for SDD_{21} are above the compliance range, achieving a working design will be easier than if characteristics are below the compliance range. Insertion loss can be improved by:

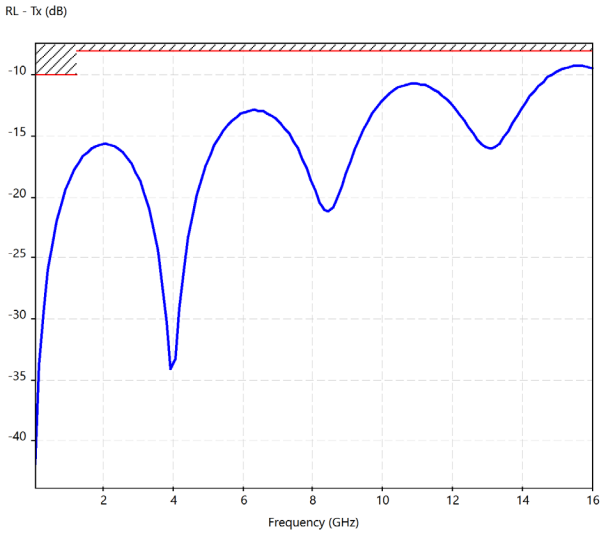
- Shortening transmission paths
- Lowering the impedance along traces
- Ensuring identical spacing along the paths

PCIe COMPLIANCE TESTING
DIFFERENTIAL RETURN LOSS

Differential return loss or differential reflection measures how much energy is reflected in the source of a signal by the receiver. For PCIe devices, return loss measurements should be analyzed at both the TX and RX ports.

TX AND RX RETURN LOSS

Analyzing the differential return loss at both the receiver and the transmitter allows you to evaluate if the port is accepting enough of the signal without reflecting too much back.



The receiver return loss is referred to as the output differential return loss or SDD_{22}. The transmitter return loss is referred to as the input differential return loss or SDD_{11}.

WHY IS IT IMPORTANT?

Any returning energy or reflected energy will interfere with the signal information being transferred. If too much energy is reflected back, it will be difficult to identify or differentiate between 0s and 1s which can result in:

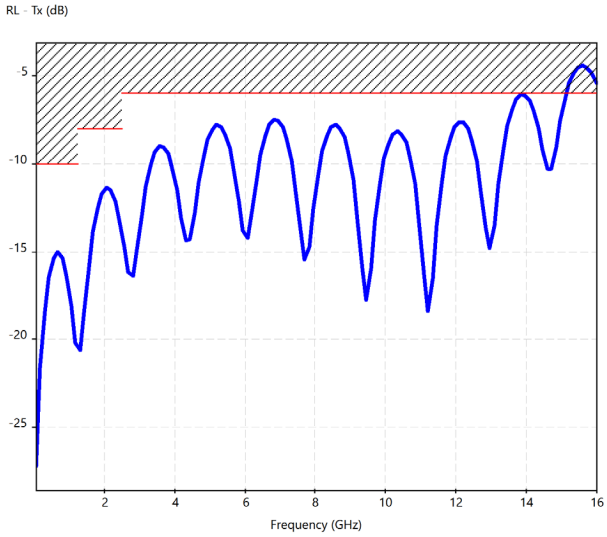
- Degraded Signal Quality
- Distortion
- Unrecognizable Signals

HOW DO YOU MEASURE IT?

The S-Parameter amplitude should be analyzed at the corresponding port over the required frequency range for both TX and RX return loss.

WHAT IS AN ACCEPTABLE VALUE?

Ideally, the differential return loss would be zero; however, no system is ideal. Reference the corresponding PCIe standard to determine the maximum return loss values.



Plotting these values will create a template to visually identify the keepout area for the TX and RX return loss. A compliance failure will occur if the SDD_{22} or SDD_{11} measurement enters the keepout area, as shown above.

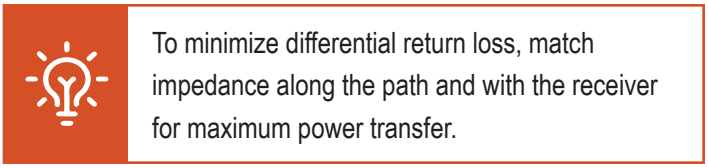
PCIe COMPLIANCE TESTING

DIFFERENTIAL RETURN LOSS

The following can be used as a guideline for both TX and RX Return loss masks:

For **PCIe 4**, the return loss should be the following bounds:

FREQUENCY	SDD_{11} OR SDD_{22}
50 MHz to 1.25 GHz	-10 dB
1.25 GHz to 2.5 GHz	-8 dB
2.5 GHz to 8 GHz	-6 dB



To minimize differential return loss, match impedance along the path and with the receiver for maximum power transfer.

For **PCIe 5**, the return loss should be the following bounds:

FREQUENCY	SDD_{11} OR SDD_{22}
50 MHz to 1.25 GHz	-10 dB
1.25 GHz to 2.5 GHz	-8 dB
2.5 GHz to 16 GHz	-6 dB

For **PCIe 6**, the return loss should be the following bounds:

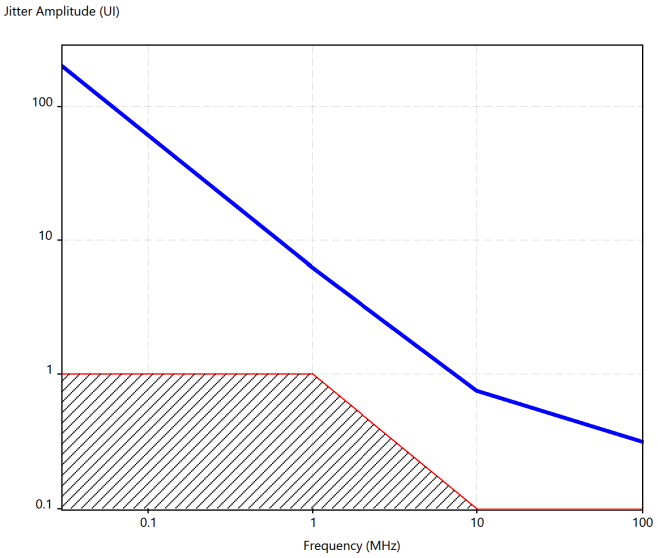
FREQUENCY	SDD_{11} OR SDD_{22}
50 MHz to 1.25 GHz	-10 dB
1.25 GHz to 16 GHz	-8 dB

PCIe COMPLIANCE TESTING
STRESSED/SWEPT JITTER

For jitter compliance testing of the PCIe device, the eye diagram must be analyzed at the Bit Error Rate (BER) of interest. The BER is the number of bits received in error at the receiver compared to the total number of bits received. For PCIe 4 and PCIe 5, the BER of interest is 10^{-12}. For PCIe 6, the BER of interest is 10^{-6}.

STRESSED/SWEPT JITTER

A stressed/swept jitter test shows the amount of jitter over a frequency sweep for the channel. The worst-case (stressed) eye diagram should be analyzed to determine the maximum jitter amplitude which produces a discernible eye at the desired BER for every frequency point.



WHY IS IT IMPORTANT?

Analyzing the Stressed/Sweep Jitter determines how much jitter margin is acceptable to accurately receive the signal at various frequencies. This evaluates the level of resilience against flawed transmissions for your PCIe device.

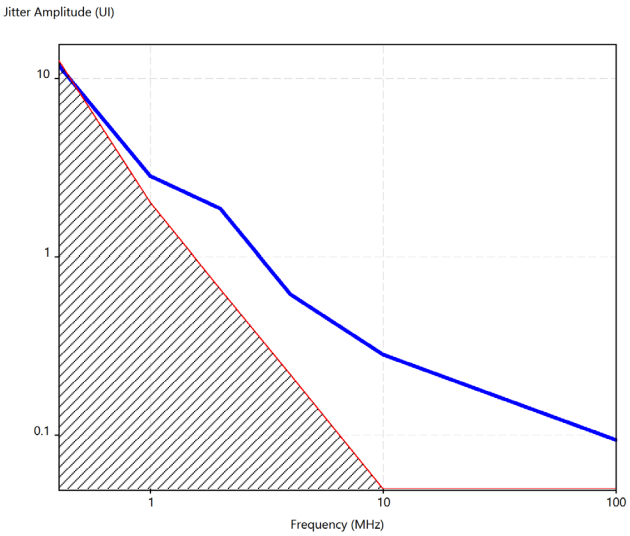
HOW DO YOU MEASURE IT?

To analyze Stressed/Swept Jitter, a plot should be created detailing the maximum jitter amplitude allowed to still have a discernible eye at the desired BER for every frequency point.

WHAT IS AN ACCEPTABLE VALUE?

The jitter tolerance should be compared to the values outlined in the corresponding PCIe standard. Jitter tolerance values (UI) are provided over a range of frequencies and should be plotted against the device characteristics for efficient evaluation.

Plotting these values will create a jitter mask in which the measured results can be visually compared to ensure compliance. A compliance failure will occur if the jitter measurement crosses the defined mask region, as shown below.



The following can be used as a guide to ensure the jitter amplitude is higher than the specified sinusoidal jitter values as dictated by PCIe compliance standards.

PCIe COMPLIANCE TESTING

STRESSED/SWEPT JITTER

For **PCIe 4**, the following parameters can be used to create the jitter mask:

FREQUENCY	JITTER AMPLITUDE
0.3 MHz	1 UI
1 MHz	1 UI
10 MHz	0.1 UI
100 MHz	0.1 UI

For **PCIe 5**, the following parameters can be used to create the jitter mask:

FREQUENCY	JITTER AMPLITUDE
0.4 MHz	15.765 UI
1 MHz	3 UI
20 MHz	0.1 UI
100 MHz	0.1 UI

For **PCIe 6**, the following parameters can be used to create the jitter mask:

FREQUENCY	JITTER AMPLITUDE
0.4 MHz	12.46 UI
1 MHz	2 UI
2 MHz	0.658 UI
4 MHz	0.217 UI
10 MHz	0.05 UI
100 MHz	0.05 UI

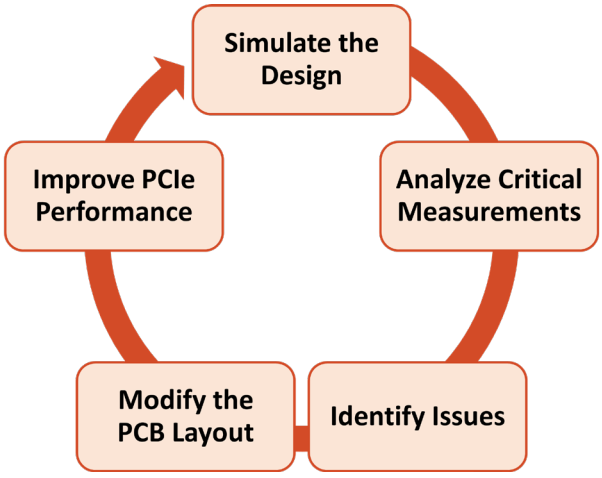
To improve jitter, the best solution is to shorten the channel length; otherwise, the configuration of the device may need to be adjusted.

PCI-SIG stipulates that all compliance testing must pass for a device or port to be labeled and recognized as PCIe compliant. Failure of any of the above parameters must be corrected to achieve this status, which may necessitate redesign, respins, and additional time and costs.

SIGN-OFF WITH CONFIDENCE

KNOW BEFORE YOUR BUILD

Conformance testing is required for products with PCIe devices before product release; however, due to the time and cost associated with each PCIe conformance test, it's critical to achieve first-pass success to keep the project on time and on budget. This can be achieved by analyzing PCIe performance metrics during the PCB layout.



PCIe performance issues or design choices that may result in compliance failures can be identified and corrected before manufacturing a design and performing compliance testing. This minimizes the need for design respins, ad-hoc design modifications, and additional compliance testing. Manual methods for analyzing PCIe performance metrics can be time-consuming and tedious consisting of:

- Researching PCIe specifications
- Determining and graphing the necessary performance metrics
- Calculating the required measurements
- Comparing the results against the corresponding PCIe standard values

Simulation and analysis of PCIe compliance can be accelerated with:

- Integrated PCIe Specification Values
- Automatic Measurements
- Color-Coded Pass/Fail Results
- Automated Report Generation

Employing a simulation software solution which incorporates these features and efficiently analyzes PCIe compliance during the PCB layout will streamline post-production conformance testing and help reach your time-to-market goals.

TIPS TO ACHIEVING PCIe COMPLIANCE

To improve PCIe performance and fix compliance failures, the following guidelines should be followed:

Accurate Modeling

Accurate modeling is essential in simulating realistic PCIe design behavior and performance. Designs containing PCIe must perform in no-ideal environments so crosstalk must also be incorporated for real-world performance.

Incorporating AMI Models

Algorithmic Modeling Interface (AMI) models incorporate the necessary internal component and connectivity information to perform statistical simulation based on the channel pulse response or time-domain simulation. This allows you to include equalization and other non-LTI (linear and time-invariant) effects into the analysis.

Avoid Stubs

Remove stubs from vias in the design with backdrilling to improve performance.

Reroute Traces

Optimize traces in the design by keeping traces short, verifying the differential pair trace configuration, and being cautious of noisy signals.

Adjust the Design

If performance metrics cannot be achieved with the current design configuration, it may be necessary to incorporate alternative components or realign performance objectives.

VERIFYING PCIe COMPLIANCE
WITH SIGRITY

Successfully adhering to performance requirements and optimizing the applicability of your product is best achieved by utilizing tools that enable you to perform compliance testing on your design during PCB layout. Sigrity can be used to analyze compliance and optimize the signal integrity, power integrity, and overall performance of your PCB design. This powerful analysis tool also includes compliance kits that allow you to test signal quality across various data transfer interfaces for compliance with industry standards. For PCIe compliance, targeted testing regimens are available for PCIe 3, 4, 5, and 6.

Sigrity provides kits specifically developed to help achieve PCIe compliance by:

- Performing all essential tests for PCIe compliance
- Automatically analyzing simulation results against PCI-SIG specified values
- Providing easy to read pass/fail results
- Automatically generating reports
- Providing seamless integration with other software design and analysis tools

To learn more go to:

ABOUT EMA DESIGN AUTOMATION

EMA Design Automation is a leading provider of the resources that engineers rely on to accelerate innovation. We provide solutions that include PCB design and analysis packages, custom integration software, and engineering expertise, which enable you to create more efficiently. For more information on achieving compliance for other technologies including MIPI, USB, and DDR, view our other e-books and whitepapers.