DFT for In-Circuit Test

When Should Testing Be Considered

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EMA Design Automation®

DFT for In-CIrcuit Test: When Should Testing Be Considered

The success of the manufacturing process is based upon the execution and measurement of the health of each process step. The machines on assembly lines install thousands of parts every minute; therefore, throughout the assembly process, checks must be completed. DFT allows capability for testing which includes component connectivity, electrical value, and proper component orientation. However, final testing—in-circuit testing capability—must be designed into the PCB at the layout stage.

Test points can be used by the test engineers to verify the continuity and performance for every connection on the PCBA. This capability is a very powerful tool when looking for manufacturing defects on an assembly. While many tests can be run without required modifications to the PCB layout, In-Circuit Testing (ICT) does require some additional features added to the PCB.

Types of Testing
AXI Post Wave Inspection
AXI Solder Joint Inspection
In-Circuit Testing
AOI Post Wave Inspection
AOI Component Measurement
AOI Solder Joint Inspection
AOI Solder Paste
Functional Test

Should I Include DFT for ICT?

An engineering team must be in touch with several attributes of the PCB before deciding to add DFT for ICT. If the team can mark all the following "DFT required" checkboxes when making their analysis, the expense up-front might be considered an investment. Some of the basic reasons to justify DFT for ICT are:

- Provides probe access to nets on the PCBA which would not be accessible otherwise for testing and analyzing signal performance.
- In production volumes, tracking and measurement of the PCB processes is the key to profitability.
- ICT can detect shorts, opens, lifted leads, and missing parts.
- ICT can detect dead parts, wrong parts, and bad parts.
- ICT can check for inverted polarity and even missing, socketed parts.

Considering materials and time, PCBs which have ridden the conveyor far into the assembly process are worth quite a bit of money if they have been assembled without defect. Checking for defects like those listed above with automated, in-circuit testing at the completion of the assembly process confirm the quality of the assembly and therefore confirm its value. However, the value of a PCBA with even one defect is zero.

Catching and tracking defects during individual assembly processes helps AMEs to see if there are any defects which are occurring consistently to any one part. For instance, if the same part is failing consistently on a run of PCBs, manufacturing engineers will perform a root cause analysis on the condition.

Incorporating DFT for ICT into a PCB layout can take time and add cost up front. Many ask the question "Why do I have to pay for a test fixture whose only purpose is to check the quality of the EMS supplier? Isn't quality their responsibility to check?" Yes, quality always falls in the lap of the EMS provider, whether building a limited run of 100 PCB assemblies or 100,000. However, the true answer to the question is a matter of cost. Measuring quality on a run of 100 PCB assemblies will most likely be accomplished manually. If it takes 30 minutes to test the PCB manually, the cost for testing the run would be calculated at 50 hours at a rate of say, $100 per hour for a total cost of $5000—far less expensive than investing in a test fixture and implementing DFT for ICT. However, to apply a manual test strategy to 100,000 would

take 50,000 technician hours, costing five-million dollars. To apply manual testing to such a large run of assemblies would lead to a doomed schedule and financial ruin. This exaggerated example is the reason one might opt to pay for automation. DFT for ICT reduces testing time to seconds and therefore saves overall cost even after investing in test equipment.

Test Points

Test points are etched target shapes which include short routes making electrical connection to the circuit nets of the PCBA. They are typically round, .035 [0.89] or larger and are cleared of any solder resist or legend ink which would impede electrical connectivity when coming into contact with a test probe. Test points can be added to the schematic and even include reference designation if required. In many cases, if testability is called for at the beginning of a layout project, the EE will work to address the requirements into the layout at the time of placement, prior to routing.

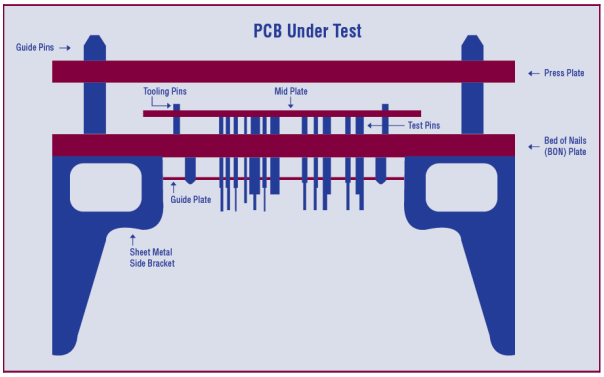
Test Point Spacing

Spacing the test points sufficiently is paramount to good DFT. Test point spacing of .100 [2.54] is considered good by the test engineering stakeholders because such spacing allows for least expensive test probes and ideal ease of access. However, real world design density will not always allow for such robust spacing. In this case, reducing spacing by .025 [0.64] -- .100, .075, .050 -- grid spacing is considered acceptable though the smaller spacing will yield a higher cost fixture.

Test Strategy and Requirements

AA test point strategy is usually determined at the time of parts placement. It's important for it to be clearly developed to identify goals, cost, quality, and scheduling. Be clear regarding which nets will need to be accessed, whether this is through a note or adding test points to the schematic.

The general requirements for adding test points to a PCB layout are simple: test points are ideally added to the non-component side of a PCB. However, if the side selected for test points includes components, avoid placement near parts taller than .200 [5.08mm]. Common test point shape and size is circular, with an ideal diameter of .040 [1.00]. This diameter ensures the spring-loaded test point probes will be placed accurately enough to raise the probability of contact to the test pads to 100% per 1000 hits. If there is limited space on the layout, test point size may be reduced slightly to .035 [0.89]; however, reducing the diameter beyond that will increase the probability of a probe miss significantly. Generally, adding a single test point per net on the PCBA design, if possible, makes the test engineering stakeholders happy. Also, it helps if many extra test points can be added to ground and power across the PCB for ease of access.



When implementing DFT for ICT, once the PCB is manufactured and a test fixture is built, any future changes to the PCB should not disturb previously placed test points—it is recommended they be locked down in the design. While it is easy to move a test point on a layout, it is very difficult and expensive to re-tool a test fixture to match the change.

The Surface Mount Technology Association (SMTA) has published TP-101E Testability Guidelines. This comprehensive guide is a great go-to which should be read by all project

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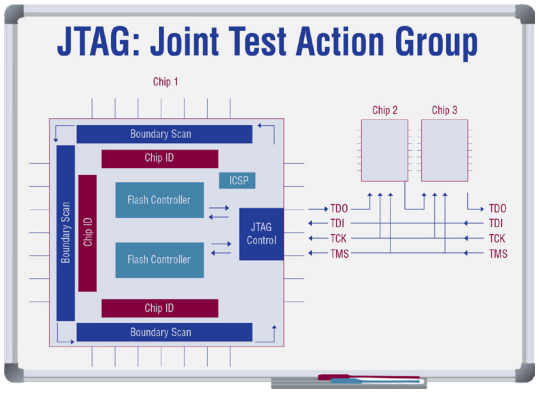
stakeholders to better understand our test engineering counterparts. This guide should interest PCB designers because the publication lists several general guidelines for creating test equipment for the board you've designed. In addition, the guide describes 32 probing-fixture guidelines which the test engineer must adhere to.

JTAG

With high density requirements on PCB's continuing to rise, having enough real estate to add test points for 100% testability on a PCBA is a rarity. Implementing partial test point coverage can make some test engineers cringe and ask, "if you're not fully testing, why test at all?" Missing test points on a PCBA with no physical space remaining is a weak compromise. However, there is another option in this circumstance brought to us by the good folks at JTAG, Joint Action Test Group.



JTAG was formed by a group of companies in the 1980s to define some extra silicon which would be added to the workhorse chips on your board. This extra silicon would then allow devices to be put into a 'test mode' giving you control of the pins on the device. It is very similar to another common test protocol, 'Boundary Scan,' both of which are governed by IEEE 1149.1-6. The JTAG test spec defines which signals need to be accessed. A PCB design engineer needs to be aware there is a minimum of four-wires. The signals used are:

- TCK (Test Clock) – this signal synchronizes the internal state machine operations.
- TMS (Test Mode Select) – this signal is sampled at the rising edge of TCK to determine the next state.
- TDI (Test Data In) – this signal represents the data shifted into the device's test or programming logic. It is sampled at the rising edge of TCK when the internal state machine is in the correct state.
- TDO (Test Data Out) – this signal represents the data shifted out of the device's test or programming logic and is valid on the falling edge of TCK when the internal state machine is in the correct state.

There is an optional signal which can be added: TRST (Test Reset), which when available, can reset the TAP controller's state machine.

Conclusion

When is the best time for considering DFT? Simply put, test engineers are important stakeholders in any PCB design project which will be going to volume. As circuit performance requirements are being defined, questions about how performance will be tested and verified do not naturally come to mind for other project stakeholders. Test engineers must be provided schematics and brought to the table at the beginning of a project to address whether testing is required, what equipment will be used, and provide estimates for initial cost.

Once the decision is made that testing will be required on the PCB, DFT can be implemented during the layout phase of the PCB. The design database can be set up to audit each net for testability. The software should be able to export a DFT report showing all net names with respective test point XY locations which can be of great use to the test engineer when creating a fixture. This design for test practice ensures the best chance for all testing requirements to be successfully included into the design.