ACHIEVING MIPI COMPLIANCE

GETTING IT RIGHT THE FIRST TIME

EMA Design Automation®

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Mobile devices such as cellular phones, tablets, and other smart electronic products have become critical to meet the functionality and capability requirements for commercial, industrial, and other critical industry applications. Achieving MIPI compliance is the global standard that ensures these devices meet the high operational and reliability objectives warranted.

This eBook discusses important aspects of the MIPI standards as well as how to create and verify that your circuit board design adheres to MIPI guidelines. This includes software solutions to simulate and analyze your board for M-PHY and C-PHY compliance before manufacturing. This can save you valuable innovation time and help optimize your development to maximize ROI by eliminating unnecessary and excessive costs.

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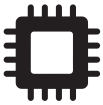
EMA Design Automation®

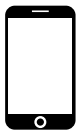
OVERVIEW OF MIPI

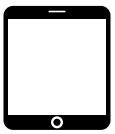
From individuals to businesses to governments, everyone uses or relies on mobile communications. Mobile Industry Processor Interface or MIPI is used in these applications for accurate and secure data exchange over mobile channels. MIPI devices are used in a variety of applications based on the device configuration including:


CAMERAS

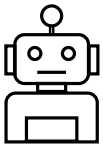

SENSORS


CHIP-TO-CHIP


SMARTPHONES


TABLETS


DRONES


ROBOTS


IOT DEVICES

To achieve the high-performance and reliable communication required for applications in transportation, aerospace, military, and more, the MIPI Alliance develops interface specifications for mobile devices, system hardware, and software integration and interoperability. The goal of these specifications is to help mobile product developers innovate easily, faster, and more efficiently for the following areas:

MIPI INTERFACE SPECIFICATION AREAS	
HARDWARE	**SOFTWARE**
Audio	Debug and Trace
Cameras and Imaging	Software Integration
Display	Software Code
Control Data	Security
Chip-to-Chip	
Physical Layers	

For mobile device hardware, physical layer (PHY) specifications are one of the most important. And for these internal communication channels, the MIPI alliance develops specific protocols, interface standards, and compliance requirements based on the type of device.

OVERVIEW OF MIPI

MIPI PHYSICAL LAYER SPECIFICATIONS

Due to the functionality and performance differences between MIPI devices, the MIPI Alliance defines PHY specification standards for the following devices:

PHY SPECIFICATION	DESCRIPTION	FEATURES	USES	CONFORMANCE TESTS
A-PHY	Serializer/Deserializer (SerDes) specification for advanced automotive technology and other applications.	32 Gbps data rate Point-to-point or daisy chain topologies Automotive Electromagnetic Compatibility (EMC) affects immunity	Autonomous Driving System (ADS) Advanced Driver Assist System (ADAS) Human Machine Interface (HMI) In-Vehicle Infotainment (IVI) IoT Industrial	N/A
A-PHY Protocol Adaptation Layers (PALS)	Allows for connecting higher layer protocols using MIPI A-PHY.	Transmission and reception over long reach A-PHY SerDes interfaces	ADS ADAS IVI	N/A
C-PHY	Encoded camera and display data transfer.	Low Electromagnetic Interference (EMI) Low power High-performance	Smartphone Displays Smartphone Cameras Tablets Surveillance Cameras Automotive Sensors IVI IoT Robots Drones	Yes
D-PHY	Differential signaling protocol specifications for 4 meter or less interconnection.	Low EMI Low power High-performance	Smartphone Cameras Smartphone Displays Automotive Cameras Dashboard Displays Radar Sensors Large Tablets Robots Drones	Yes
M-PHY	Multimedia and Inter-Processor Communication (IPC) communication interface specifications.	Low EMI Low power High Bandwidth	RF interface Universal Flash Storage (UFS) memory Processor-to-Processor Communication	Yes

The number of mobile data communications product developers that adopt and adhere to the MIPI PHY specifications above spans the globe and continues to grow. To create a successful MIPI product, it is increasingly imperative to consider how to achieve MIPI compliance during the PCB layout.

MIPI COMPLIANCE
PRODUCT DEVELOPMENT

All MIPI devices are point-to-point connections; however, each type of MIPI device differs in functionality and performance to fit specific design applications. For PCB design, two common devices MIPI incorporates are MIPI M-PHY and MIPI C-PHY.

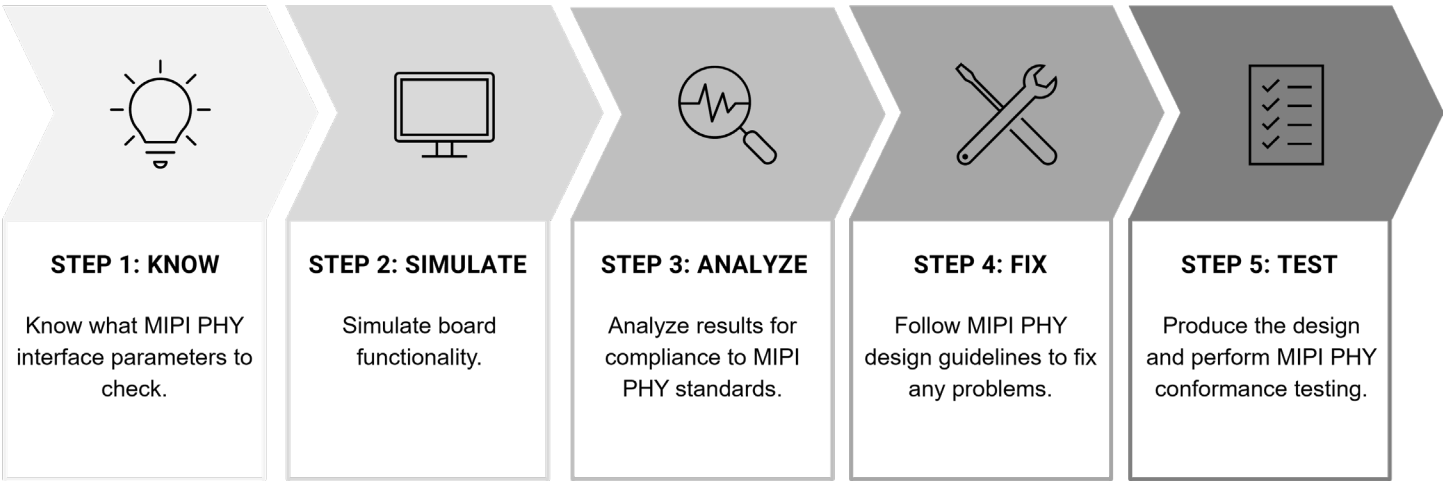
MIPI M-PHY

MIPI M-PHY devices are high-speed serial links, transmitted with differential signaling. MIPI M-PHY devices consists of lanes, which can be either transmitter or receiver. Lanes are independent units with individual configurations and data interfaces.

MIPI C-PHY

MIPI C-PHY uses three wire groups to achieve higher throughput in a rate-limited channel application. The three wires (A, B, C) comprise a lane. For MIPI C-PHY devices, high-speed signaling is differential for terminated data signals.

When building MIPI compliant devices, circuit boards, and systems, analyzing adherence to device standards must be incorporated into your PCB design process. Regardless of which MIPI device is being utilized in the design, steps can be taken to achieve MIPI compliance the first time:



STEP 1: KNOW

Know what MIPI PHY interface parameters to check.

STEP 2: SIMULATE

Simulate board functionality.

STEP 3: ANALYZE

Analyze results for compliance to MIPI PHY standards.

STEP 4: FIX

Follow MIPI PHY design guidelines to fix any problems.

STEP 5: TEST

Produce the design and perform MIPI PHY conformance testing.

If a product fails initial conformance testing, it often results in additional costs and time added to the scope of the project due to:

- Post-production design modifications
- Complete PCB re-design and re-production
- Additional conformance testing

By following these steps and incorporating MIPI compliance analysis into the PCB design process, performance issues can be identified when change is easiest. Designers can easily adjust the PCB layout to improve performance and ensure designs containing MIPI devices are compliant before manufacturing and conformance testing. This shift-left process begins with an understanding of the required interface parameters to simulate and verify for MIPI M-PHY and MIPI C-PHY devices.

MIPI M-PHY
COMPLIANCE TESTING

Multimedia physical layer (M-PHY) requirements were established in 2011 to provide standards for internal mobile device data transfer. This includes the MIPI UniPro®, an IPC layer protocol that is application-agnostic. The standard has been incorporated into the JEDEC UFS open standard for high-speed interface connections. This relationship has extended adherence to M-PHY specifications to every mobile device product development type.

For M-PHY compliance, clear metrics allow designers to validate their designs for MIPI compliance and optimize the development of their mobile device, board, or system. Achieving MIPI compliance for M-PHY requires validating the following parameters:

- Pulse width
- Transition time
- Slew rate
- Common mode voltage
- Differential voltage
- Power spectral density (PSD)
- Minimal eye-opening
- Short- and long-term jitter fall*

*Within the target ranges for Type I (PWM), Type II (system), and/or high-speed signal types.

These parameters can be analyzed through:

- Transmitter (TX) Eye Mask
- Channel Tolerancing Eye Mask
- Differential Insertion Loss
- Differential Return Loss
- Stressed/Swept Jitter Test

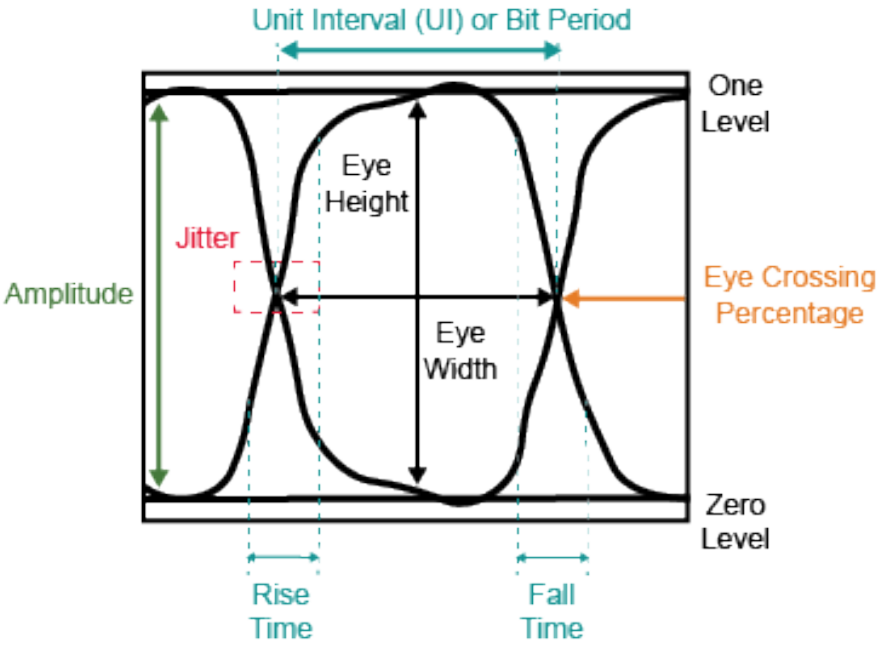
To comply with MIPI standards and regulations, these tests must produce results within a specific value range. Compliance checks are performed with S-Parameter analysis for interconnect specifications and time domain channel simulations for eye metrics.

For MIPI devices, it's important to ensure compliance not only in ideal situations but also in real-world scenarios. While the product may pass compliance in a controlled environment, exhaustive testing is performed during conformance which includes analyzing the product when outside influences are applied. Ensure your simulation software can model and analyze both ideal and real-world scenarios; this includes non-ideal power and crosstalk.

MIPI M-PHY COMPLIANCE TESTING

TRANSMITTER (TX) AND CHANNEL TOLERANCING EYE CHARACTERISTICS

Eye metrics and eye diagrams are excellent tools for visually inspecting signal integrity parameters. Using eye diagrams provides a more convenient and meaningful way to analyze large amounts of data for proper voltage and timing results.



Eye diagrams display a long sequence of data bits by chopping the stream into 2 Unit Intervals (UI) and overlaying each one on top of each other. Eye diagrams should be used to analyze the performance of the following items for MIPI M-PHY devices:

TRANSMITTER

The eye diagram of the transmitter analyzes signal transfer quality during MIPI device transmission.

CHANNEL TOLERANCING

The eye diagram for channel tolerancing analyzes signal transfer quality at the receiver.

To ensure compliance of the transmitter and receiver, the following eye characteristics should be measured on the eye diagram and evaluated:

- Eye Height
- Eye Width
- Eye Mask

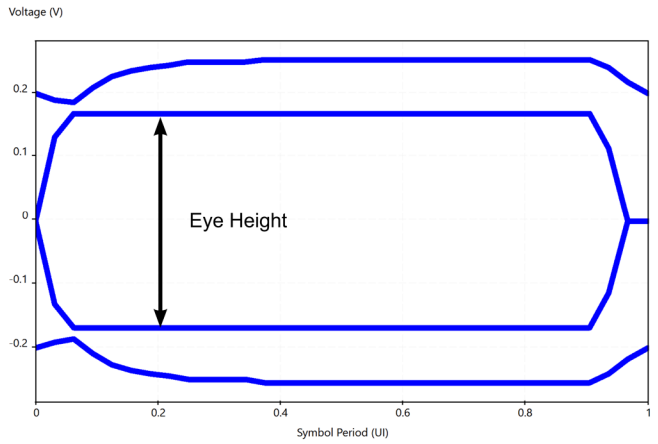
While the eye characteristics are the same for both the transmitter and channel tolerancing analysis, the values required to meet MIPI M-PHY standards vary.

MIPI M-PHY COMPLIANCE TESTING

TRANSMITTER (TX) AND CHANNEL TOLERANCING EYE CHARACTERISTICS

EYE HEIGHT

The eye height measures the vertical opening of the eye or the maximum difference between the innermost 0 bit and 1 bit voltage representations during MIPI signal transmission.



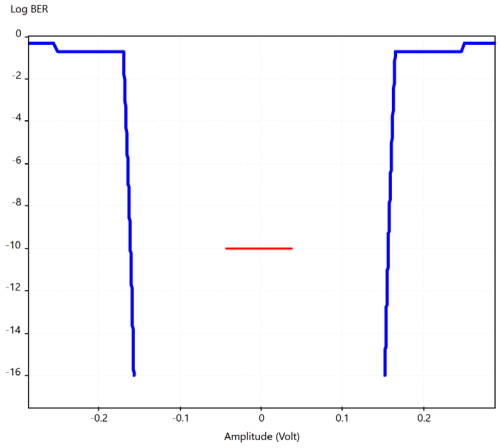
WHY IS IT IMPORTANT?

Jitter, noise, and signal attenuation directly affect eye height. Comparing the eye height to MIPI standards provides the best probability of good signal quality during signal transmission. Poor signal quality during MIPI transmission can result in:

- Unreliable data identification
- Data loss
- Erroneous system behavior
- Product shut down

HOW DO YOU MEASURE IT?

To analyze the eye height, generate the eye with a voltage scale at the BER of interest (1e-10 for MIPI technology). The eye height value can be obtained by measuring the maximum distance between the innermost '1' bit representation and the inner most '0' bit representation. This measurement should be taken in the +/-10% vicinity of the center of the bit interval or unit interval.



Eye Height is often analyzed by graphing the Log BER values against the amplitude in Volts. This generates a bathtub curve and allows you to easily assess the eye height.

WHAT IS AN ACCEPTABLE VALUE?

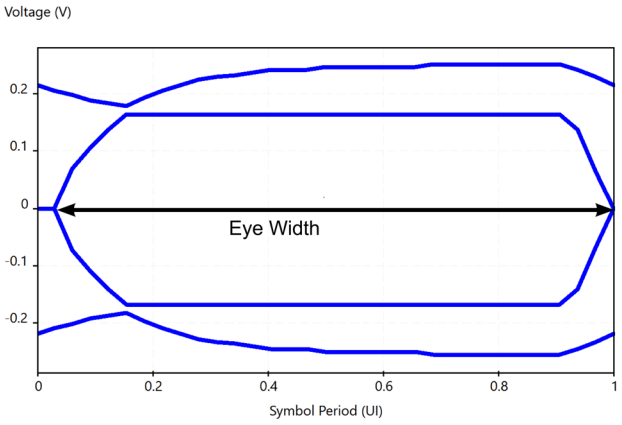
Transmitter: Greater than 80mV
Channel Tolerancing: Greater than 80mV

MIPI M-PHY COMPLIANCE TESTING

TRANSMITTER (TX) AND CHANNEL TOLERANCING EYE CHARACTERISTICS

EYE WIDTH AT ZERO CROSSING

Eye width measures the horizontal opening of the eye and provides the offset between the unit interval and where the signal peaks.

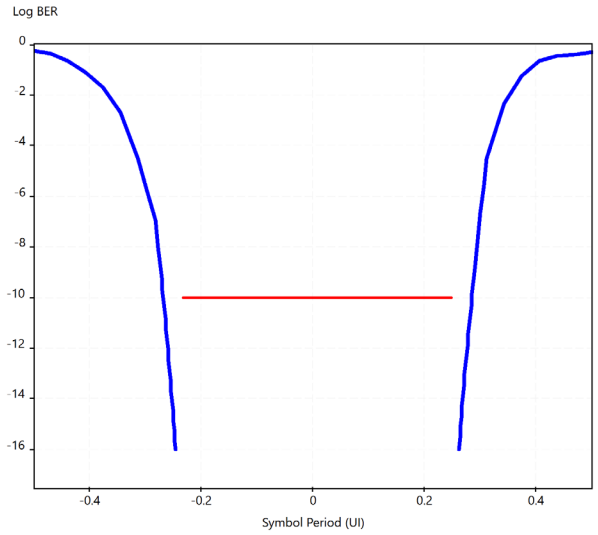


WHY IS IT IMPORTANT?

If the eye width is too small, it can indicate that your signal is out of phase or there is too much timing jitter. This can lead to the receiver inaccurately differentiating between sequential signals.

HOW DO YOU MEASURE IT?

In the eye diagram, identify the time at which the signals cross zero and measure the distance between instances.



Eye Width is often analyzed by graphing the Log BER values against the symbol period (UI). This generates a bathtub curve and allows you to easily assess the eye width.

WHAT IS AN ACCEPTABLE VALUE?

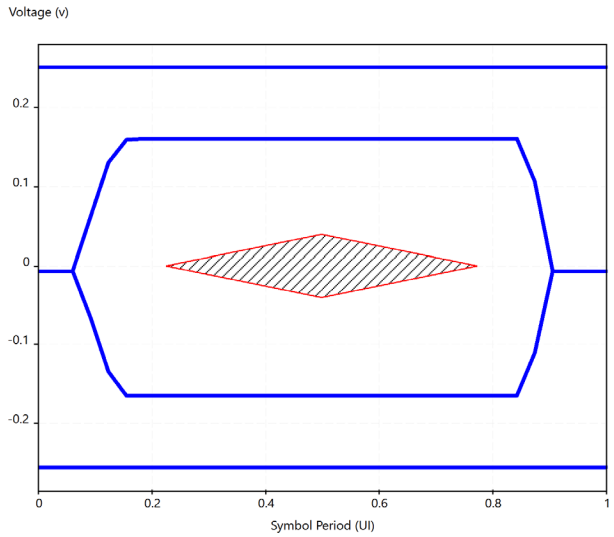
Transmitter: Greater than 0.55 UI
Channel Tolerancing: Greater than 0.48 UI

MIPI M-PHY COMPLIANCE TESTING

TRANSMITTER (TX) AND CHANNEL TOLERANCING EYE CHARACTERISTICS

EYE MASK

The eye mask shows the boundaries for signal voltages and timing data within the eye diagram.



WHY IS IT IMPORTANT?

The eye mask, which should fit within the eye diagram, provides a quick inspection method for checking how well the eye mask conforms to desired specifications. Confirming that the eye mask fits fully within the eye of the signal will ensure an error-free data transmission.

HOW DO YOU MEASURE IT?

Create a template by plotting the values for the eye mask within the eye diagram for both the Transmitter and Channel Tolerancing. To achieve the required functionality and performance, the eye mask must fit fully within the constraints of the eye.

WHAT IS AN ACCEPTABLE VALUE?

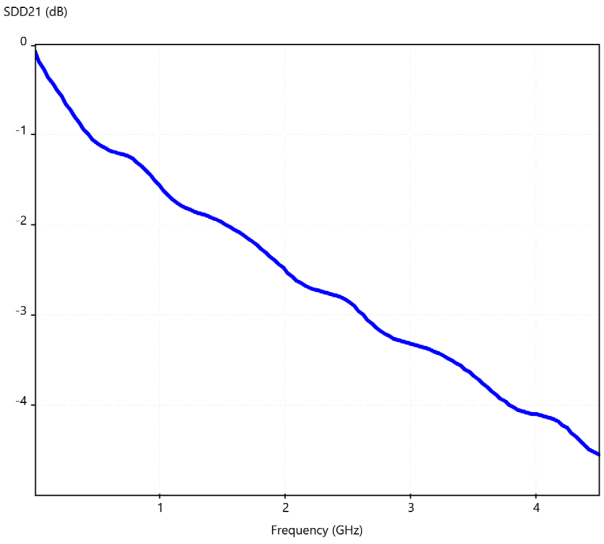
Acceptable values are given over a range of frequencies for both transmitter and channel tolerancing behavior. MIPI standards should be referenced for the required values.

Correcting eye mask issues can be difficult or impossible once the board is built. Therefore, it is important to identify potential issues during design and make the appropriate adjustments. This includes avoiding all situations that may result in stubs. Signal timing should also be thoroughly analyzed for all signal frequencies the channels may encounter during operation.

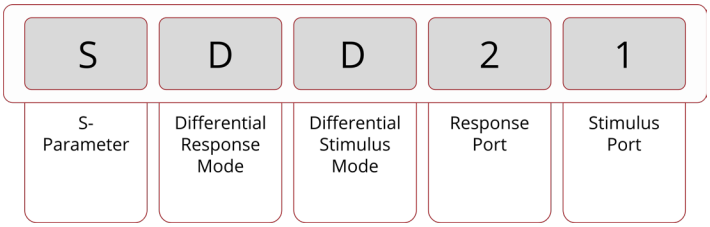
MIPI M-PHY COMPLIANCE TESTING
DIFFERENTIAL INSERTION LOSS

DIFFERENTIAL INSERTION LOSS

Differential Insertion Loss is the amount of attenuation or loss the signal will experience as it travels along a channel, in this case a differential pair net.



This is also known as SDD_{21}. The SDD_{21} parameter represents the following:



S: S-Parameter
D: Differential Response Mode (Differential receiver)
D: Differential Stimulus Mode (Differential transmitter)
2: Response Port (Port 2 or the output of receiver)
1: Stimulus Port (Port 1 or the input of transmitter)

WHY IS IT IMPORTANT?

Every data channel will result in some degree of loss due to signal attenuation; however, if the loss is too high it can lead to incorrect interpretation and unrecognizable signals at the receiver.

HOW DO YOU MEASURE IT?

Differential insertion loss is calculated by dividing the input signal at the receiver by the output signal at the transmitter. Simulate and analyze the ratio of energy at the receiving end of the channel (S-parameter port '2') to the energy introduced to the channel at the transmitter end (S-parameter port '1') over the desired frequency range.

WHAT IS AN ACCEPTABLE VALUE?

For differential signal transmission, 0.1dB/in per GHz can be expected. The acceptable value depends on the cable length and frequency in the design and can be calculated by:

0.1dB x cable length (inches) x Frequency (GHz)

If design characteristics for SDD_{21} are above the compliance range, achieving a working design will be easier than if characteristics are below the compliance range. Insertion loss can be improved by:

- Shortening transmission paths
- Lowering the impedance along traces
- Ensuring identical spacing along the paths

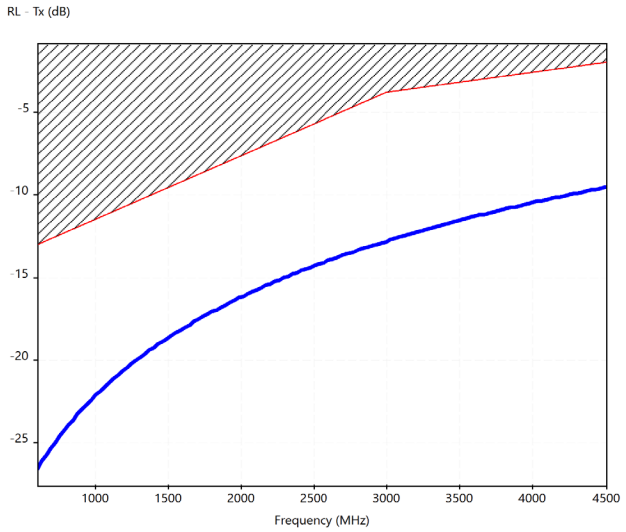
MIPI M-PHY COMPLIANCE TESTING

DIFFERENTIAL RETURN LOSS

Differential return loss or differential reflection measures how much energy is reflected in the source by the channel/receiver pair. For MIPI M-PHY devices, return loss measurements should be analyzed at both the TX and RX ports.

TX AND RX RETURN LOSS

Analyzing the differential return loss at both the receiver and the transmitter allows you to evaluate if the port is accepting enough of the signal without reflecting too much back.



The transmitter return loss is also referred to as the input differential return loss or SDD_{11}, while the receiver return loss is referred to as the output differential return loss or SDD_{22}.

WHY IS IT IMPORTANT?

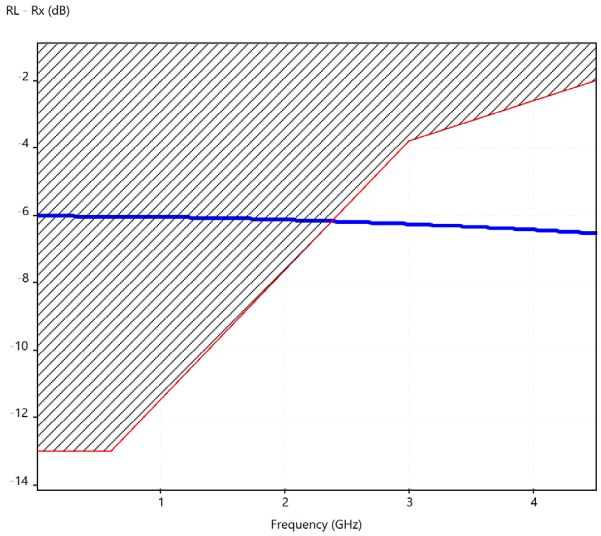
If too much energy is reflected back, the returning energy will interfere with the signal information being transferred. This can degrade signal quality and cause distortion, making it difficult to identify or differentiate between 0s and 1s. If this loss is too extensive, the signal will be unrecognizable at the receiver.

HOW DO YOU MEASURE IT?

For both TX and RX return loss, the S-Parameter amplitude should be analyzed at the corresponding port over the required frequency range.

WHAT IS AN ACCEPTABLE VALUE?

Ideally, the differential return loss would be zero; however, return loss must be less than the values indicated in the MIPI standards. These values should be plotted as a template and indicate the keepout area for the TX and RX return loss.



NOTE: The RX Return Loss plotted above indicates a compliance failure.

The following can be used as a guideline for both TX and RX return loss:

FREQUENCY	SDD_{11} OR SDD_{22}
0	-17dB
F_{SYS_MAX}	-17dB
F_{HS}	-12dB
F_{HS_MAX}	-8dB

Where:

F_{SYS_MAX} = Maximum frequency of the system clock

F_{HS} = 1/(2UIHS)

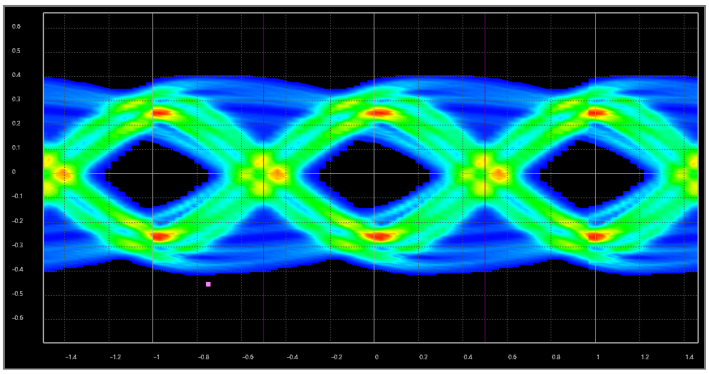
F_{HS_MAX} = ¾ $F_{HS\_MAX\_BAUD}$.

To minimize differential return loss, match impedance along the path and with the receiver for maximum power transfer. Impedance matching is crucial to keep the eye open and maintain signal integrity, especially as transfer rates rise.

MIPI M-PHY COMPLIANCE TESTING
STRESSED/SWEPT JITTER TEST

For jitter compliance testing of the MIPI device, the eye diagram must be analyzed at the Bit Error Rate (BER) of interest. Bit Error Rate (BER) is the number of bits received in error at the receiver compared to the total number of bits received. For MIPI M-PHY, the BER of interest is 10^{-10}.

STRESSED/SWEPT JITTER TEST



A stressed/swept jitter test shows the amount of jitter over a frequency sweep for the channel. The worst-case (stressed) eye diagram should be analyzed to determine the maximum jitter amplitude which produces a discernable eye at the desired BER for every frequency point.

WHY IS IT IMPORTANT?

Analyzing the Stressed/Sweep Jitter shows how much jitter margin is acceptable to accurately receive the signal at various frequencies. This lets you assess the level of resilience against flawed transmissions for your MIPI device.

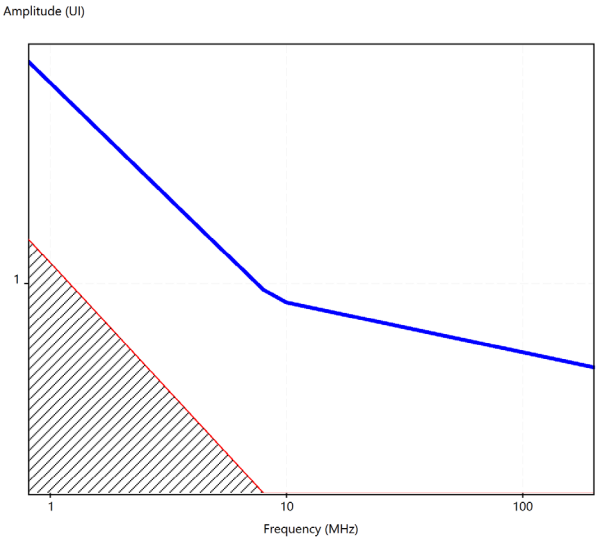
HOW DO YOU MEASURE IT?

To analyze Stressed/Swept Jitter, a plot should be created detailing the maximum jitter amplitude allowed to still have a discernible eye at the desired BER for every frequency point. For MIPI M-PHY devices, the BER of interest is 1e-10.

To improve jitter, the best solution is to shorten the channel length; otherwise, the configuration of the device may need to be adjusted. Incorporating Algorithmic Modeling Interface (AMI) models can help identify the optimal device configuration.

WHAT IS AN ACCEPTABLE VALUE?

The jitter tolerance should be compared to the values outlined in the MIPI M-PHY standards. Jitter tolerance values (UI) are provided over a range of frequencies and should be plotted against the device characteristics for efficient evaluation.



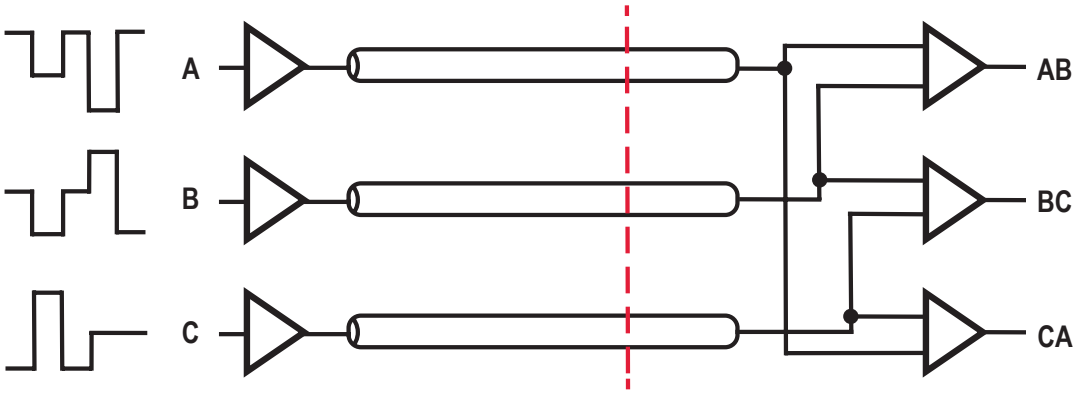
Plotting these values will create a jitter mask in which the measured results can be visually compared to ensure compliance. The following can be used as a guide to ensure the jitter amplitude is higher than the specified sinusoidal jitter values as dictated by MIPI M-PHY compliance standards:

FREQUENCY	JITTER AMPLITUDE
0.8MHz	1.5 UI
8MHz	0.15 UI
10MHz	0.15 UI
200MHz	0.15 UI

Simulating the eye characteristic metrics and S-parameter analysis of interconnect specifications for MIPI M-PHY devices will help ensure compliance to standard values during conformance testing.

MIPI C-PHY
COMPLIANCE TESTING

MIPI C-PHY devices target low-power, low-EMI, and high-performance applications within a 4-meter range. C-PHY differs from M-PHY in that a three-wire or lane signaling technology format is employed instead of two-wire differential signaling.



These differences in device performance result in the following functionality:

SYMBOL ENCODING

Symbol encoding allows for approximately 2.28 bits/symbol transmission, including a clock over one of the lanes.

SYMBOL RATE

Maximum symbol rate of 6 GB/s, translating into up to 41 GBs for three trios or three sets of three-wire lanes.

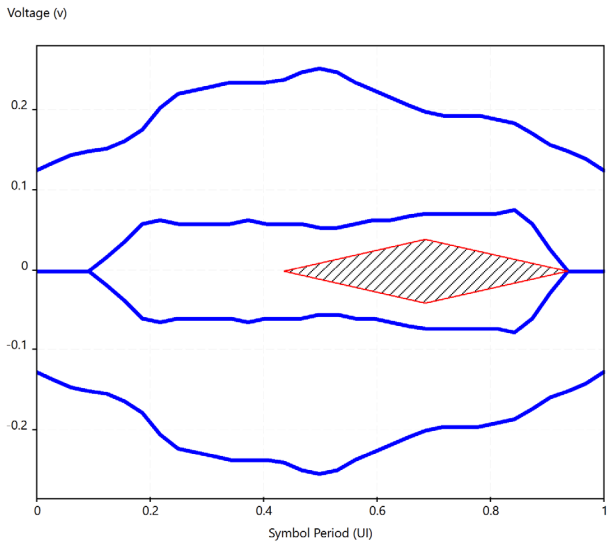
To comply with MIPI C-PHY performance standards, two checks should be performed when validating your design:

- Receiver Eye Mask
- Differential Insertion Loss

MIPI C-PHY COMPLIANCE TESTING
RECEIVER EYE MASK

RECEIVER EYE MASK

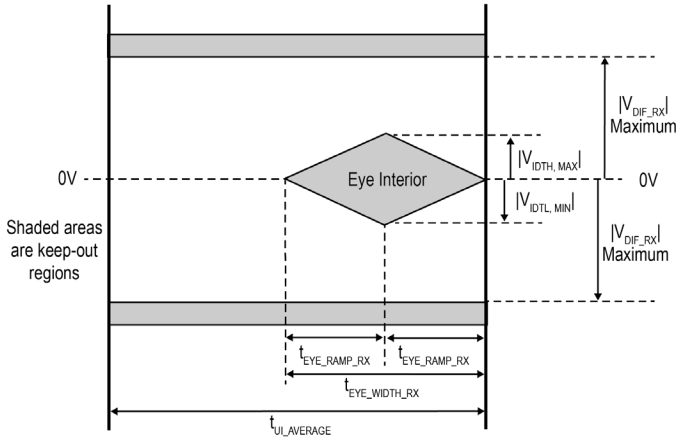
The receiver eye mask is a template detailing the boundaries for voltage and timing reference points and indicates where the eye diagram should fall. The eye mask should fit within the eye diagram and clear the inner-most signal transitions.



WHY IS IT IMPORTANT?

Analyzing the receiver eye diagram and mask ensures the signal is being understood without errors, including proper timing and voltage levels.

HOW DO YOU MEASURE IT?



The receiver eye mask should be applied to the RX eye diagram. To create the receiver eye mask, several timing parameters need to be incorporated:

- $t_{EYE\_RAMP\_RX}$: Eye ramp time at the receiver
- $t_{EYE\_WIDTH\_RX}$: Eye width at the receiver
- $t_{UI\_AVERAGE}$: Unit Interval average
- UI_{CHANN_RX}: Minimum Rx UI at the receiver
- $UI\_Jitter_{PEAK\_RX}$: Maximum Rx UI Jitter at the receiver

Voltage parameters must also be incorporated into the eye diagram. The differential voltage can be calculated with the following formula:

$$V_{DIF\_RX} = V_{IHHS,\ MAX} - V_{ILHS,\ MIN}$$

The right side of the eye mask should be aligned at the trigger point, which is the first zero crossing for any of the three differential waveforms.

WHAT IS AN ACCEPTABLE VALUE?

To analyze compliance of the RX eye diagram to MIPI C-PHY standards, the following timing specifications should be used to create the RX eye mask and keep-out regions:

PARAMETER	VALUE
$t_{EYE\_RAMP\_RX}$	0.25 UI
$t_{EYE\_WIDTH\_RX}$	0.5 UI
$t_{UI\_AVERAGE}$	1/Symbol Rate
UI_{CHANN_RX}	0.6 UI
$UI\_Jitter_{PEAK\_RX}$	0.4 UI or 0.42 UI*

* $UI\_Jitter_{PEAK\_RX}$ values are dependent on the maximum symbol rates.

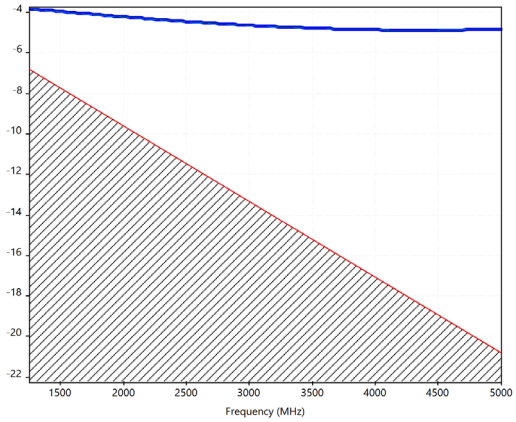
The individual device datasheet should be referenced to obtain the appropriate voltage specifications.

Eye mask problems are related to insufficient signal/energy transfer and timing misalignment and are very hard to fix once the device or board has been built.

MIPI C-PHY COMPLIANCE TESTING

DIFFERENTIAL INSERTION LOSS

Differential insertion loss analyzes the differential transfer behavior during signal transmission.



Like MIPI M-PHY compliance, differential insertion loss must be analyzed for MIPI C-PHY compliance; however, based on the application the length of channel must be specified.

WHY IS IT IMPORTANT?

Analyzing the insertion loss evaluates the loss of signal quality through transmission in differential mode. Long channel simulation and analysis enables signal integrity validation for wireless mobile systems like IoT applications.

HOW DO YOU MEASURE IT?

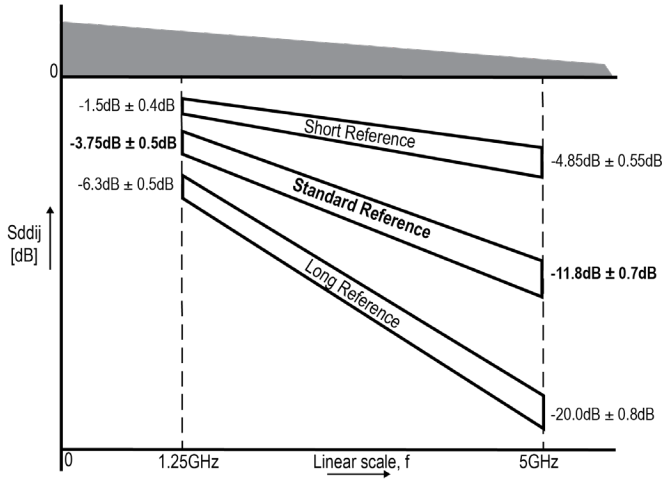
To analyze differential insertion loss, the mixed-mode S-Parameter, SDD_{21}, must be evaluated. The following formula can be used to calculate the differential insertion loss based on the single-ended parameters, assuming input ports are numbered 1 and 3, and output ports are numbered 2 and 4:

$$SDD_{21}=0.5*(S_{21}-S_{23}-S_{41}+S_{43})$$

Differential insertion loss must be analyzed for all three differential pairs (AB, BC, and CA) of the MIPI C-PHY device. The differential transfer behavior should adhere to MIPI C-PHY specifications according to the length of the channel. The following indicate the channel lengths (measured in gigasamples per second):

- Short Channel: 8 GSPS
- Standard Channel: 6 GSPS
- Long Channel: 4 GSPS

WHAT IS AN ACCEPTABLE VALUE?



The differential insertion loss must fall within the specified range for the corresponding channel length:

SHORT CHANNEL:

FREQUENCY	SHORT REFERENCE
1.25GHz	-1.5dB ± 0.4dB
5GHz	-4.85dB ± 0.55dB

STANDARD CHANNEL:

FREQUENCY	STANDARD REFERENCE
1.25GHz	-3.75dB ± 0.5dB
5GHz	-11.8dB ± 0.7dB

LONG CHANNEL:

FREQUENCY	LONG REFERENCE
1.25GHz	-6.3dB ± 0.5dB
5GHz	-20.0dB ± 0.8dB

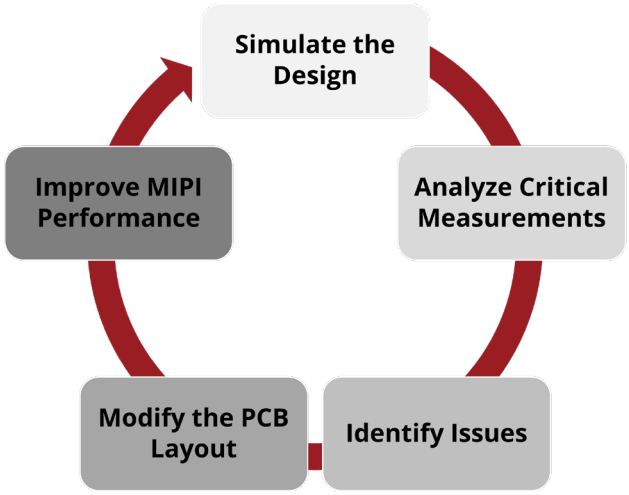
Excessive loss can be lowered by:

- Shortening traces
- Ensuring the same spacing is maintained over the entire signal path
- Impedance matching

SOLVING FOR MIPI IN-DESIGN

Post-build validation using a signal generator, oscilloscope, or other electronic testing equipment is a valid experimental method for checking whether your mobile device is MIPI compliant. However, utilizing software tools to validate compliance before manufacturing or during design is significantly more efficient. Software testing can help:

Simulating your MIPI designs will allow you to analyze critical measurements, identify issues, and make any design modifications to improve performance and ensure compliance before manufacturing and conformance testing.



It is critical that your software simulation tool be able to efficiently check and compare measurements to the required MIPI standard values. For MIPI devices, these measurements should include:

- Transmitter and Receiver Eye Masks
- Eye Width and Height
- Differential Insertion Loss
- Differential Return Loss
- Stressed/Swept Jitter

To ensure reliability, this analysis can be taken a step further to evaluate performance in a non-ideal environment, incorporating crosstalk to evaluate how EMI will affect MIPI performance. Using simulation software to analyze MIPI compliance during PCB layout will result in a more robust system design and is essential for MIPI design success.

TIPS TO IMPROVE MIPI PERFORMANCE

- **Keep traces as short as possible.**

  This will minimize signal flight time across interconnects.

- **Verify the configuration of differential traces.**

  Differential traces should have the same length, same impedance, and be spaced equidistantly apart.

- **Be cautious of noisy signals.**

  Do not place clock lines and other switching device lines close to or directly above MIPI signal lines.

- **Optimize component placement.**

  Place passive elements close to processing elements, such as FPGAs.

- **Avoid stubs in all situations**

  For example, place test points inline instead of off the transmission line path.

- **Apply fixed impedance control**

  Ensure impedance matching between transmitter and receiver. Consult your device datasheet and MIPI specifications for the corresponding impedance requirements.

ENSURING MIPI COMPLIANCE
WITH SIGRITY

Achieving MIPI compliance is rapidly becoming the standard for mobile device communications across all industry applications. The collaborations with JEDEC for UFS exemplify this realization. However, it is equally important that you can fully and efficiently vet your design for MIPI compliance.

Conformance testing that requires expensive hardware is a solution; however, simply relying on this verification technique is inefficient. For electronic circuit development, proofing with the best software simulation tools for analysis, evaluation, and compliance verification is necessary for an optimized PCB design process.

Sigrity provides kits specifically developed to help achieve MIPI compliance by:

- Performing all essential tests for MIPI C-PHY and MIPI M-PHY compliance
- Automatically analyzing simulation results against MIPI standard values
- Providing easy to read pass/fail results
- Automatically generating reports
- Providing seamless integration with other software design and analysis tools

To learn more go to:

ABOUT EMA DESIGN AUTOMATION

EMA Design Automation is a leading provider of the resources that engineers rely on to accelerate innovation. We provide solutions that include PCB design and analysis packages, custom integration software, and engineering expertise, which enable you to create more efficiently.

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