FIELD GUIDE TO DDR SIGNAL INTEGRITY ANALYSIS

EMA Design Automation®

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The demand for smart electronics has extended into virtually every industry. Consequently, many commercial, industrial, medical, automotive, aerospace and defense (A & D), and other products rely on embedded systems to deliver advanced functionality and capabilities. A critical element of these processor-based systems is data storage; the most implemented memory type is DDR.

DDR has attractive performance attributes, such as high bandwidth and low latency, that make it the preferred RAM protocol for many computing environments. Yet, there are requirements that must be adhered to when designing PCBAs with DDR. Chief among these is achieving DDR compliance. In this eBook, we discuss what performance metrics should be analyzed during the PCB design to ensure your board will successfully pass DDR compliance testing and how compliance verification can be enhanced with software simulation tools.

Throughout this e-book, click the ⓘ for more information.

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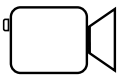
OVERVIEW OF DDR

MEETING THE NEED FOR SPEED

Double Data Rate (DDR) devices utilize both the rising and falling edges of the clock pulses to achieve faster data transmission and reception. This clock synchronization has made DDR the preferred choice for applications where fast data processing is required. DDR memory is an essential element of many of the products we use and depend on every day including:

SERVER & NETWORKING EQUIPMENT

DESKTOP, TOWERS, AND COMPUTING DEVICES



DIGITAL CAMERAS AND AV EQUIPTMENT

GPS AND NAVIGATIONAL EQUIPMENT

DDR has consistently improved its functionality and capabilities since its introduction in 2000. Major areas of enhancement between DDR iterations include TX/RX speeds, CAS latency, prefetch width, module density, and supply voltage, which is evident in the changes from DDR4 to DDR5:

ATTRIBUTES	DDR4	DDR5
YEAR	2014	2019
TRANSFER RATE	1.6-3.2 Gbs	3.2-6.4 Gbs
CAS LATENCY	10-15 Clocks	32-40 Clocks
PREFETCH WIDTH	8n	8n/16n
DENSITIES	2-16 Gb	8-64 Gb
SUPPLY VOLTAGE	1.2V/2.5V	1.1V

This thrust for continual enhancement is also evident for low-power DDR or LPDDR memory.

OVERVIEW OF DDR

MEETING THE NEED FOR SPEED **AND** LOW POWER

LPDDR is a more power-efficient version of DDR (introduced in 2014) that is often used in mobile devices such as laptops and smartphones. Attributes for LPDDR4 and LPDDR5 include the following specification changes:

Click the ⓘ for more information.

ATTRIBUTES	LPDDR4	LPDDR4X	LPDDR5	LPDDR5X
YEAR	2014	2017	2019	2021
TRANSFER RATE ⓘ	3,200 MT/s	4,267 MT/s	6,400 MT/s	8,533 MT/s
I/O CLOCK	1,600 MHz	2,133 MHz	3,200 MHz	4,267 MHz
MEMORY ARRAY CLOCK	200 MHz	266 MHz	400 MHz	533 MHz
MINIMUM SUPPLY VOLTAGE	1.1 V	0.6 V	0.5 V	0.5V

For some applications, incorporating LPDDR instead of standard DDR devices is crucial to extend the battery life of the device; however, designers should weigh the design trade-offs including:

Low Power

LPDDR devices have additional features to achieve low power including, deep sleep mode, low refresh rate of the memory when idle, and more.

Increased Verification Complexity

Power needs to be considered throughout analysis, especially in low-power applications. It becomes even more critical to analyze how power fluctuations can have a material effect on signal quality as well as to ensure adequate power can be delivered.

Soldering

LPDDR must be soldered onto the board. This can save crucial PCB space; however, results in a device that is not upgradeable.

Cost

Compared to DDR devices, LPDDR comes at an increased cost due to the higher efficiency and smaller package size.

Whether opting for the shorter latency/lower cost of DDR4, the faster transfer rate and higher density of DDR5, or one of the high-efficiency LPDDR versions, achieving DDR compliance is essential for the success of your product. All DDR devices are managed by defined specifications. The remainder of this e-book will discuss what these specifications include and how they will guide you in achieving compliance.

DDR COMPLIANCE TESTING

JEDEC SPECIFICATIONS

Any board that includes memory needs to satisfy standards that ensure reliable interface operation between modules, processors, and other products. The Joint Electron Device Engineering Council (JEDEC) is the globally recognized organization for setting the standards for DDR memory and other solid-state devices.

JEDEC and its members develop open standards that promote cooperation among electronic industry companies to design and build products that ensure interoperability. This level of collaboration helps protect consumers against inferior products while advancing innovation and minimizing development costs. The JEDEC standards are extensive and provide specifications for all aspects of DDR memory. For example, publications for DDR5 include the following:

Click the ⓘ for more information.

JEDEC DDR5 PUBLICATIONS	DESCRIPTION
JESD79-5B	DDR5 SDRAM specifications.
JESD82-11, 12, and 13	DDR5 RCD ⓘ specifications.
JESD82-521	DDR5 Buffer Interface specifications.
JESD400-5A.01	DDR5 SPD ⓘ values.
JESD401-5A	DDR5 Label specifications.
JESD309	DDR5 SODIMM ⓘ specifications.
JESD308	DDR5 UDIMM ⓘ specifications.

This is not an exhaustive list for DDR5 and similarly, several publications exist for DDR4, LPDDR4, and LPDDR5. In order to ensure compliance for your DDR device, the first step is to determine the corresponding JEDEC standard.

DDR COMPLIANCE TESTING

DETERMINING JEDEC STANDARDS

With numerous JEDEC standards, it's important to identify which standard and performance specifications should be used for your DDR device. JEDEC standards, and the resulting acceptable values for performance, can be determined based on the DDR device specifications and operation parameters:

AC/DC Threshold

AC Threshold and DC threshold values define the device performance, operation, and consequently the JEDEC compliance values for:

- DDR1
- DDR2
- DDR3
- LPDDR1
- LPDDR2

DC threshold (mV) defines the level the input must maintain for a given state. AC threshold (mV) defines the level the input must exceed to force a change in state.

Data Transfer Rates

The speed at which the DDR device transfers data will dictate the JEDEC compliance values for:

- DDR4
- DDR5
- LPDDR4
- LPDDR4x

Common data rates for these DDR devices include 1,600 MT/s, 2,400 MT/s, 3,200 MT/s, 4,000 MT/s, 4,800 MT/s, and 6,400 MT/s.

Clock Speed

The evolution of LPDDR5 introduced a new clocking scheme which dictates the corresponding JEDEC compliance values. The speed of the Clock (CK) signal and Write Clock (WCK) signal should be considered when evaluating LPDDR5 compliance.

Signaling Method

GDDR6 devices, typically used to support high-bandwidth applications such as game consoles, use a Pseudo-Open Drain (POD) configuration. POD is a signaling method where the current required for driving a signal high is eliminated, resulting in less power consumption. The voltage values for the POD configuration dictate the required JEDEC compliance values, typically 1.25V (POD125) and 1.35V (POD135).

These DDR performance characteristics and parameters, typically obtained from the manufacturer datasheet, will help determine which JEDEC specification should be adhered to throughout your PCB design and conformance testing.

The acceptable DDR compliance values throughout this e-book will focus on DDR5 devices with a data transfer rate of 6,400 MT/s, as this is the latest device and fastest transfer rate available.

DDR COMPLIANCE TESTING

WHAT TO MEASURE?

To verify your design for DDR compliance to these JEDEC specifications, the following parameters should be measured and compared with the appropriate DDR standard(s):

- Eye Width
- Eye Height
- Overshoot
- Undershoot
- Ringback
- Jitter Margin
- Noise Margin
- DQ to DQS Skew
- Skew Across All DQ
- Slew Rates
- Interconnect Skew
- Strobe Interconnect Skew

Data and analysis results from these measurements are critical as they are the primary metric used by JEDEC to evaluate:

SIGNAL QUALITY BIT SYNCHRONIZATION CHANNEL INTERFERENCE NOISE

Verifying these measurements adhere to the desired performance objectives and fall within the defined JEDEC specification values during the PCB layout is critical to passing compliance testing once the PCB is built.

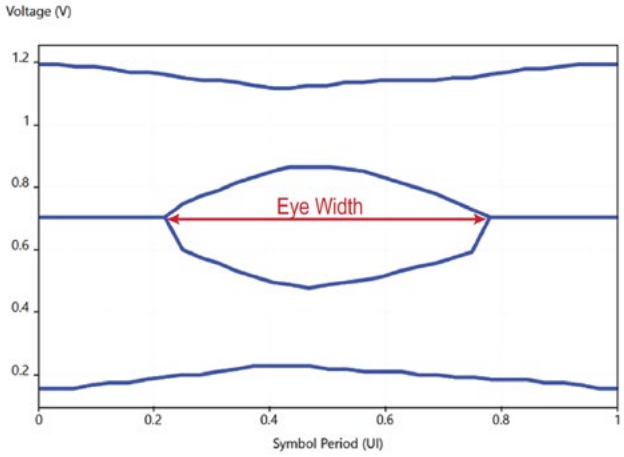
DDR COMPLIANCE TESTING

BER REPORTS: EYE WIDTH

Much of the important data needed to evaluate these items and the quality of DDR interface signal transfer can be visualized from an eye diagram. Bit Error Rate (BER) reports provide valuable feedback about the ratio of bit transfer failures to actual bits sent. For DDR Compliance testing, the eye width and eye height can be evaluated with BER Reports at the area of interest. The BER of interest will vary based on the DDR technology and characteristics.

EYE WIDTH

Eye width measures the horizontal opening of the eye, providing the offset between the unit interval and where the signal peaks.

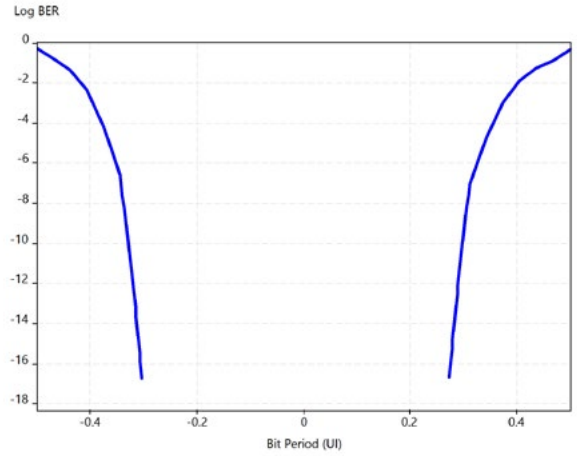


WHY IS IT IMPORTANT?

Eye width provides an indication of the quality of signal transmission. If the eye width is too small, the signal may be out of phase or there may be too much timing jitter. This can lead to inaccurate differentiation between sequential signals.

HOW DO YOU MEASURE IT?

The eye width is determined by measuring the statistical mean of transitions (rise and fall times) or the horizontal eye opening.



Eye width is often analyzed by graphing the Log BER values against the symbol period (UI). This generates a bathtub curve and allows you to easily assess the eye width.

WHAT IS AN ACCEPTABLE VALUE?

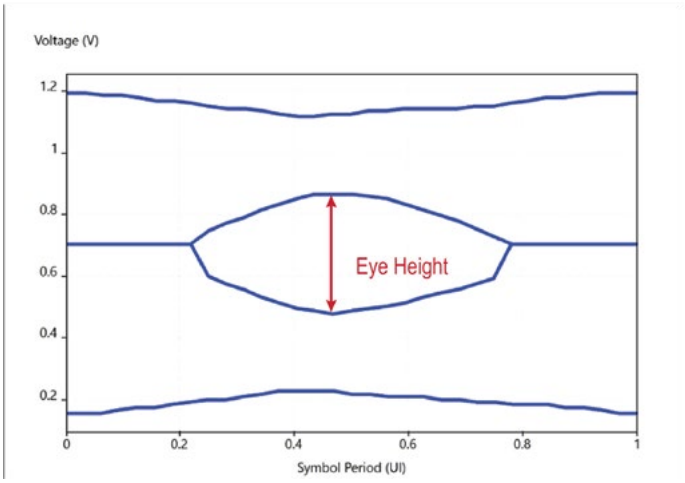
Values for eye width vary based on the DDR device, speed, and operating characteristics. For DDR5 with a transfer rate of 6,400 MT/s eye width should be greater than 0.25UI.

DDR COMPLIANCE TESTING

BER REPORTS: EYE HEIGHT

EYE HEIGHT

Eye height evaluates how much amplitude separation there is between 0s and 1s during DDR transmission by measuring the vertical opening of the eye.



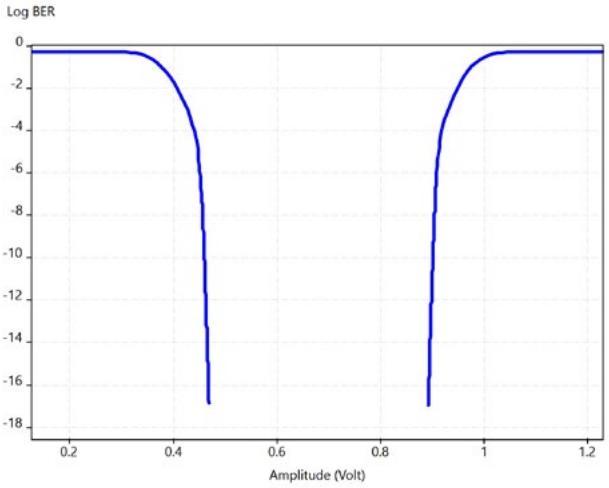
WHY IS IT IMPORTANT?

The eye height provides information about the quality of signal transmission. A narrow eye height increases the likelihood of unreliable data identification. This may lead to:

- Data Loss
- Erroneous System Behavior
- Product Shut Down

HOW DO YOU MEASURE IT?

The eye height is determined by measuring the vertical opening of the eye.



Eye height is often analyzed by graphing the Log BER values against the amplitude in Volts. This generates a bathtub curve, also referred to as the noise bathtub, and allows you to easily assess the eye height.

WHAT IS AN ACCEPTABLE VALUE?

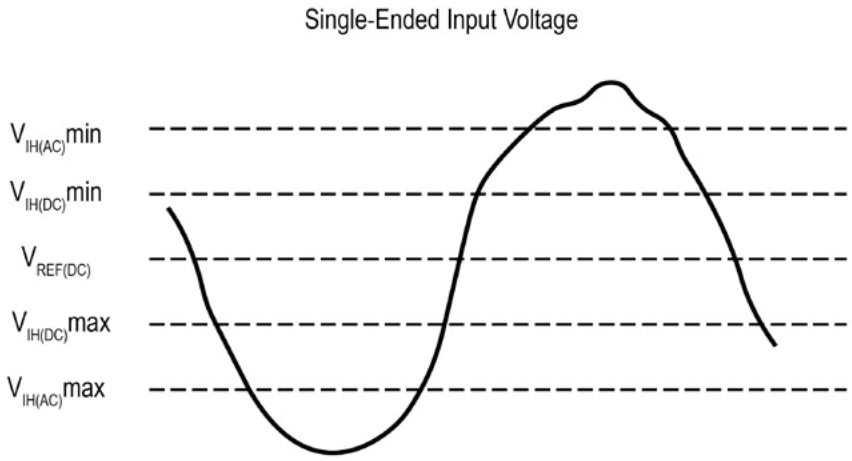
Values for eye height vary based on the DDR device, speed, and operating characteristics. For DDR5 with a transfer rate of 6,400 MT/s eye height should be greater than 0.7mV.

Insufficient eye width and/or eye height typically means there is excessive noise or jitter. Correcting these issues may require switching components and/or altering layout parameters.

DDR COMPLIANCE TESTING

AC AND DC LOGIC LEVELS

To calculate many of the remaining DDR compliance items, AC and DC logic levels must be determined. JEDEC specifications define the acceptable values for DDR performance including AC threshold and DC threshold allowing you to calculate the minimum and maximum corner voltages or AC and DC logic levels:



SINGLE-ENDED VOLTAGE PARAMETERS

$V_{IH(ac)}$ Min:

AC voltage value required to force a low-to-high state change

$V_{IH(dc)}$ Min:

High state DC maximum threshold voltage

$V_{IL(dc)}$ Max:

Low state DC minimum threshold voltage

$V_{IL(ac)}$ Max:

AC voltage value required to force a high-to-low state change

These values should be calculated based on the signal configuration, single-ended or differential, as well as the type of DDR technology including DDR iteration and LPDDR iteration.

DDR COMPLIANCE TESTING

AC AND DC LOGIC LEVELS

For single-ended and differential signals, the corner voltage values for AC and DC logic levels should be calculated based on the type of DDR technology.

SINGLE-ENDED SIGNALS

For DDR4, the single-ended corner voltages for AC and DC logic levels can be calculated with the following equations:

$V_{IH(ac)}Min = 0.25 + V_{REF}$

$V_{IL(ac)}Max = -0.25 + V_{REF}$

$V_{IH(dc)}Min = 0.15 + V_{REF}$

$V_{IL(dc)}Min = -0.15 + V_{REF}$

If V_{REF} is set to on-the-fly, it is calculated as:

$V_{REF} = V_{cent\_DQ}$ or V_{cent_CA}

For LPDDR4, the single-ended corner voltages for AC and DC logic levels can be calculated with the following equations:

$V_{IH(ac)}Min = 0.5*VdIVM + V_{REF}$

$V_{IL(ac)}Max = -0.5*VdIVM + V_{REF}$

$V_{IH(dc)}Min = 0.5*VdIVM + V_{REF}$

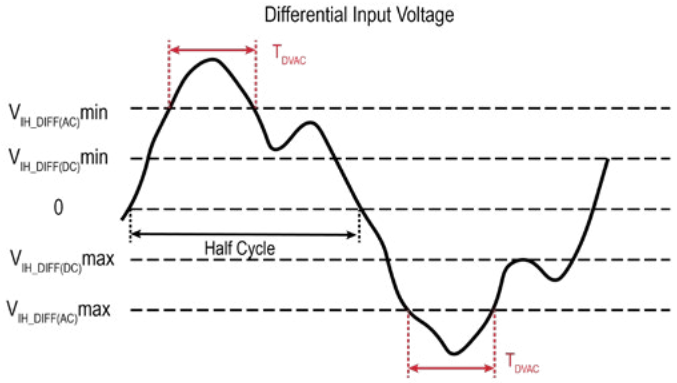
$V_{IL(dc)}Min = -0.5*VdIVM + V_{REF}$

If V_{REF} is set to on-the-fly, it is calculated as:

$V_{REF} = V_{cent\_DQ}$ or V_{cent_CA}

These calculations will depend on the device and specification you are trying to meet.

DIFFERENTIAL SIGNALS



For DDR4, the single-ended corner voltages for AC and DC logic levels can be calculated with the following equations:

$V_{IHdiff(ac)}Min = 2 * (V_{IH(ac)}Min – V_{IL(ac)}Max)$

$V_{ILdiff(ac)}Max = 2 * (V_{IL(ac)}Max – V_{IH(ac)}Min)$

$V_{IHdiff(dc)}Min = 0.15$

$V_{ILdiff(dc)}Max = - 0.15$

For LPDDR4, the corner voltage values for the AC logic are calculated the same; however, the DC logic levels can be calculated with the following equations:

$V_{IHdiff(dc)}Min = V_{IH(dc)}Min – V_{IL(dc)}Max$

$V_{ILdiff(dc)}Max = V_{IL(dc)}Max – V_{IH(dc)}Min$

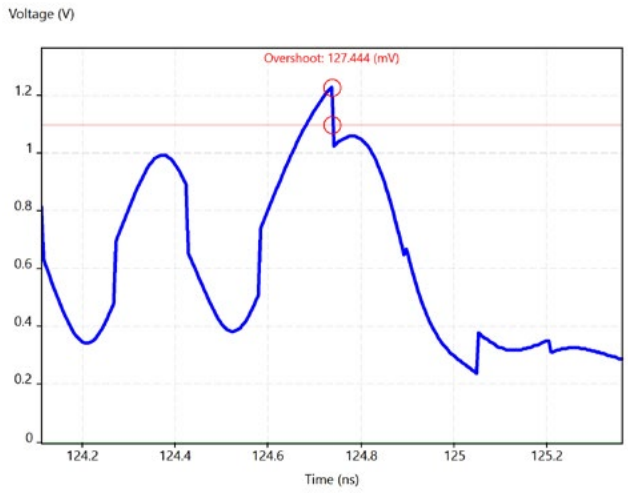
If these threshold values are not maintained, the DDR device may not work as expected. Determining the acceptable AC and DC logic levels will provide a baseline for the remainder of the compliance calculations.

DDR COMPLIANCE TESTING

WAVEFORM QUALITY: OVERSHOOT

Waveform quality is a qualitative term for the overall compliance of various quantitative metrics for DDR signal transfer. Waveform quality provides a summary that is indicative of how reliable data transfer will be to and from your DDR modules. For DDR compliance, overshoot, undershoot, and ringback should be evaluated.

OVERSHOOT

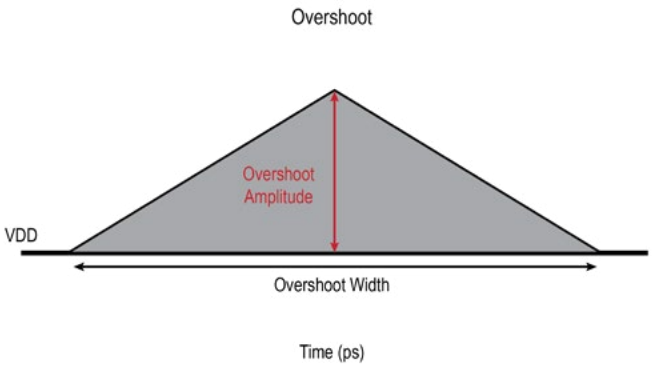


Overshoot occurs when the signal exceeds the nominal or desired amplitude during signal transitions and is the maximum excursion of the signal over the power rail.

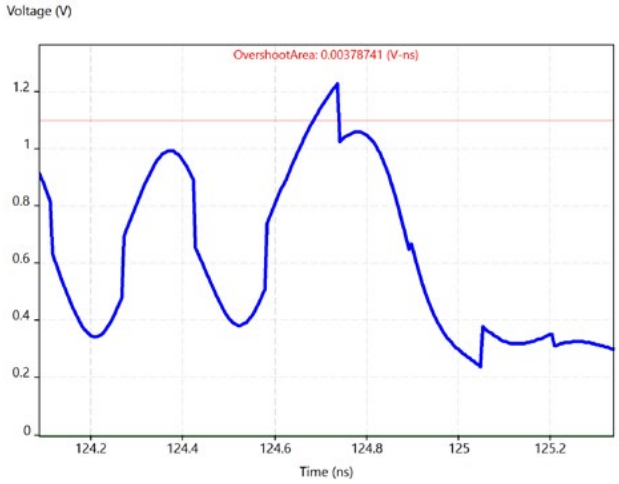
WHY IS IT IMPORTANT?

Overshoot is a common feature when feedback is used for error correction; however, it is undesirable for filtered signal processing typical for DDR design. Analyzing overshoot provides a good indication of signal quality as any issues are usually indicative of excess noise accompanying the signal, either from the source or along the channel.

HOW DO YOU MEASURE IT?



Both the maximum overshoot amplitude and the overshoot area should be evaluated. For the maximum overshoot, measure the maximum amplitude of the signal above VDD.



The overshoot area can be calculated by:

0.5 x Overshoot Amplitude (V) x Overshoot Width (ns)

WHAT IS AN ACCEPTABLE VALUE?

The maximum amplitude and overshoot area is the amount of over-voltage the device can take without damage. These values can be obtained from the device datasheet.

DDR COMPLIANCE TESTING

WAVEFORM QUALITY: UNDERSHOOT

UNDERSHOOT

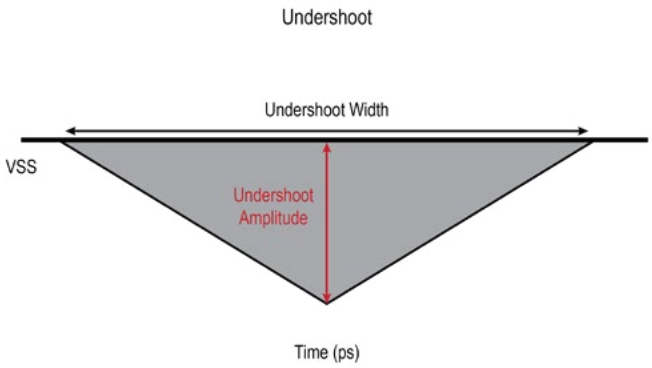
Undershoot occurs when a signal does not reach the nominal or desired amplitude during signal transitions and is the minimum excursion of the signal below the ground reference.

WHY IS IT IMPORTANT?

Analyzing undershoot provides a good indication of signal quality as any issues are usually indicative of excess noise accompanying the signal, either from the source or along the channel.

DDR devices often incorporate a voltage protection diode located on the input pin for protection against undershoot damage.

HOW DO YOU MEASURE IT?



Both the maximum undershoot and the undershoot area should be evaluated. For the maximum undershoot, measure the maximum amplitude of the signal below VSS. The undershoot area can be calculated by:

0.5 x Undershoot Amplitude (V) x Undershoot Width (ns)

WHAT IS AN ACCEPTABLE VALUE?

The maximum amplitude and undershoot area is the amount of undershoot voltage the device can take without damage. These values can be obtained from the device datasheet.

DDR COMPLIANCE TESTING

WAVEFORM QUALITY: RINGBACK

RINGBACK

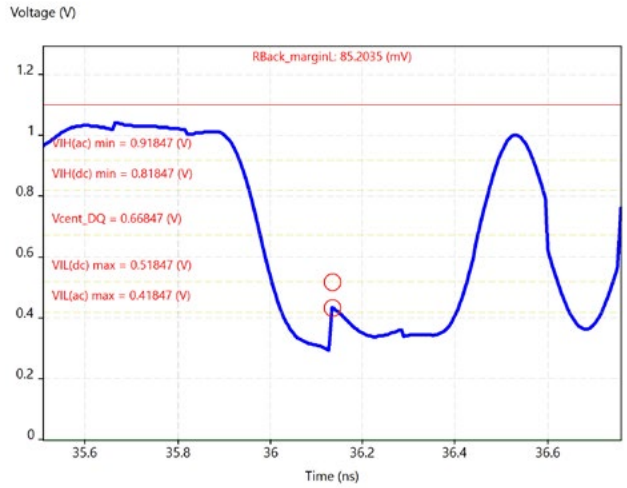
Ringback is the oscillatory behavior on a waveform before the signal finally settles into a nominal state. Ringback margin measures how much ringback is tolerable without creating a signal error.

WHY IS IT IMPORTANT?

Ringback can be used to identify signal quality issues, such as reflection along a transmission path due to impedance mismatch.

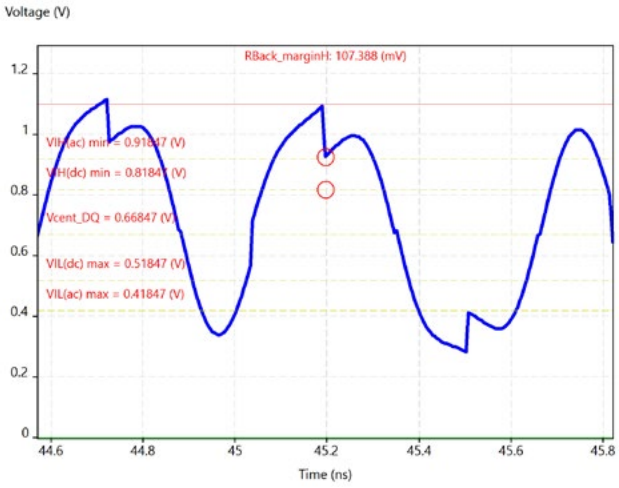
HOW DO YOU MEASURE IT?

Ringback margins should be calculated for both high and low logic levels for each signal of the bus.



To calculate the Low Ringback Margin locate the highest point after the initial 1 to 0 signal transition when the signal has moved through the $V_{IH(dc)}$Min, $V_{IL(dc)}$Max, and $V_{IL(ac)}$Max positions. Measure the voltage difference between $V_{IL(dc)}$Max and this highest signal point.

These signal quality issues may be correctable by trace rerouting or other layout redesigns. However, they may also be due to material selection such as improper dielectric constant choices.



To calculate the High Ringback Margin locate the lowest point after the initial 0 to 1 signal transition when the signal has moved through the $V_{IL(dc)}$Max, $V_{IL(dc)}$Min, and $V_{IL(ac)}$Min positions. Measure the voltage difference between this lowest signal point and $V_{IH(dc)}$Min.

Additionally, the time at which ringback occurs must be analyzed. If ringback occurs before the specified T_{ac} time point, where the device has seen the signal above the $V_{IH(ac)}$Min or below the $V_{IL(ac)}$Max values for the poper amount of time, it will result in a compliance failure.

If ringback occurs after the T_{ac} time point that is higher than $V_{IH(dc)}$, it does not impact the eye-width measurement and is therefore not a failure.

The T_{ac} time point can be derived from the characteristics of the input drivers of the device specified in the device datasheet.

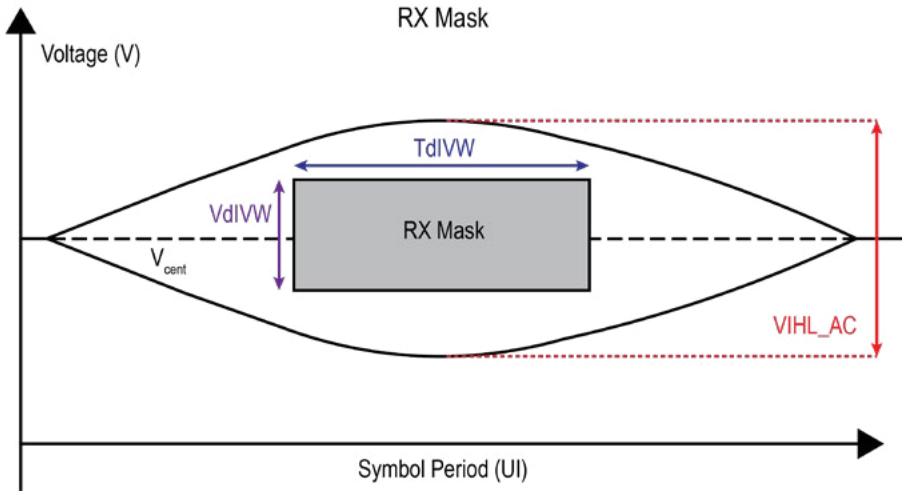
WHAT IS AN ACCEPTABLE VALUE?

For acceptable ringback, the ringback margin should be greater than 0mV and occur after the defined T_{ac} time point. This means the high ringback and low ringback should not surpass the $V_{IH(dc)}$Min and $V_{IL(dc)}$Max values respectively.

DDR COMPLIANCE TESTING

DQ MASKS

DQ Masks are applied to the receiver eye diagram during data write simulations to analyze signal performance. Masks are applied to the eye diagram as a way of representing data to facilitate testing or analysis.



JEDEC defines compliance specifications for data (DQ) and strobe (DQS) masking by providing values for the mask characteristics including:

RX MASK PARAMETERS	
VdIVW:	**VIHL_AC:**
Peak-to-Peak RX Mask Voltage	Peak-to-Peak DQ AC input swing
TdIVW:	**V_{cent_DQ}:**
RX Timing Window	The midpoint between the largest and smallest V_{ref_DQ} voltage levels across all DQ pins for a given DRAM component.

These values can be used to create the receiver mask (RX mask). This RX mask defines the area in which the input signal must not encroach to successfully capture a valid input signal at the DRAM input receiver. During signal analysis, this can be determined by ensuring the RX mask fits fully within the opening of the eye diagram. Evaluating the interaction between the RX mask and eye diagram can provide insight to crucial DDR performance metrics, such as jitter margin and noise margin.

For DDR5 with a transfer rate of 6,400 MT/s, the following values should be used to create an RX mask to ensure compliance:

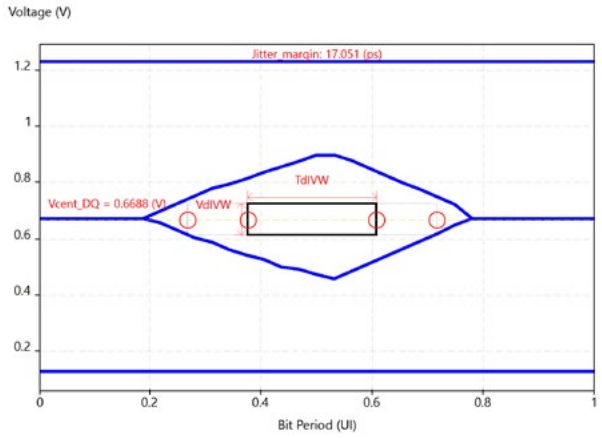
- VdIVW: 130 mV
- TdIVW: 2UI
- VIHL_AC: 150mV

DDR COMPLIANCE TESTING

DQ MASKS: JITTER AND NOISE MARGINS

JITTER MARGIN

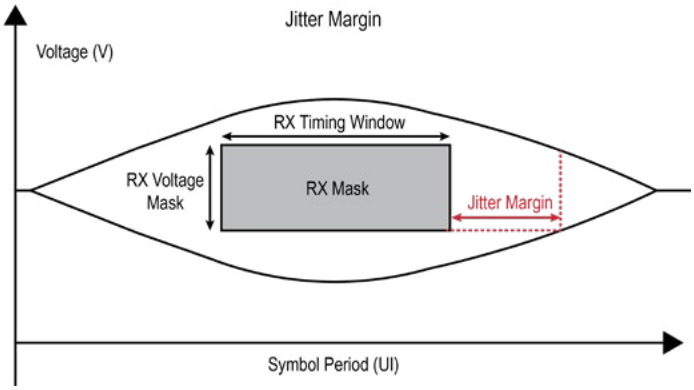
Jitter margin measures how much timing delay or jitter is tolerable without creating a signal error.



WHY IS IT IMPORTANT?

Any variations in timing will create jitter. If too much jitter exists, the signal can become distorted or misinterpreted. Measuring the jitter margin will ensure proper signal functionality when timing variations are introduced into the system.

HOW DO YOU MEASURE IT?



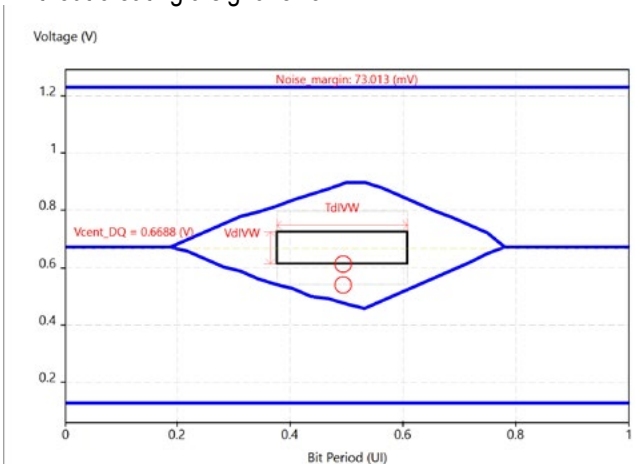
Plot the RX Eye Mask then measure the symbol period margin (UI) or horizontal distance between the RX eye mask and receiver eye diagram.

WHAT IS AN ACCEPTABLE VALUE?

The jitter margin should be greater than 0 picoseconds. A larger jitter margin is preferred to allow for slight timing variations.

NOISE MARGIN

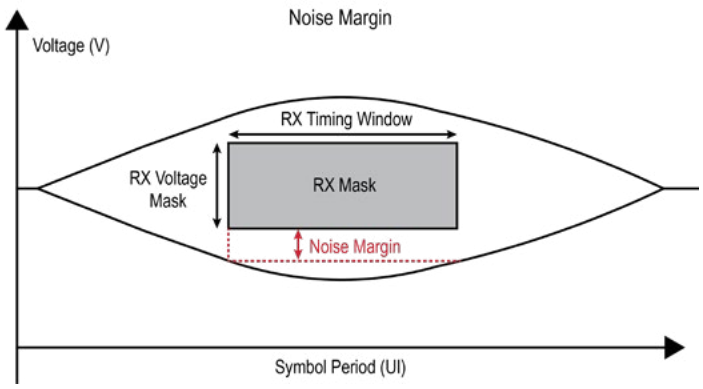
Noise margin is the amount of noise the system can absorb without creating a signal error.



WHY IS IT IMPORTANT?

Measuring the noise margin will ensure proper signal functionality even when additional noise is introduced into the system. The noise margin determines how much noise the system can absorb without creating a signal error.

HOW DO YOU MEASURE IT?



Plot the RX Eye Mask then measure the voltage margin (mV) or vertical distance between the RX eye mask and receiver eye diagram.

WHAT IS AN ACCEPTABLE VALUE?

The noise margin should be greater than 0mV. A larger noise margin is preferred to allow for the effects of noise.

DDR COMPLIANCE TESTING

DQ MASKS: TIMING

Timing is critical in DDR device operation. In order to accurately analyze DDR performance, a timing budget should be configured with specifications from the DDR device datasheet. This is typically specified with either setup and hold times or skew:

WRITE (DATA, ADDCMD, AND CTRL BUSES)

Minimum Transmit Setup

The minimum amount of setup time that is guaranteed to exist between the signals and their timing reference at the driving component (controller).

Minimum Transmit Hold

The minimum amount of hold time that is guaranteed to exist between the signals and their timing reference at the driving component (controller).

Minimum Receive Setup

The amount of setup time required between the signals and their timing reference at the receiving component (memory). This parameter is typically provided in the device datasheets as $t_{DS(base)}$ for Data buses and $t_{IS(base)}$ for AddCmd buses.

Minimum Receive Hold

The amount of hold time required between the signals and their timing reference at the receiving component (memory). This parameter is typically provided in the device datasheets as $t_{DH(base)}$ for Data buses and $t_{IH(base)}$ for AddCmd buses.

READ (DATA BUSES ONLY)

Max Receive Skew (+)

The maximum amount by which the Data is allowed to lag the Strobe at the receiving component (controller).

Max Receive Skew (-)

The maximum amount by which the data is allowed to lead the strobe at the receiving component (controller).

Transmit Skew (+)

The maximum amount that the Data will lag the Strobe signal at the driving component (controller). This parameter is typically provided in the memory datasheet as t_{DQSQ}.

Transmit Skew (-)

The maximum amount that the Data will lead the Strobe signal at the driving component (controller). This parameter is typically provided in the memory datasheet as t_{QH}.

From this information the Skew Budget can be calculated. The Skew budget is intended to show the user how much skew can be introduced by the interconnect while still meeting timing requirements. These are calculated as follows:

WRITE

Setup (Skew Budget) =

Min Transmit Setup – Min Receive Setup

Hold (Skew Budget) =

Min Transmit Hold – Min Receive Hold

READ

(+) (Skew Budget) =

Max Receive Skew (+) – Transmit Skew (+)

(-) (Skew Budget) =

Max Receive Skew (-) – Transmit Skew (-)

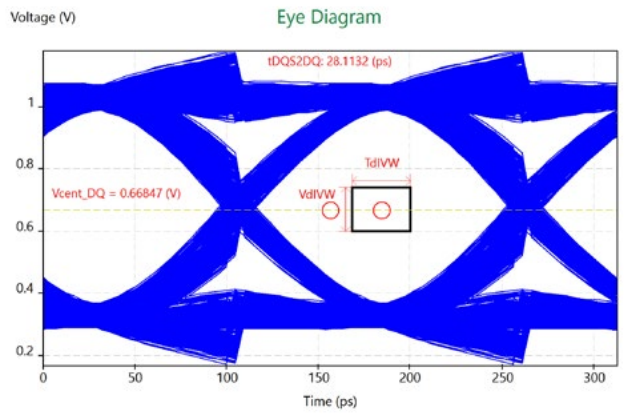
Configuring the timing specifications associated with the transmitting component enables worst-case phase shifts to be applied on the timing reference signal to simulate worst case timing conditions and ensure the DDR device performance is still within compliance even in worst-case operation.

DDR COMPLIANCE TESTING

DQ MASKS: SKEW

DQ TO DQS SKEW

DQ to DQS Skew is the time between the strobe (DQS) and signal (DQ) transmission.

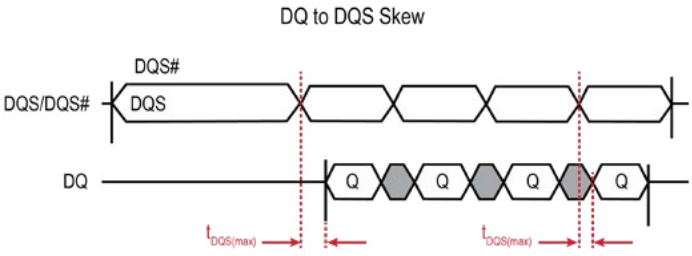


WHY IS IT IMPORTANT?

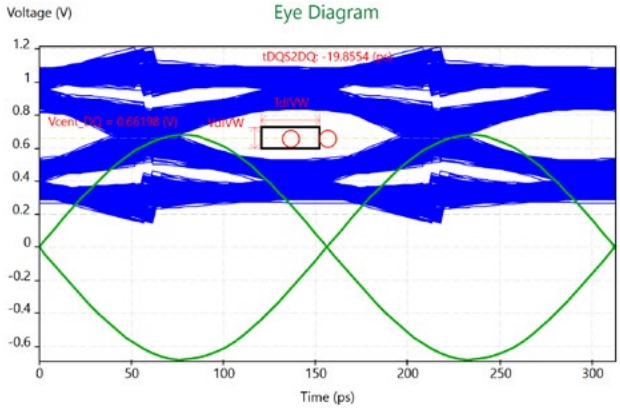
Inadequate DQ to DQS skew effectively reduces the size of the data eye for successful signal transmission.

HOW DO YOU MEASURE IT?

To ensure proper timing of the DDR device, both the minimum and maximum values for DQ to DQS Skew should be evaluated.



Measure the time between the end of the strobe transmission and the beginning of the signal transmission.



When analyzing the eye diagram, this can be achieved by measuring the horizontal distance between the midpoint of the DQ signal's RX mask and the latch point. The latch point is the time point where the differential strobe (or DQS) crosses.

WHAT IS AN ACCEPTABLE VALUE?

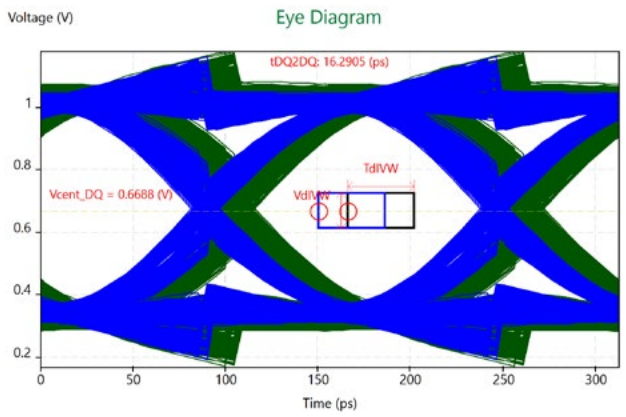
The time or skew between DQ and DQS signal transmissions must fall between a minimum of -1 UI and a maximum 1UI for DDR5 with a data transfer rate of 6,400 MT/s.

DDR COMPLIANCE TESTING

DQ MASKS: SKEW

SKEW ACROSS ALL DQ

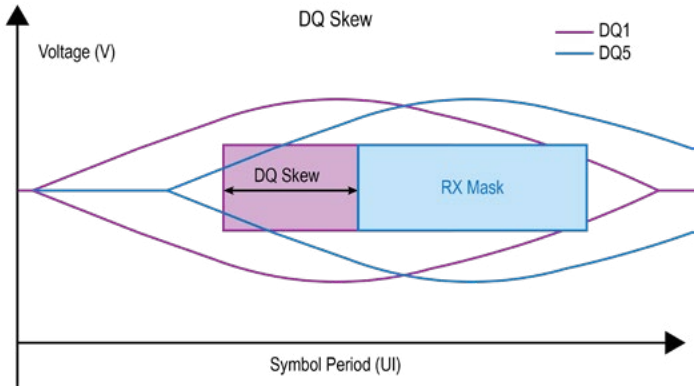
The skew across all DQ is the time delay or variations between all DQ signals in a group.



WHY IS IT IMPORTANT?

The skew across all DQ signals must match within an acceptable tolerance to ensure accurate timing and signal transmission.

HOW DO YOU MEASURE IT?



When analyzing the eye diagrams of the DQ signals, measure the horizontal distance or time (picoseconds) between the RX masks for each DQ signal in the group.

WHAT IS AN ACCEPTABLE VALUE?

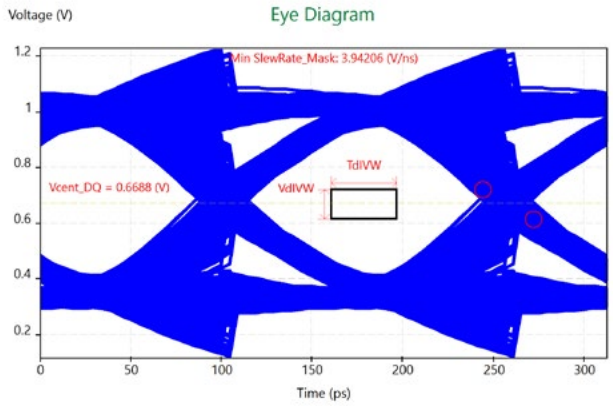
Per the corresponding JEDEC specifications, the maximum DQ to DQ skew should be less than 0.5 Unit Interval (UI) for DDR5 with a data transfer rate of 6,400 MT/s.

DDR COMPLIANCE TESTING

DQ MASKS: SLEW RATE

SLEW RATE

Slew rate is the amount of change in voltage over time or how fast the signal edge is.

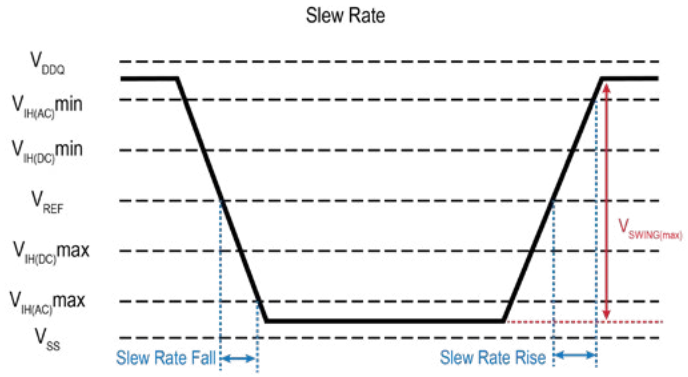


WHY IS IT IMPORTANT?

Too much variation will result in an increased BER and unreliable operation.

HOW DO YOU MEASURE IT?

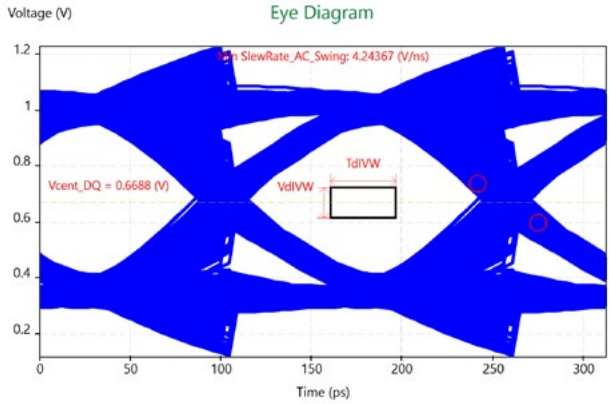
To accurately determine the slew rates for DDR devices, derating must be incorporated into the simulation. Derating information contains setup or hold scaling constants for specified slew rates and can be obtained from device datasheet. This is often input as a table and is used to adjust the setup and hold requirements when the edge rate is not what's expected.



To calculate the AC swing, measure the voltage difference between $V_{IH(ac)}$Min and $V_{IH(ac)}$Max. Divide this value by the time it took to make this transition.

To calculate the falling slew rate, measure the voltage difference between V_{REF} and $V_{IH(ac)}$Max and divide it by the time it took to achieve this transition.

To calculate the rising slew rate, measure the voltage difference between $V_{IH(ac)}$Min and V_{REF} and divide it by the time it took to achieve this transition.



WHAT IS AN ACCEPTABLE VALUE?

The AC Swing should be between 0.2V/ns and 9 V/ns. Both the rising and falling slew rates should be between 1 V/ns and 7V/ns.

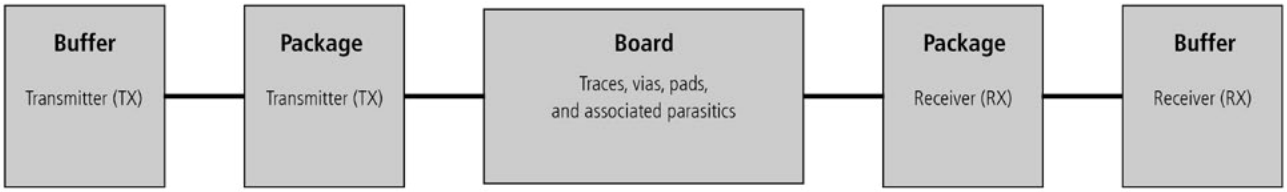
Failure to comply with DQ Mask specifications may be due to a number of factors; however, high slew rates are common for devices that incorporate Decision Feedback Equalization (DFE). Design changes that mitigate noise or EMI will likely be necessary to address DQ Mask compliance failures.

The techniques used to analyze data buses with DQ masks are very similar to the techniques required to analyze control and address buses with CA Masks for LPDDR.

DDR COMPLIANCE TESTING

TIMING: INTERCONNECT AND STROBE INTERCONNECT SKEW

The margin for error in DDR timing accuracy continues to shrink due to higher frequencies and faster transfer rates. Delays that previously seemed insignificant can result in system instability or misinterpretations that cause erroneous functionality.



For this reason, delays from interconnects and buffer/packages, as well as the resulting skews need to be analyzed for DDR compliance. To calculate the Interconnect Skew and Strobe Interconnect Skew, some initial measurements need to be determined:

BUFFER/PACKAGE DELAY

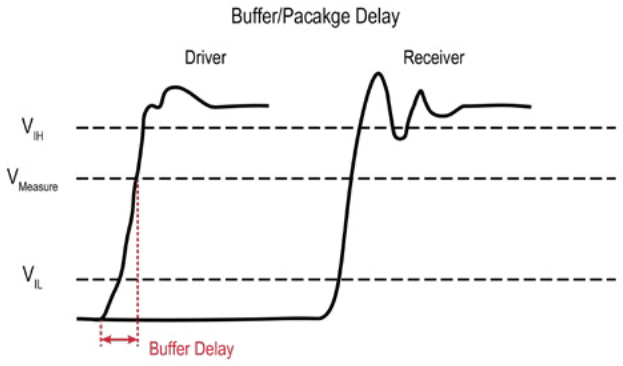
The Buffer delay is the delay of the transmitter IO model or the time from when the signal departs the die to when it arrives onto the die. The package delay is the time in which the signal transitions through the package.

WHY IS IT IMPORTANT?

For correct system functionality, no actions should be taken until after the buffer/package delay and all necessary bits have been sent and received.

HOW DO YOU MEASURE IT?

Connect the output buffer model, used for signal integrity analysis, to the T_{co} test load and simulate the design.



To calculate the delay, measure the distance or time from the beginning of the signal transmission to the point where the output pin crosses its threshold.

INTERCONNECT DELAY

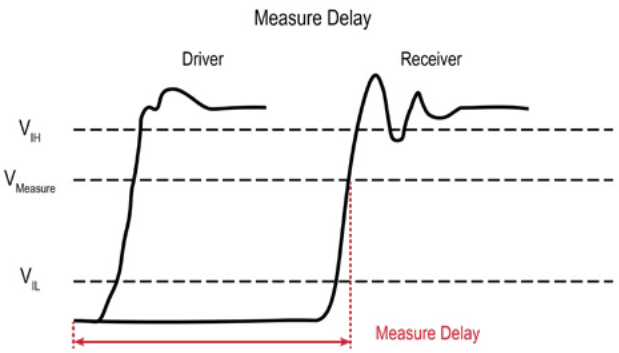
The interconnect delay is the delay in signal transmission due to the interconnects and the length of the traces between the transmitter and receiver in the system.

WHY IS IT IMPORTANT?

These issues typically have physical root causes related to skin effects, increased resistance, or line spacing and can result in system instability or signal misinterpretations.

HOW DO YOU MEASURE IT?

The interconnect delay should be measured for each net.



Measure the interconnect delay on the first cycle of the signal transmission through the following equation:

Interconnect Delay = MeasDelay - BufferDelay

Where MeasDelay is the time from 0 in the simulation to when the receiver waveform crosses the voltage threshold.

DDR COMPLIANCE TESTING

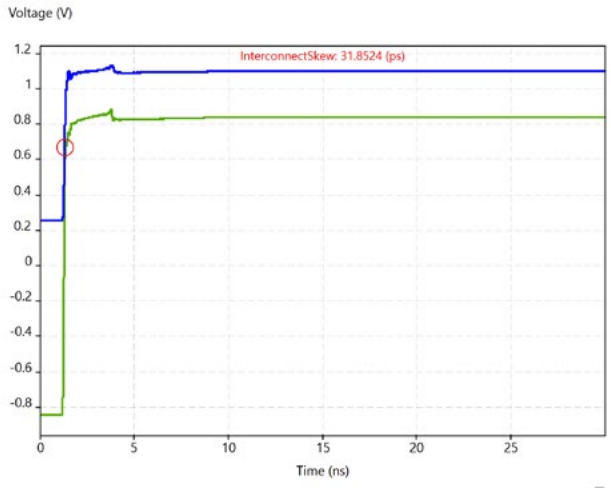
TIMING: INTERCONNECT AND STROBE INTERCONNECT SKEW

With the delays calculated, the Interconnect Skew and Strobe Interconnect Skew can be verified against JEDEC standards to ensure DDR compliance.

The buffer/package delay is saved and used in flight time computations for accurate interconnect skew calculations and signal integrity analysis.

INTERCONNECT SKEW

Interconnect Skew is the amount of delay that can be introduced by the interconnect while still meeting the timing requirements.



WHY IS IT IMPORTANT?

When completing the PCB layout and routing, additional interconnect skew is incorporated into the system. Analyzing the interconnect skew will allow you to determine how much skew can be introduced before timing requirements are impacted.

HOW DO YOU MEASURE IT?

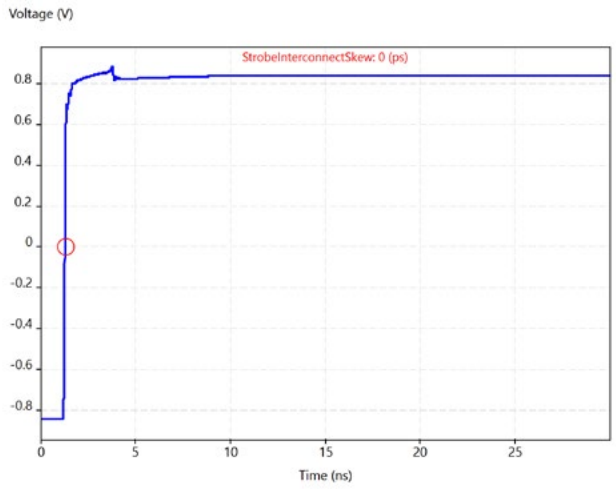
Interconnect Skew should be measured on each cycle and can be calculated with the following equation:

Interconnect Skew =

InterconnectDelay_Signal - InterconnectDelay_TimingRef

STROBE INTERCONNECT SKEW

The Strobe Interconnect Skew is the time between the strobe and clock signal transmissions.



WHY IS IT IMPORTANT?

Strobe is generated within the transmitter package and is a derivative of the clock. To achieve proper timing and data latching, the skew between the strobe and clock must be minimized.

HOW DO YOU MEASURE IT?

The Strobe Interconnect Skew should be measured on each cycle and can be calculated with the following equation:

Strobe Interconnect Skew =

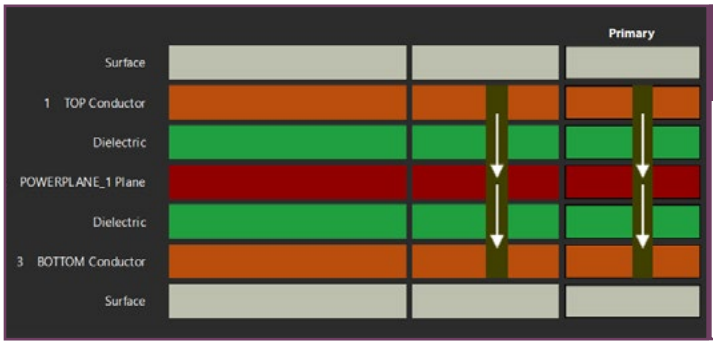
InterconnectDelay_Strobe - InterconnectDelay_Clock

The timing budget for DDR is relative to the data and associated strobe. While there isn't a defined acceptable value for interconnect skew and strobe interconnect skew, adding equal amounts of skew to the data and associated strobe will help preserve proper DDR functionality.

DDR DESIGN CHALLENGES

ADDITIONAL PCB DESIGN CONSIDERATIONS

Designing and building PCBAs where the memory will reliably meet the high-performance demands of processor-based systems can be daunting. When designing with DDR, additional consideration is required for:

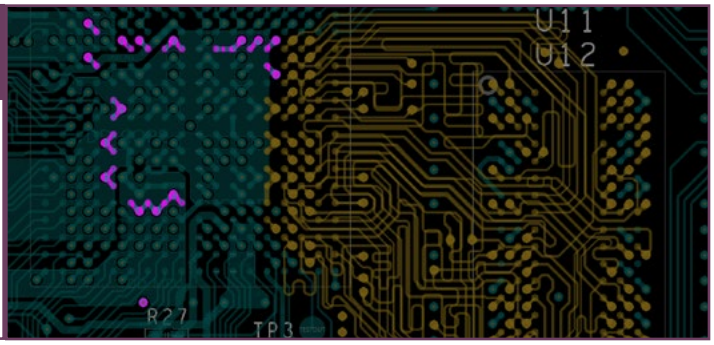


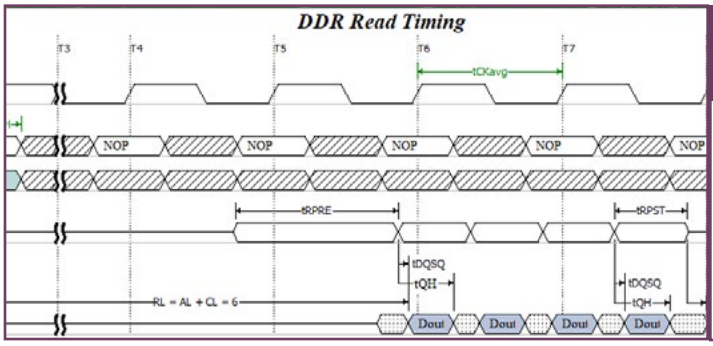
Physical and Material Constraints

Dielectric constant, copper weight, clearance requirements, and other physical/dimensional specifications affect DDR design.

PCB Layout Optimization

To achieve the level of performance expected for DDR and LPDDR implementation, your layout needs to be optimized. This means following best practices for component placement and trace routing that are guided by SI and PI considerations.





Timing and Synchronization

The popularity of DDR and LPDDR is due in large part to its double-data rate timing protocol. At higher frequencies, however, the margin for error in synchronization becomes much smaller. Therefore, timing alignment and transition times must be accurate to ensure reliable transmission and reception.

Due to these design complexities, it's imperative to accurately analyze DDR performance during the PCB layout to ensure functionality and compliance to JEDEC standards.

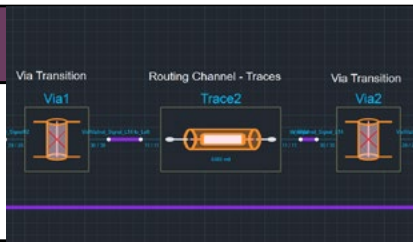
DDR DESIGN CHALLENGES

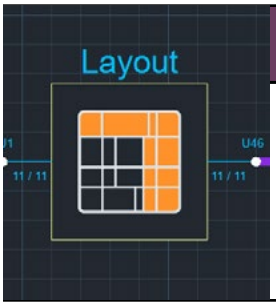
KEY SOFTWARE FEATURES FOR REALISTIC ANALYSIS

To accurately analyze DDR compliance, simulation software must include support for:

Pre and Post-Layout Analysis

Both pre-layout and post-layout analyses are critical to DDR design and compliance. Pre-layout capabilities allow you to define critical design constraints while post-layout analysis helps to identify and fix performance issues before production.



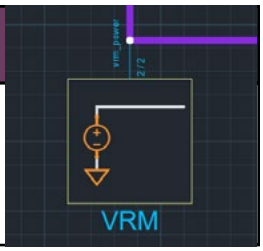


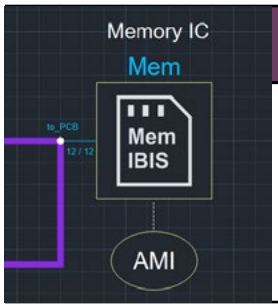
PCB Parasitics

With increasing transfer rates and decreasing timing margins, it is critical to accurately analyze the skew of the entire system. Often the IBIS models used in the simulation are just signal representations at the die of the device. To accurately analyze the entire system skew, IBIS models, the extracted board parasitics (or the interconnect delay from the board), and package models should be incorporated into the simulation.

Power-Aware Design

With faster switching speeds, it's imperative to create a robust and responsive power-delivery network. Power-aware simulation is required for DDR and becomes even more critical for low-power, LPDDR devices.



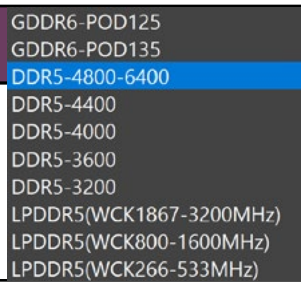


AMI Models

DDR devices incorporate decision feedback equalization and other non-LTI (linear and time-invariant) effects. These can be realistic simulated with Algorithmic Modeling Interface (AMI) models which allow you to incorporate the necessary internal component and connectivity information to perform statistical simulation based on the channel pulse response or time-domain simulation.

Integrated Compliance Standards

Verifying DDR performance against the corresponding JEDEC specifications can be time consuming and often includes researching the required values, performing various measurements, and comparing the results. Integrating compliance standards within your simulation software easily outlines the measurements and results required.



Incorporating a simulation and analysis tool with these features will help achieve first-pass compliance success.

DDR COMPLIANCE VERIFICATION
WITH SIGRITY

The best means of verifying your design is to employ a proven EDA software solution specifically designed for DDR compliance testing. Sigrity, which is well known for its SI interface verification capabilities, includes a compliance testing kit for DDR interfaces.

Sigrity provides kits specifically developed to help achieve DDR compliance by:

- Performing all essential tests for DDR compliance
- Automatically analyzing simulation results against JEDEC specified values including support for:
  - DDR
  - LPDDR
  - GDDR
- Providing easy to read pass/fail results
- Automatically generating reports
- Providing seamless integration with other software design and analysis tools

To learn more go to:

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EMA Design Automation is a leading provider of the resources that engineers rely on to accelerate innovation. We provide solutions that include PCB design and analysis packages, custom integration software, and engineering expertise, which enable you to create more efficiently. Learn more about verifying compliance for other devices in your PCB designs with our e-books and whitepapers.