DDR PCB LAYOUT GUIDELINES:

AVOIDING COMMON MEMORY ISSUES WITH YOUR BOARD LAYOUT

EMA Design Automation®

DDR PCB LAYOUT GUIDELINES

AVOIDING COMMON MEMORY ISSUES WITH YOUR BOARD LAYOUT

DDR is the preferred memory type for commercial, industrial, and critical industry electronics devices that require internal onboard data processing. Designing error-free PCB layouts that include these devices can be challenging. Countless redesigns, extended development times, and unnecessary costs are all possible.

This eBook discusses how to ensure your DDR circuit board implementation adheres to applicable standards and satisfies constraints. This includes software verification tools to ensure your design is first-pass manufacturable for the popular DDR4 and the latest evolution, DDR5.

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A BRIEF HISTORY OF DDR

A QUICK TRIP DOWN MEMORY LANE

The ever-increasing demand for smaller, faster, and smarter electronics in recent decades has resulted in onboard processing capability becoming a basic requirement for many PCBA designs. To meet performance objectives for processors and controllers, reliable random access memory (RAM) is essential. This can be achieved through the following:

- Static random access memory (SRAM)
- Synchronous dynamic random access memory (SDRAM)
- Asynchronous dynamic random access memory (DRAM)
- Double data rate (DDR)

Definition of DDR: DDR stands for double-data-rate, which refers to how TX/RX data is synced with both the rising and falling edges of the source clock signal. This feature allows for double the rate of data transmission per clock cycle.

DRAM used to be the standard for data transmission; however, this method needed more uniformity and constant speed and was ill-suited for faster processors being developed. This has led to DDR being the preferred protocol for memory devices. DDR revolutionized memory data transmission for speed, density, size, voltage, column access strobe (CAS) latency, and other specifications. These technological advances have continued throughout the evolutions of DDR.

Feature	DDR	DDR2	DDR3	DDR4	DDR5
Year Released	2000	2003	2007	2014	2019
Transfer Rate	200-400 Mbs	400-800 Mbs	800-1600 Mbs	1.6-3.2 Gbs	3.2-6.4 Gbs
Densities	128Mb-1Gb	256Mb-4Gb	512Mb-8Gb	2Gb-16Gb	8Gb-64Gb
Prefetch Width	2n	4n	8n	8n	8n/16n
Clock Type	Differential	Differential	Differential	Differential	Differential
Strobe Type	Single	Single/Diff	Differential	Differential	Differential
Supply Voltage	2.5V/2.6V	1.8V	1.35V/1.5V	1.2V/2.5V	1.1V
Interface Tech	SSTL-2	SSTL-18	SSTL-15	POD	POD
CAS Latency	2-3 clocks	3-5 clocks	5-10 clocks	10-15 clocks	
ODT	No	Yes	Yes	Yes-Dynamic	Yes

DDR3, which was introduced in 2007, remained the most used DDR DRAM until being surpassed by DDR4 in 2017.

BREAKING DOWN DDR4

SMALLER, FASTER, LOWER POWER

Currently, DDR4 is the most common type of memory used in desktops, laptops, PDAs, and gaming systems. This RAM technology is the culmination of four generations of enhancements, and distinct advantages justify its implementation compared with former versions.

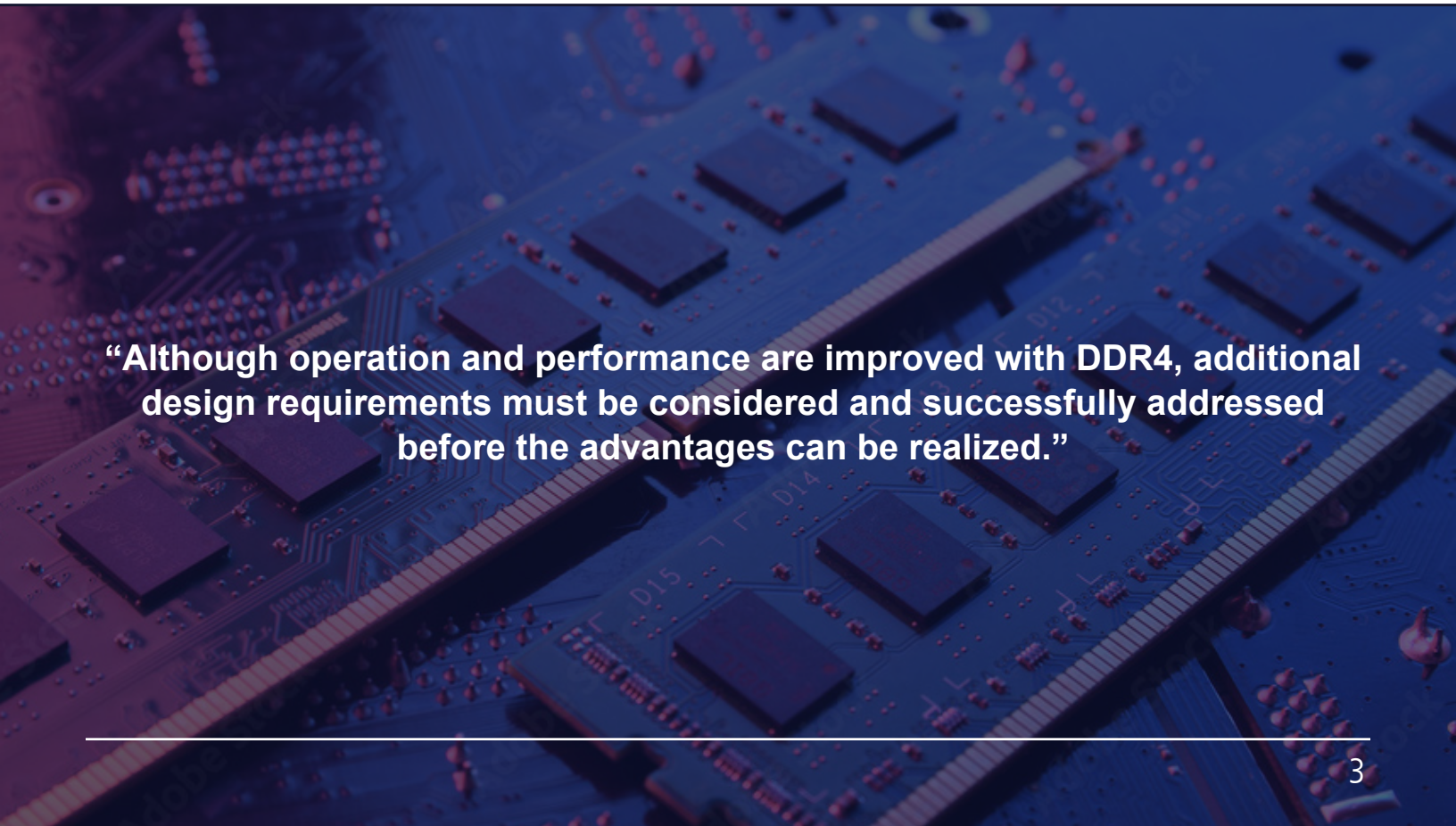
DDR4 Performance Enhancements

Transfer Rate
The data transfer rate doubled from 1.6 to 3.2 Gbs.

IC Density
Memory module density increased from 8 to 16 Gb.

Power
Power consumption requirements reduced by 10%.

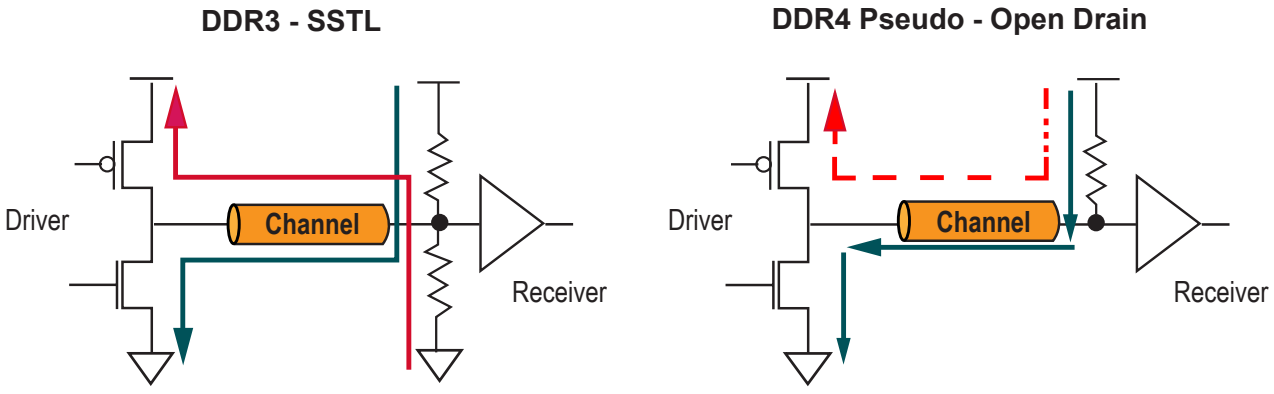
Due to these performance improvements, DDR4 technology required operational changes. The most impactful modifications that occurred with the transition to DDR4 are Pseudo Open Drain or POD I/O Technology and Data Bus Inversion or DBI control.



“Although operation and performance are improved with DDR4, additional design requirements must be considered and successfully addressed before the advantages can be realized.”

BREAKING DOWN DDR4
POD TECHNOLOGY

POD Technology



Pseudo-open drain (POD) is a signaling method where the current required for driving a signal high is eliminated, resulting in less power consumption. This switch from the previously used series-stub terminated logic or SSTL, where both drive and termination currents were required for driving a signal high, was motivated by the need to improve power efficiency in DDR modules. Faster or more frequent signals coupled with higher density place a higher premium on minimizing power consumption. POD technology contributes significantly to solving this issue by eliminating the need for current when driving signals are high and has several advantages.

Advantages of POD Technology

- Reduces switching current for I/O control.
- Enables more compact IC sizing options.
- Helps improve energy efficiency.

Along with the above advantages, the switch to POD technology allows the implementation of Data Bus Inversion Control (DBI).

BREAKING DOWN DDR4

DBI CONTROL

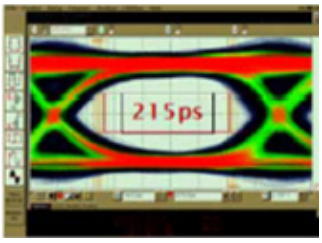
Data Bus Inversion (DBI) control inverts a bus when more than 4 bits of a byte lane are low to reduce the transferring and switching of zeros then reinverts the bus before bringing it into the memory array.

DBI Control

	Controller				Data Bus				Memory			
DQ0	0	1	0	0	1	1	0	1	0	1	0	0
DQ1	1	1	0	0	0	1	0	1	1	1	0	0
DQ2	0	0	0	0	1	0	0	1	0	0	0	0
DQ3	0	1	1	0	1	1	1	1	0	1	1	0
DQ4	0	1	0	0	1	1	0	1	0	1	0	0
DQ5	1	0	1	0	0	0	1	1	1	0	1	0
DQ6	1	1	1	0	0	1	1	1	1	1	1	0
DQ7	0	0	1	0	1	0	1	1	0	0	1	0
DBI_n					0	1	1	0				
Number of low bits	5	3	4	8	4	3	4	1				

NO DBI

Minimum zeros DBI



This process of determining whether to store the actual or inverted bits to minimize the number of 0s, reduces the power requirements as high bits do not require current. Combined with POD, this technique provides additional advantages to DDR design including:

- Less power usage
- Lower noise
- Cleaner data eye

POD and DBI are not the only improvements that come with implementing DDR4. For example:

On-Die Termination (ODT)

A new PARK mode was added to the dynamic on-die termination or ODT protocol, resulting in better EMI or noise suppression.

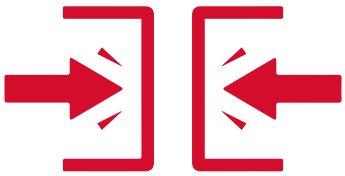
Cyclic Redundancy Cycle (CRC)

Cyclic redundancy cycle or CRC checking is also included, which has a 100% success rate in identifying random single-bit, double-bit, odd count and multi-bit, and unit interval or UI error detection.

Transitioning from DDR3 to DDR4 does cause an increase in column address strobe or CAS latency. However, the substantial processor and controller operational advantages gained from these enhancements, along with signal integrity (SI) improvements, more than justify the widespread implementation of DDR4, especially when high-speed memory access is necessary. Although operation and performance are improved with DDR4, additional design requirements must be considered and successfully addressed before the advantages can be realized.

WHAT ARE THE CHALLENGES OF IMPLEMENTING DDR?

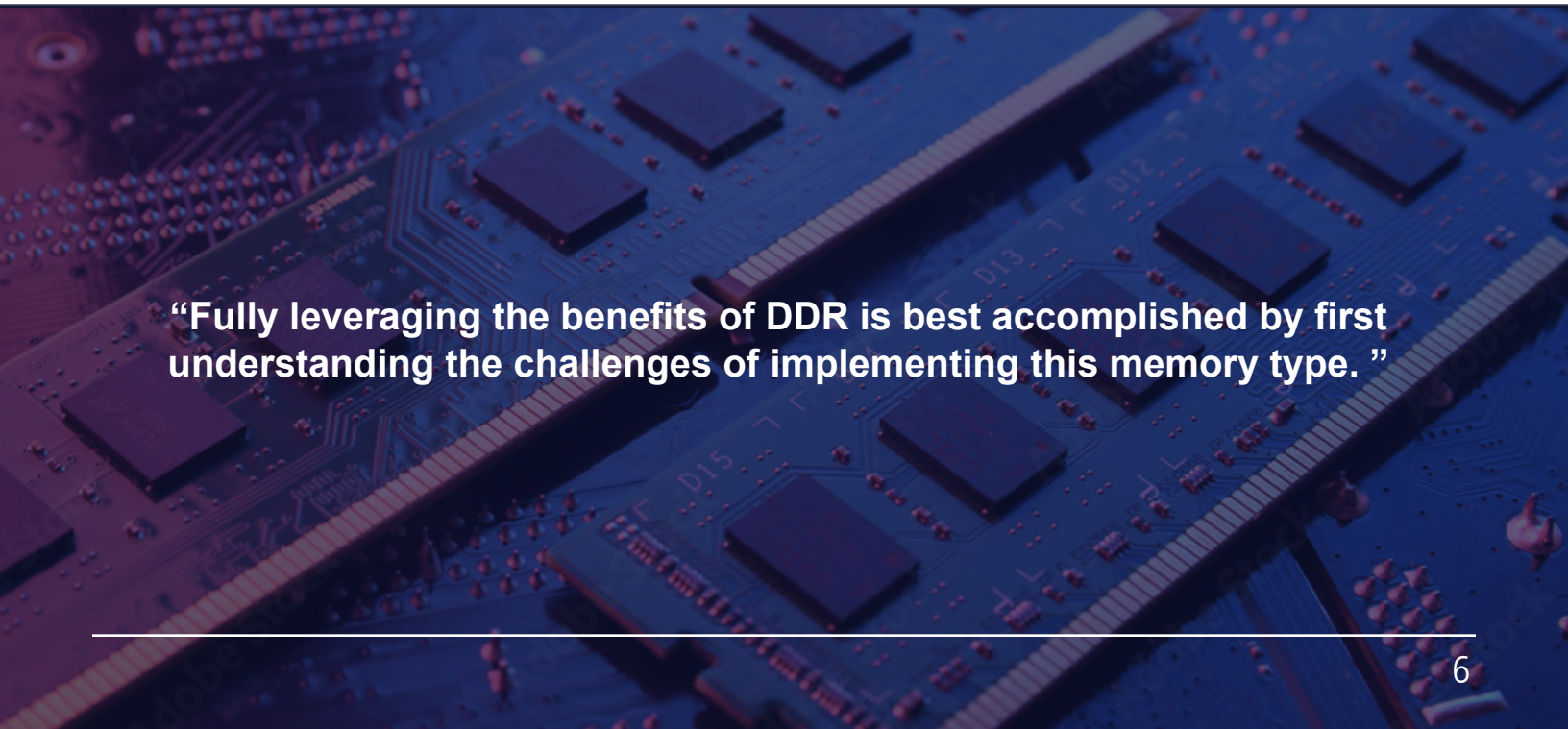
Fully leveraging the benefits of DDR is best accomplished by first understanding the challenges of implementing this memory type. First, designing with DDR is time-consuming, which can create a ripple effect that permeates throughout your development project. Increased redesign cycles and respins, whether to improve functionality and performance or adhere to compliance standards, drive up development costs. These issues are exacerbated with each progressively more complex version of DDR. Therefore, knowing and meeting the requirements for implementing DDR4 technology on your circuit board is essential. Common challenges to implementing DDR4 include:



Adhering to Constraints

Optimizing Component Placement

Achieving Proper Timing



“Fully leveraging the benefits of DDR is best accomplished by first understanding the challenges of implementing this memory type. ”

DESIGN CHALLENGE
ADHERING TO CONSTRAINTS

DDR4 are complex devices consisting of over 200 nets that require multiple rules to guarantee proper functionality. Although there is creative latitude, material and dimensional limitations restrict your PCBA layout design. Significant constraints that limit your design choices include:

- Dielectric constant(s) of selected materials
- Stackup organization
- Copper weights and thicknesses
- Spacing
- Clearance limitations

All of these affect impedance, signal flow fidelity, and transmission delays which are critical for DDR4 design.

Managing all the required rules for DDR4 nets can be complicated as all design constraints must be simultaneously adhered to. While utilizing a spreadsheet approach for constraint management is possible, this manual process is time-consuming and increases the possibility of errors. Your software solution method needs to be comprehensive with the best solution including a robust, easy-to-use, modifiable constraint manager as well as real-time feedback on constraint adherence.

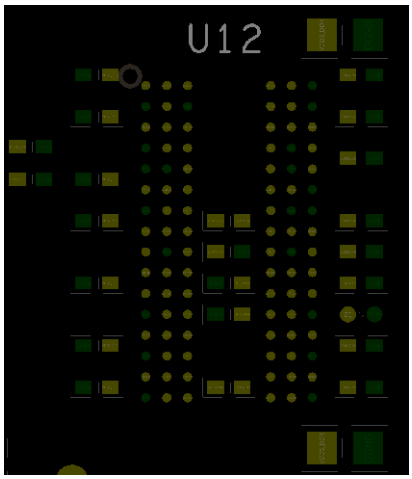
Tips for Adhering to DDR4 Constraints

- **Determine the board stackup in the beginning of the PCB Design**
  Changes to stackup will affect the impedance of critical traces.
- **Control trace impedances**
  For DDR4 to function as intended, single-ended traces should have a 50-60Ω impedance and differential pairs should have a 100-120Ω impedance.
- **Determine the minimum/maximum propagation delay as well as the relative propagation delays**
  This will ensure your clocks, data, and strobe signals arrive at the proper time.
- **Indicate routing layers to prevent crosstalk and noise**
- **Route interface signals between power/ground planes**
- **Reference device datasheets and standards to verify critical design requirements**
- **Control the via count and equalize the number of vias to help control impedances**

Note: Impedance requirements may differ between DDR versions. Make sure to verify values against DDR standards for your specific DDR device.

DESIGN CHALLENGE
OPTIMIZING COMPONENT PLACEMENT

Another significant design challenge is achieving the best component placement. This applies to primary DDR4 ICs, such as processing units and memory modules as well as decoupling and bypass capacitors for directing signals and blocking noise.



With DDR4, the need for less termination reduces routing requirements and makes additional space available on the PCB; however, designers can no longer just place components and hook them up. It is critical to know what the devices are as well as their function in the circuit to achieve first pass success with placement and routing.

Careful consideration should be given to component placement early in the PCB design process when change is easiest. Achieving an optimal component placement will simplify routing, improve signal quality, and ensure critical constraints, such as timing, can be met.

Note: Some software packages allow you to visualize and determine if timing constraints can be achieved based on the component location during placement.

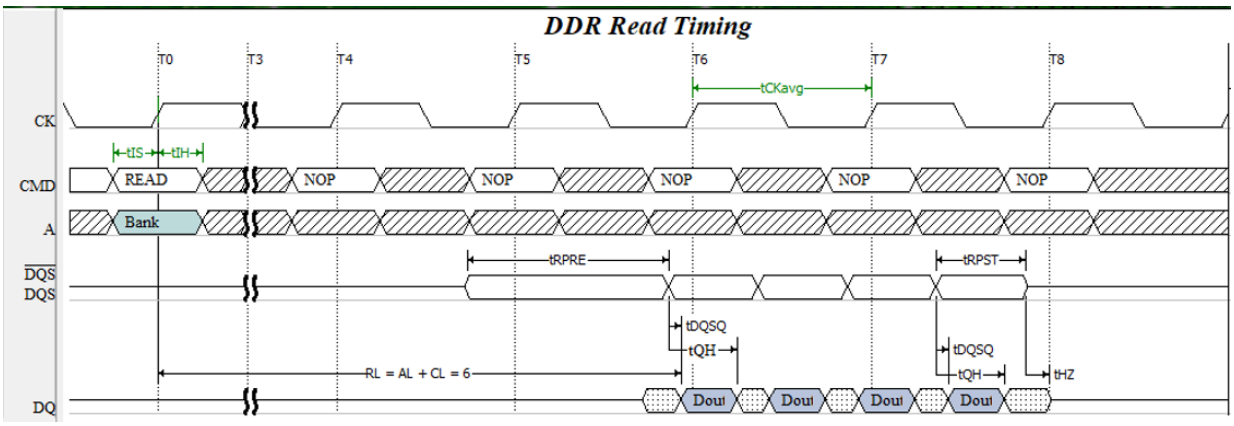
Tips for DDR4 Component Placement Optimization

- Place memory module as close to controller as possible
- Place decoupling capacitors as close to the IC as possible
- Minimize trace lengths
- Maintain constant spacing for differential routes
- Plan for pin fanout and/or escape
- Space memory chips at least 200mils apart
- Use a strategic pin and/or gate swapping to help achieve routing, timing, and placement objectives.
- Consider routing strategy during placement
- Ensure timing requirements can be met with component placement
- Replicate known-good circuit placement
- Color code nets for easier component placement and rotation

DESIGN CHALLENGE
ACHIEVING PROPER TIMING

Synchronizing nets and ensuring signals are presented when needed can be very hard to achieve. Achieving this proper timing becomes more difficult with each iteration of DDR due to:

- Faster switching speeds
- Larger amounts of storage
- Less margins



Depending on the DDR4 device selected for the design, there is anywhere from 64 to 128 bits of data. TThis data is divided into groups or byte lanes typically containing 8 bits of data. Each byte lane is then “latched” or captured via a strobe signal which is skewed a quarter cycle behind the data to allow it to stabilize. Once latched, the data needs to remain stable for a specified increment of time after the strobe has stabilized. With clock cycles around 1ns for DDR4, timing must be managed at every level of the design to ensure accuracy:

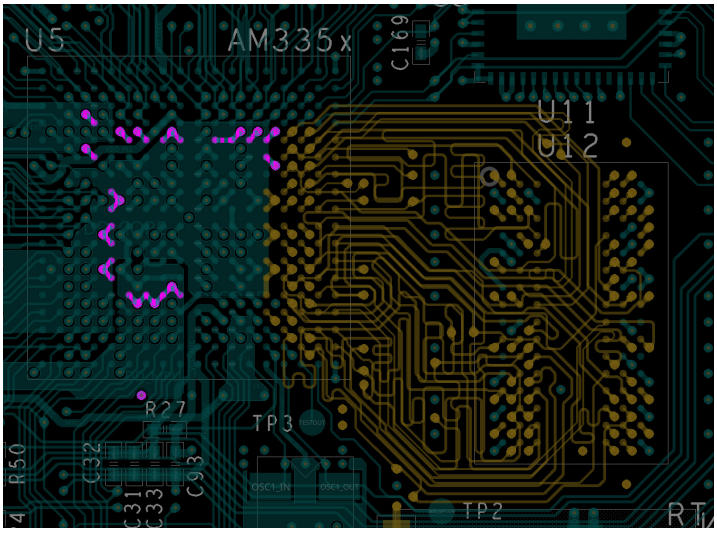
1. Timing must be consistent for all bit of a byte lane (typically 8 bits per byte lane)
2. Timing must be consistent for all byte lanes (approximately 8 byte lanes depending on the device)
3. Each strobe must be accurately timed with its corresponding byte lane

While DDR4 read/write leveling can help equalize timing, by measuring the delay at each DRAM and internally adjusting for differences up to 20 picoseconds, it is crucial that timing is taken into consideration during the PCB layout. Relying on the device datasheet alone will not ensure proper timing for complex DDR devices. Evaluating timing prior to layout with analysis software can help engineers visualize the timing of critical nets, analyze tight margins, and solidify more accurate constraints to guarantee proper timing can be achieved.

DESIGN CHALLENGE
ACHIEVING PROPER TIMING

Overcoming these timing challenges requires applying the best topology timing techniques and following good tips for signal TX/RX within memory modules and with controllers.

Often the goal of DDR4 design is to keep signals as short as possible; however, as complexity increases, this becomes difficult and may not be achievable. Since it is the relationship between signals that matters, adding delay is necessary to maintain those relationships. Implementing precise constraints based on verified timing analysis will help you know where to add propagation delay instead of trying to minimize it, which is most important to achieve the necessary DDR4 signal synchronization. Utilizing advanced functionality of PCB layout software can help ensure proper timing is achieved with color coded timing analysis, automatic trace tuning, and real-time feedback.



While DDR4 design must be guided by rules and strategies to produce an optimized layout which minimizes EMI issues and synchronizes signals, it is important that these good design practices are followed with a comprehensive analysis to verify proper functionality.

Tips for Achieving the Best DDR4 Timing

- Reference the device datasheet for the recommended timing
- Analyze timing for critical signals
- Tune critical signals, adding length to synchronize traces
- Match the length of data byte lanes to the strobe length (total propagation delay)
- Match the length of all bits in a byte lane (relative propagation delay)
- Avoid introducing vias and complex routing structures. This will add length and effect skew.
- Reduce unwanted signal noise
  - Don’t route across voids. This will create reflections and the byte will take longer to stabilize, increasing the delay before latching
  - Stay in close proximity to the reference plane from routing start to finish

Note: If incorporating vias, blind & buried vias are best but come with a higher price tag. Backdrilling may be a less expensive way to remove antennas.

HOW DO YOU VERIFY PROPER DDR INTERFACE OPERATION?

With the PCB layout completed (to the best of the designer's knowledge), you must perform SI and PI simulations on your board to ensure proper operation and adherence to performance objectives. However, DDR4 analysis presents a challenge due to:

- Faster clock speeds and increased data rates
- Decreased core and I/O voltages
- Increased impact of power noise
- Decreased noise budget
- Training cycles and auto-leveling to adjust propagation delay for each memory bank

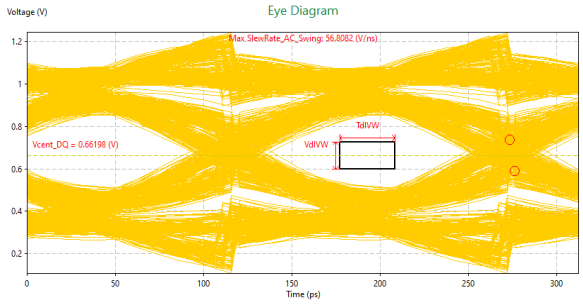
As a result of the decreased voltage and the ability to switch fast with a low impedance PDN, special consideration must be given to the impact of Simultaneous Switching Output (SSO) and Simultaneous Switching Noise (SSN) in the design, as there is a reduced margin for any noise on the system. Your interface operation verification tool must be able to accurately measure this metric to aid you in successfully addressing SSN issues that can greatly impact DDR operation.

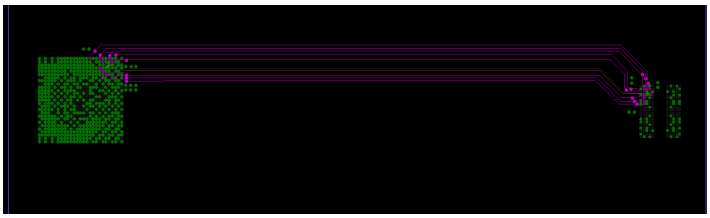
Impact of SSO/SSN on DDR4 PCBA Design

- **False triggers due to power/ground level changes (bounce)**
  The presence of ground bounce from SSN makes the detection of signal transitions difficult. Therefore, pins can be enabled/disabled erroneously.
- **Reduced time margins due to SSO-induced skew**
  When signal arrival times exceed the time margin or skew occurs, which can be caused by SSN at the output port, transmission errors happen that can have disastrous effects on circuit operations.
- **Reduced voltage margin due to power/ground noise**
  Noise on power/ground lines can shrink voltage margins resulting in false triggers, missed triggers and other signal misinterpretations.
- **Slew rate variations**
  Slew rate changes can cause a host of problems. These include erroneous signals and lack of signal transmissions.

HOW DO YOU VERIFY PROPER DDR INTERFACE OPERATION?

Achieving a high-quality design that takes full advantage of this evolution in memory capabilities must include advanced simulation and analysis to contend with the major enhancements.



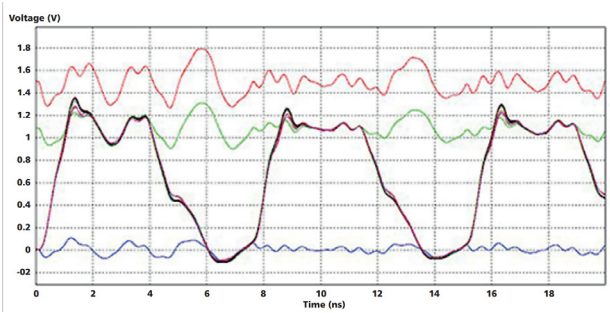


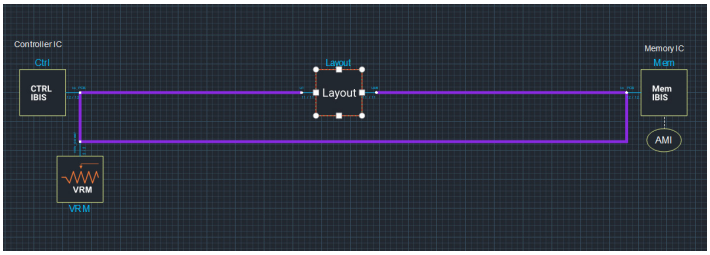
Accurate Simulation and Measurements

Faster speeds place more scrutiny on analysis resolution. Lower voltages make signal discrimination more acute and noise measurement more difficult. The ability to precisely measure parameters is required.

Serial Link Design Methodologies

Serial link design methodologies should be implemented to analyze DDR4 performance. This allows you to model each data bit as a discrete channel and use convolution algorithms offered by true channel simulators to send up to 100k bits down the in a short amount of time.





Power-Aware Signal Analysis

Noisy power will produce inconsistent wave transitions on data lines. Enabling DBI helps mitigate power noise. However, a simulation that includes power-aware analysis is needed to verify satisfactory performance levels and ensure SSN is lowered or well compensated for in the power delivery network.

Topology Environments

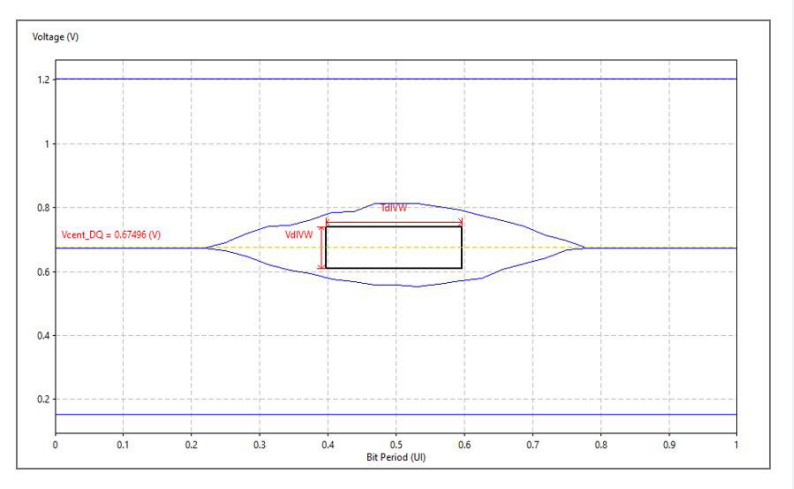
Due to the sheer amount of interconnectivity between devices, the need for a topology environment is crucial. A topology environment provides a clear view of system connections and understands the connectivity between devices. This approach is best for DDR4 as IBIS models, PCB parasitic models, and S-parameter models can be assigned for an accurate representation and the complete interaction can be analyzed.

HOW DO YOU VERIFY PROPER DDR INTERFACE OPERATION?

Utilizing an analysis software with the features outlined above will help analyze the interface operation between crucial elements in the design as well as the ensure adherence to JEDEC regulations and standards.

JEDEC uses bit error rate (BER) as a metric for signal quality or the degree to which noise, bit synchronization, or other interference errors affect data channel communication. For the DDR device to pass compliance, the following items should be analyzed and verified against the values outlined in the JEDEC specifications:

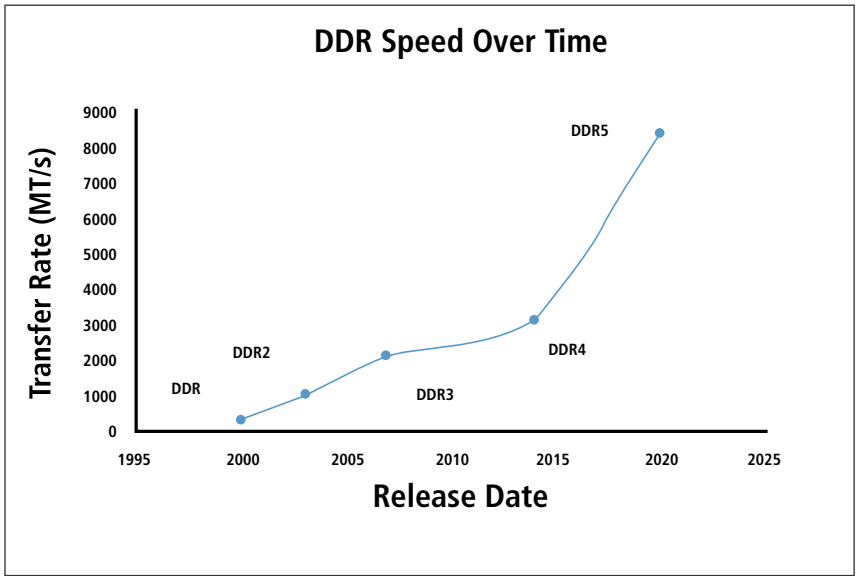
- **DQ Masks**
  - Jitter Margin
  - Noise Margin
  - DQ to DQS Skew
  - Skew Across All DQ
  - Slew Rates
- **Buffer/Package Delays**
- **Waveform Quality**
  - Overshoot
  - Undershoot
  - Ringback
- **BER Report**
  - Eye Width
  - Eye Height
- **Interconnect Delays**



While critical to the success of the design, producing a realistic simulation, researching the JEDEC requirements, and manually verifying compliance can be time-consuming. To save time without compromising accuracy, engineers should utilize a software that implements a power-aware analysis and pass/fail compliance reporting. This is especially important as complexity and speed of DDR devices continue to increase.

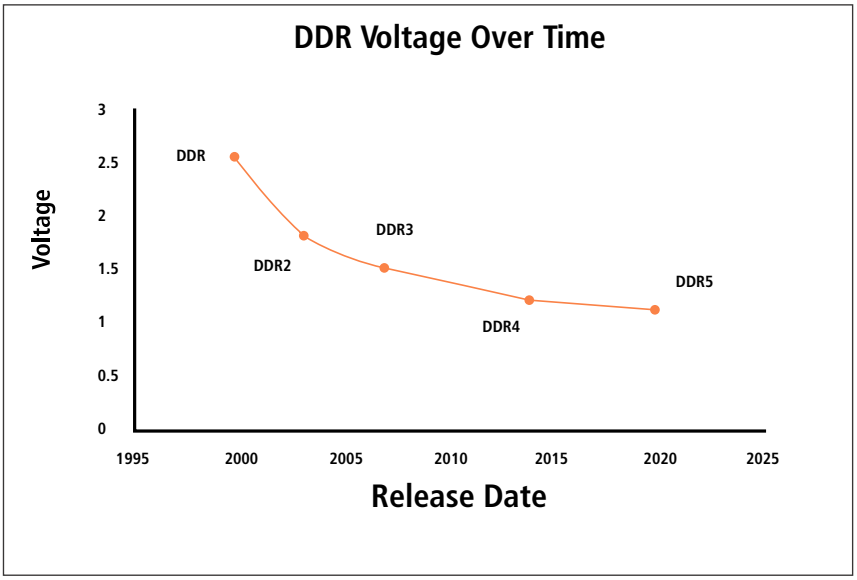
WHAT IS THE FUTURE OF DDR?

What is the future of DDR? Modern smartphones, smartwatches, and tablets all utilize LPDDR5 memory. Instead of the standard DDR variant, this new type of memory aims to keep power consumption as low as possible; however, bandwidth is sacrificed in the process. The introduction of DDR5 provides a good indication of what to expect for DDR and LPDDR evolutions:



The speed at which DDR devices transfer data has grown significantly since the release in 2000, with each iteration typically doubling the transfer rate. This graph shows the evolution of DDR speed overtime by displaying the megatransfers per second (MT/s) or millions of transfers per second for each DDR iteration.

The ongoing trend for all electronics and products to minimize power consumption can also be seen with the evolution of DDR. As seen with this graph comparing the required supply voltage for each DDR iteration, power requirements for DDR devices have decreased over 50% since the release of DDR.



WHAT IS THE FUTURE OF DDR?

As with previous evolutions, the data transfer rates doubled, density increased, and voltages decreased. These along with other upgrades and new features show the benefit of incorporating DDR5 into your cutting-edge designs:

Specified Impedance Requirements

The additional time spent calculating the required PDN impedance is eliminated, easing the AC PDN analysis. The provided PDN impedance for DDR5 is:

2-10 MHz: 10mΩ
20 MHz: 20mΩ

Benefits:

- Reduce time
- Reduce calculations required for PDN analysis

Inclusion of a PMIC on DIMM

With the incorporation of a Power Management IC (PMIC), voltage is generated directly on the DIMM. This eliminates the need for an additional connector.

Benefits:

- Improves IR drop for DC power integrity
- Reduces parasitic inductance
- Improves PDN impedance

Internal VREF for CA Bus

VREFCA is now internally generated for the command/address bus and is identical to VREFDQ This eliminates the need for a VTT/VREF regulator.

Benefits:

- Fewer power planes
- Reduced layout requirements
- Reduced BOM requirements

Decision Feedback Equalization (DFE)

DFE provides a high frequency boost which compensates for dispersive, frequency-dependent, channel loss. DFE removes scaled interference from four previous bits based on the channel impulse response. With DFE there is no amplification of noise but no pre-cursor equalization.

Benefits:

- Equalizes DQ signals
- Reduces effects of inter-symbol interference

Generic Command/Address (CA) Bus

Specific pins are no longer used and the command/address lines use a generic bus (CA[0…13]). If using a DIMM, fewer CA pins means more ground pins can be incorporated on the connector.

Benefits:

- Easier schematic capture
- Improve return path
- Improve signal quality

Note: Inter-symbol interference increases as data rates increase. Reflections on the memory channels due to impedance discontinuities from packages, vias, and connectors, adds to the interference.

WHAT IS THE FUTURE OF DDR?

With the increased data rate, updated features, and DDR5 enhancements discussed above, simulation is a must to ensure DDR5 functionality and a successfully system. However, even though the package sizes and pinouts are similar and the basic architecture between DDR4 and DDR5 is unchanged, the advancements require an alternate approach to simulation and analysis. When transitioning from DDR4 to DDR5 it is important to consider the following:

1 Will the Power Delivery Network withstand faster switching speeds?

With even faster switching speeds, it's imperative to create a robust and responsive power-delivery network. Power-aware simulation, as seen with DDR4, becomes even more critical.

2 With DDR5 devices using DFE, how do you know it will work?

Extending traditional IBIS behavioral models with Algorithmic Modeling Interface (AMI) allows you to incorporate the necessary internal component and connectivity information to perform statistical simulation based on the channel pulse response or time-domain simulation. IBIS-AMI allows you to incorporate equalization and other non-LTI (linear and time-invariant) effects into the analysis and simulate ultra-low bit error rates using statistical simulation.

3 Will the design comply to JEDEC Standards?

With tight margins and time-to-market deadlines, it's important to analyze compliance before production. Verifying the design performance against JEDEC specifications will increase the likelihood of passing compliance tests the first time.

4 How do you address compliance failures?

Failing a compliance test often results in design modifications or complete PCB redesigns which can derail the project budget and timeline. Finding and fixing common compliance issues with post-layout analysis will allow you to make any design modifications to guarantee compliance before production.

Each iteration of DDR brings faster speeds and new functionality which drive the need for effective CAD solutions. Incorporating IBIS-AMI models, power-aware signal integrity, pre-layout analysis, and post-layout analysis will help produce DDR-compliant PCBA designs.

PUTTING IT ALL TOGETHER

HOW TO IMPROVE DDR SIGNAL INTEGRITY DURING PCB DESIGN

The complexity of DDR memory continues to increase in order to provide the required reliable data transfer between components as computing, and other communication architectures evolve. Producing designs that satisfy performance objectives and facilitate efficient development requires robust tools for PCB layout as well as simulation and analysis.

PCB Design

The advanced functionality of OrCAD PCB Designer can help you achieve the required layout and timing for proper DDR operation:

- Interactive routing
- Automatic and interactive delay tuning
- Real-time design feedback
- Visual timing adherence feedback
- Advanced constraints
- Component placement assistance
- Placement replication
- Integrated impedance calculator incorporating stackup

SI, PI, & Compliance Analysis

Sigrity, the signal analysis flagship of Cadence's suite of PCB Design and Analysis programs, satisfies DDR-compliant design requirements with:

- Power-aware signal integrity
- IBIS-AMI support
- Incorporating topology and physical layout
- Providing a clear view of system connectivity
- Simulating for compliance
- Compliance reporting
- Troubleshooting and what-if scenario analyses

Timing Analysis

TimingDesigner provides engineers with a visual timing analysis to ensure proper functionality of critical DDR nets:

- Easy-to-use graphical interface
- Model timing constraints, cause and effect relationships, delays, and sequence protocols
- Identify worst case timing scenarios
- Analyze critical path timing and margins
- Communicate timing with efficient documentation

To learn more go to:

info@ema-eda.com

Get the Free Trial

GLOSSARY OF TERMS

CAS **Column Address Strobe** latency is the time delay between when the READ command is presented, the memory module receives the column address, and the column address strobe signal. Data is available to be read from memory.

CRC **Cyclic Redundancy Check** is a test instituted by JEDEC for DDR4 in 2015 to improve system reliability during memory READ and WRITE data transmissions.

DBI **Data Bus Inversion** is an optionally enabled feature for DDR4, where bits or their inversions are transmitted or stored depending upon the memory state (READ or WRITE) and operation mode.

IBIS-AMI **I/O Buffer Information Specification-Algorithm Modeling Interface** is an industry-standard that provides an interface model between EDA and simulation tools for statistical analysis and simulation.

ODT **On-die Termination** is a technological method where impedance-matching termination resistance is located on the memory chip instead of near the processor (e.g., motherboard). This helps minimize reflections from the memory module onto the signal line.

POD **Pseudo-Open Drain** is a signaling method instituted in DDR4 where the current required for driving a signal high is eliminated, resulting in less power consumption.

SSN **Simultaneous Switching Noise**, or ground bounce, is when the device's ground potential is raised as a result of multiple switching activities occurring simultaneously.

SSTL **Series Stub Terminated Logic** is the interface signaling method used through DDR3, where both a drive and termination currents were required for driving a signal high.

UI **Unit Interval** is a dimensionless measurement of the time between signal events. For example, the time between successive clock signals.

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