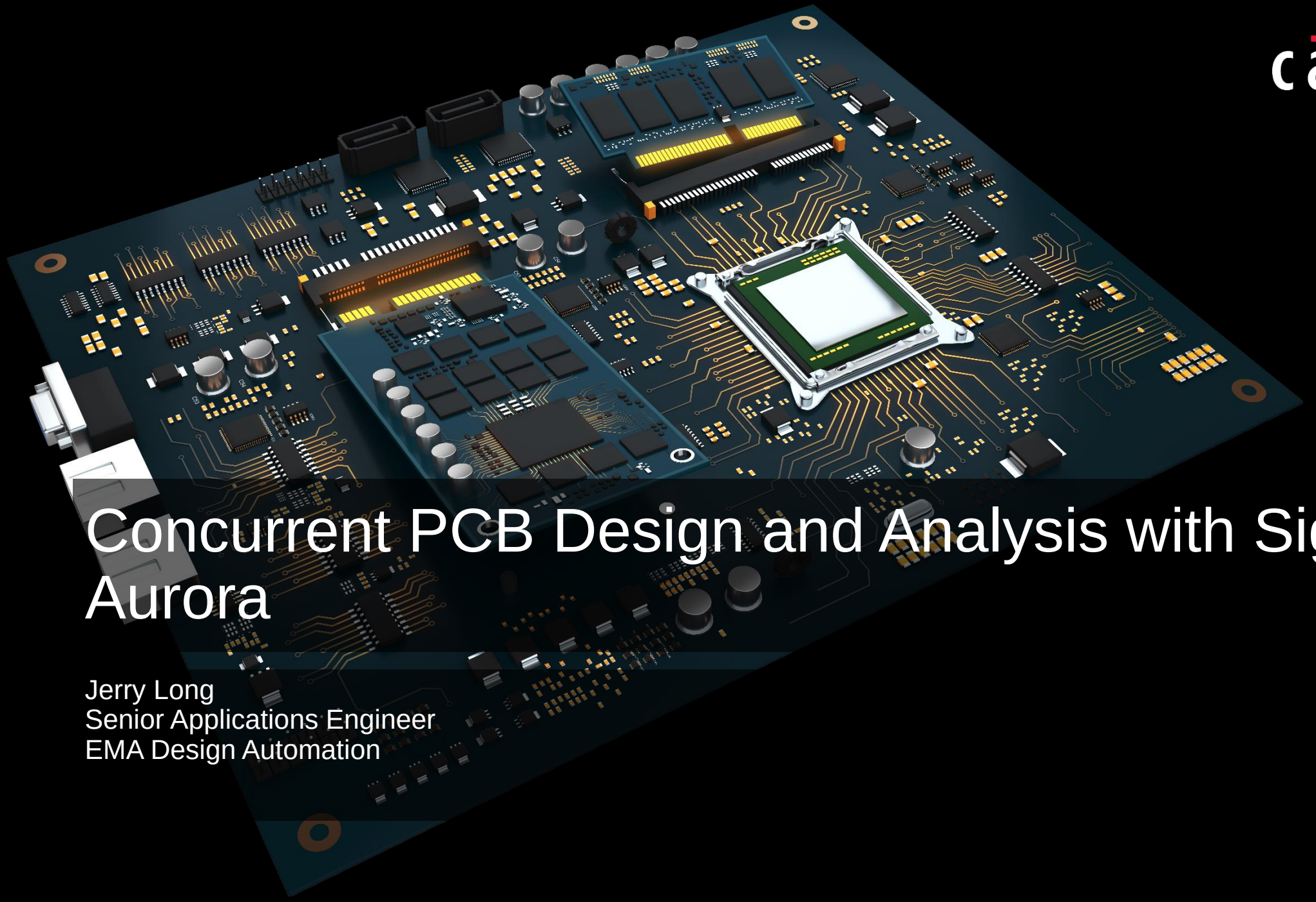

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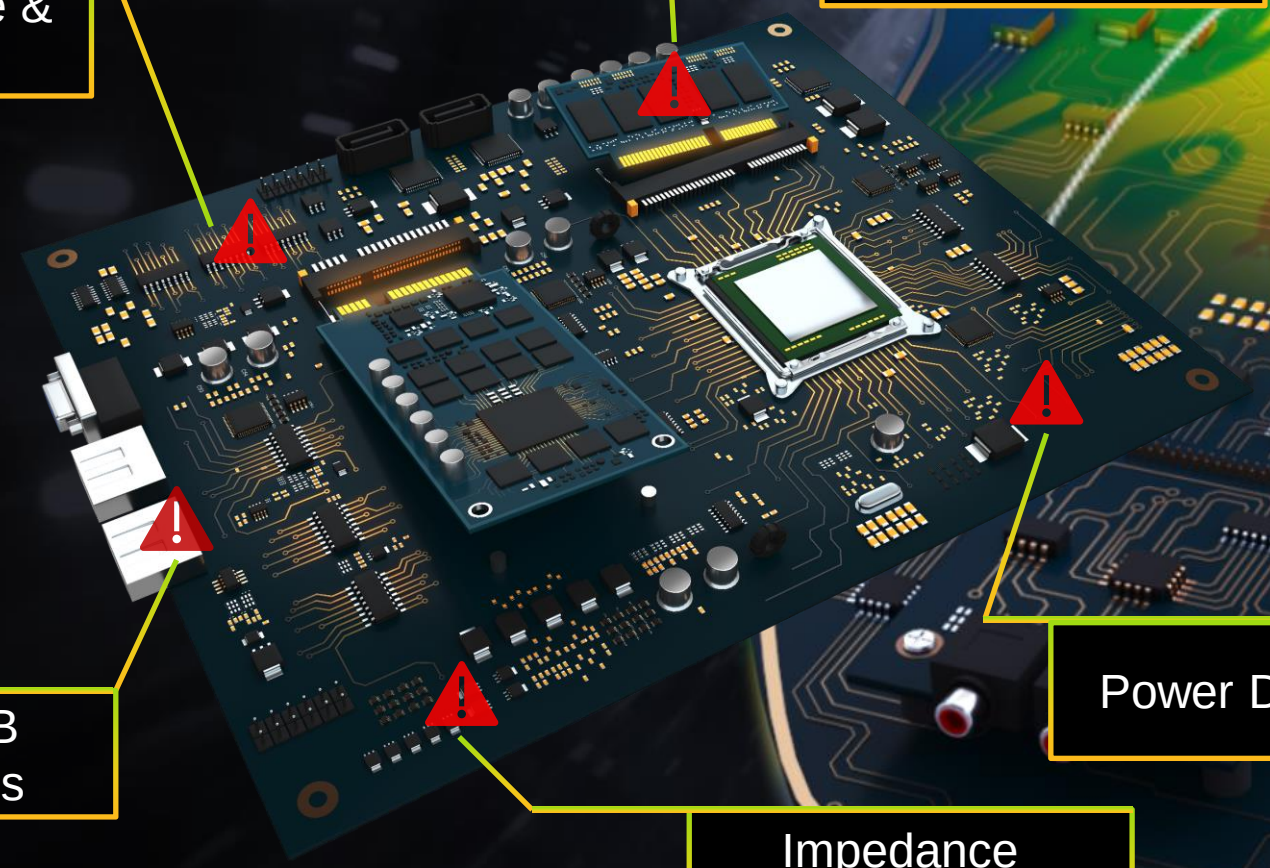
Concurrent PCB Design and Analysis with Sigrity Aurora

Jerry Long
Senior Applications Engineer
EMA Design Automation

EMA Design Automation®

Design Challenges

Modern Designs Present Series of Complex Electrical Challenges



Resonance & EMI

Return Path Discontinuities

Multi-GB Interfaces

Power Delivery

Impedance Discontinuities

Which If Not Caught Lead to

- Missed Schedules
- Re-Spins
- Field Failures
- Increased Costs

And these issues are often relational one affecting the other

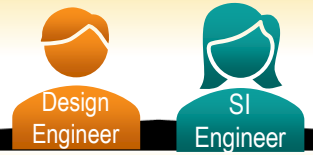
EMA Design Automation®

The Allegro Constraint-Driven Flow (Powered by Sigrity Technology)

Explore | **Design** | **Verify**

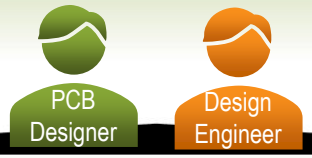
Conception — **Constraint-Driven Signal Integrity Flow** — **Signoff**

Constraint Development



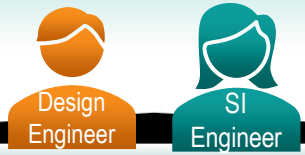
Sigrity™ Aurora (Virtual Prototype, Floorplan)

In-Design Analysis



Sigrity™ Aurora + Allegro / Constraint Manager

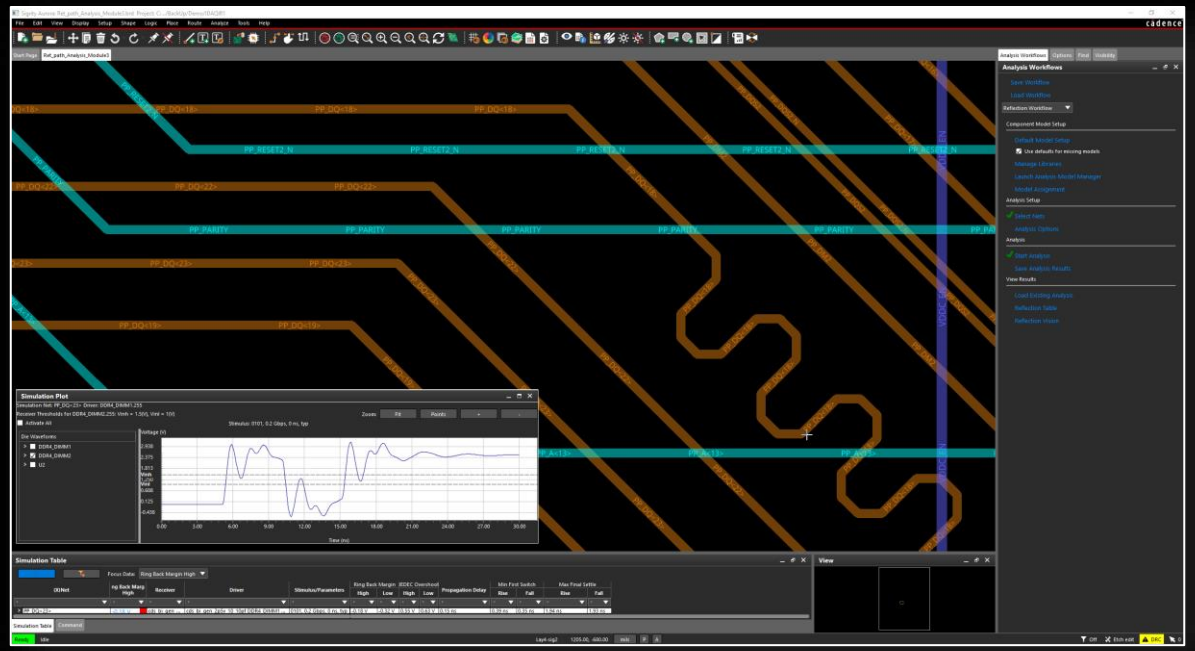
Full Board Analysis & Critical Interface Signoff

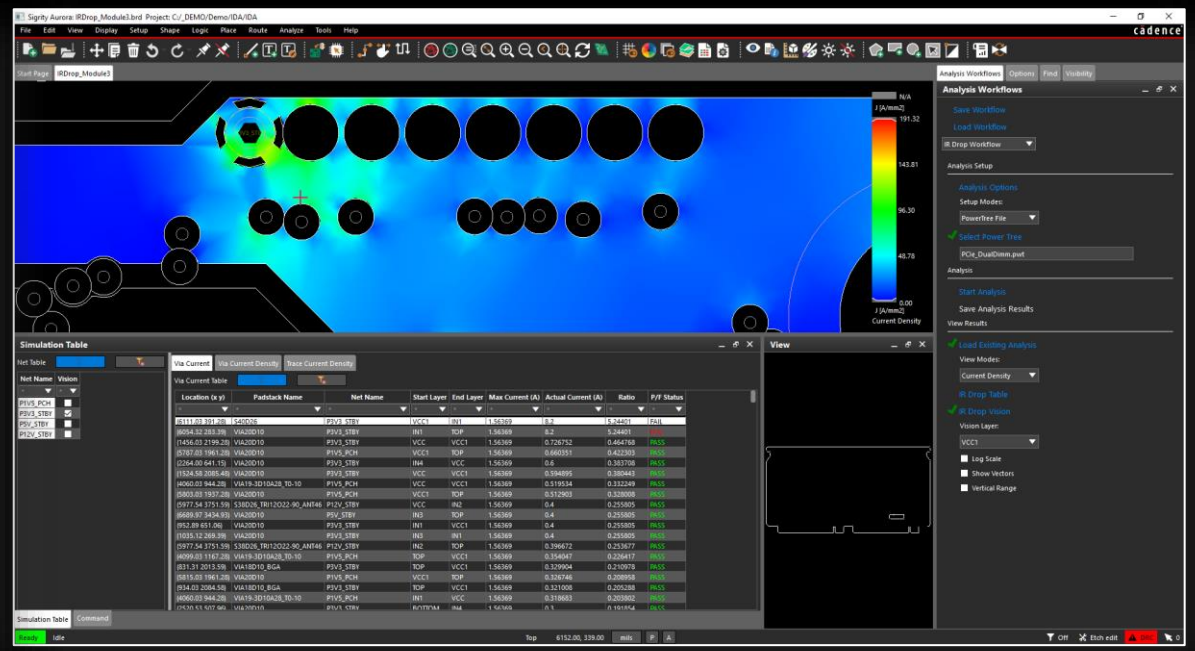


Sigrity™ Aurora + SystemSI ™

SI/PI - Aurora

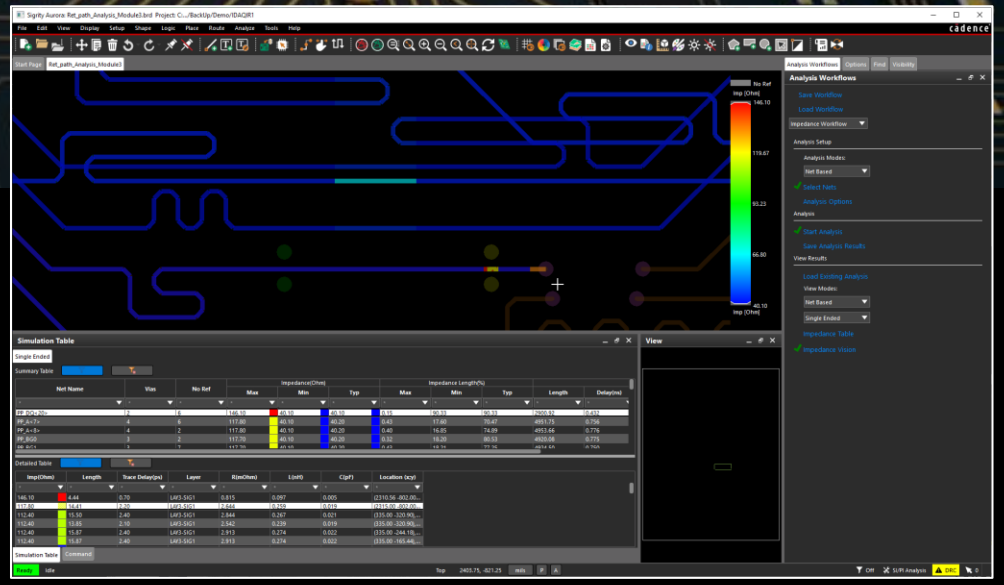
- Aurora provides basic signal and power integrity analysis, integrated directly into the Allegro front-to-back design environment. It enables SI and PI issues to be quickly identified and fixed in-design or Optimized idesign. Thus minimizing iterative analyze / fix / re-verify loops and reducing the overall design cycle.

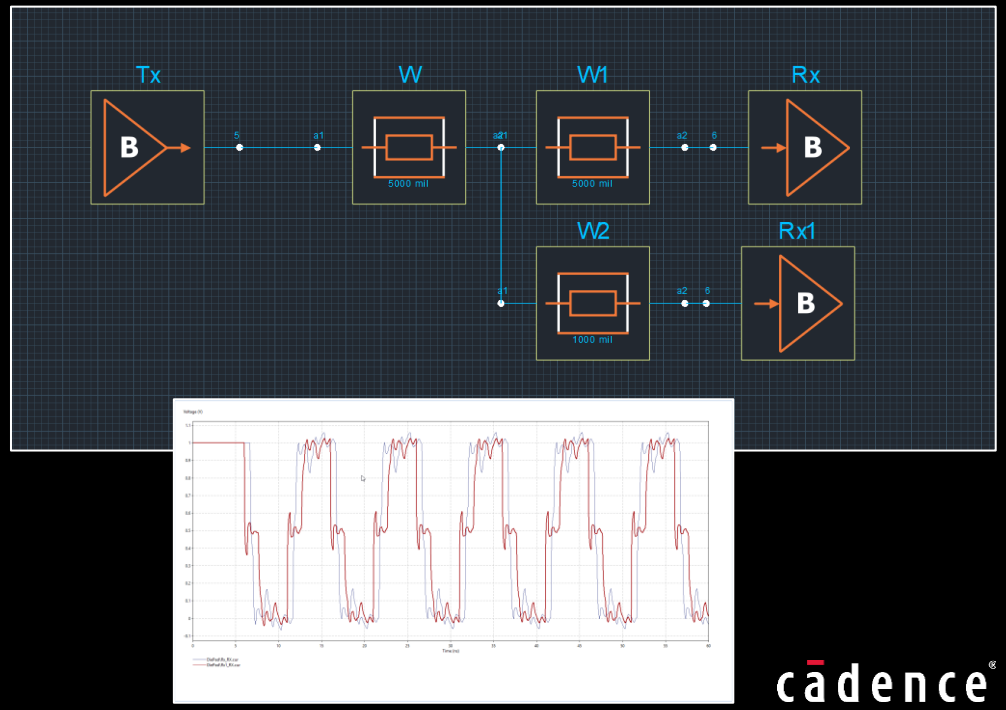




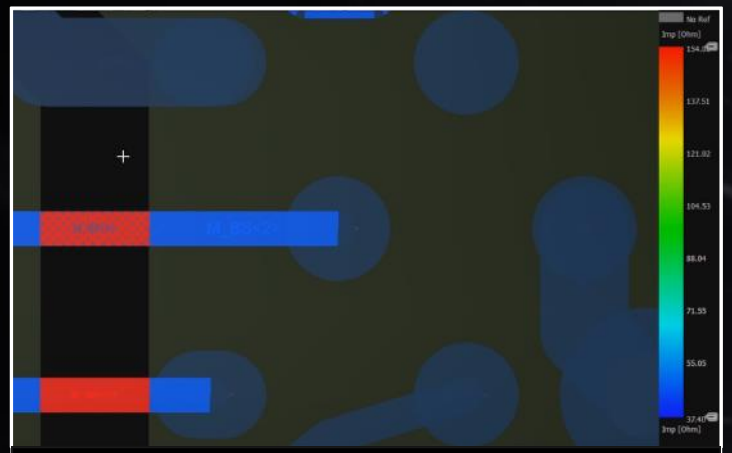
Aurora Primary Advantages

- Integration into the Allegro design flow with visions minimizes analysis / layout iterations and accelerates time-to-market
- Access to Sigrity analysis technology is brought to the design engineer and layout designer's desktop, making analysis results actionable with real-time design edits
- IR drop analysis by the non-expert, enabling real-time copper edits to address IR drop in-design
- Topology Explorer can be used pre-design to explore solution space and derive constraints to drive Allegro layout during exploration phase of the design
- Topology extraction can provide the electrical view of a signal topology for what-if analysis and troubleshooting

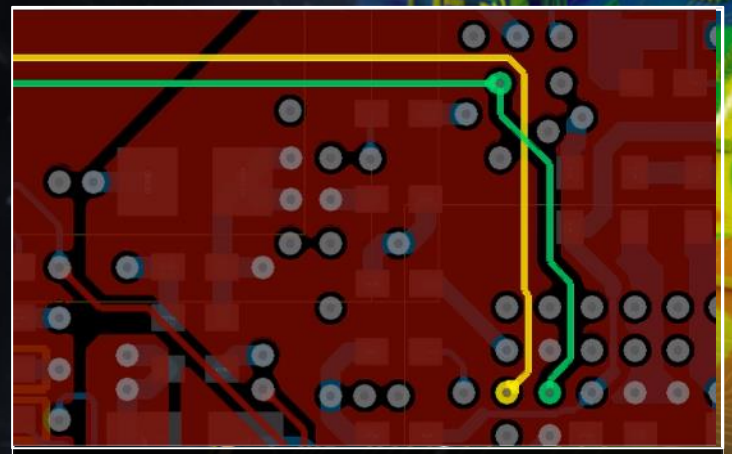




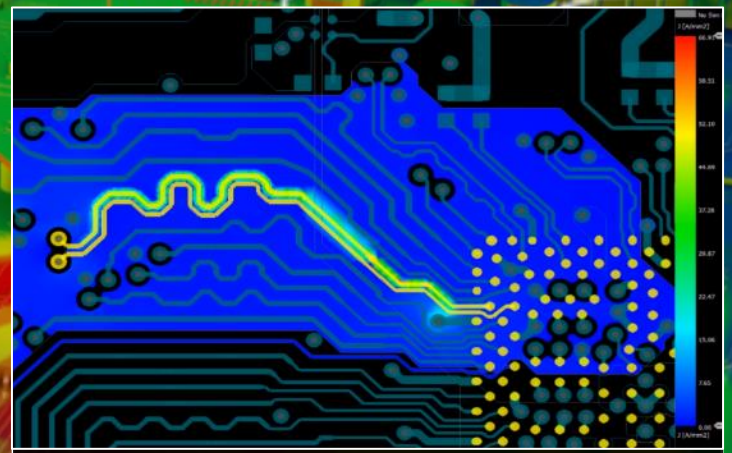
Aurora Analysis Workflows



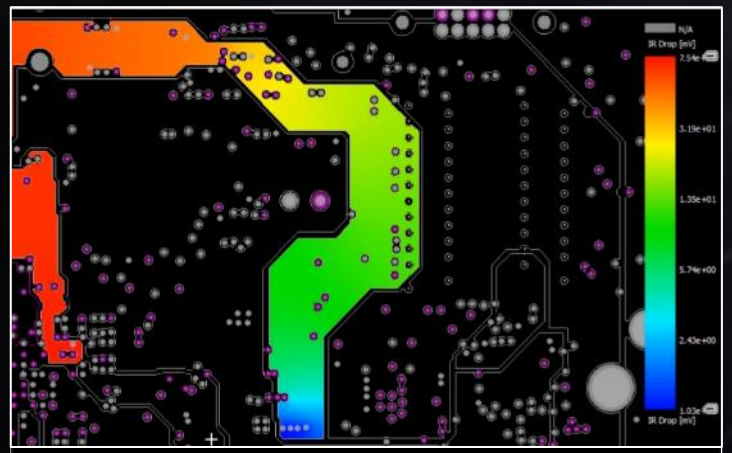
IMPEDANCE



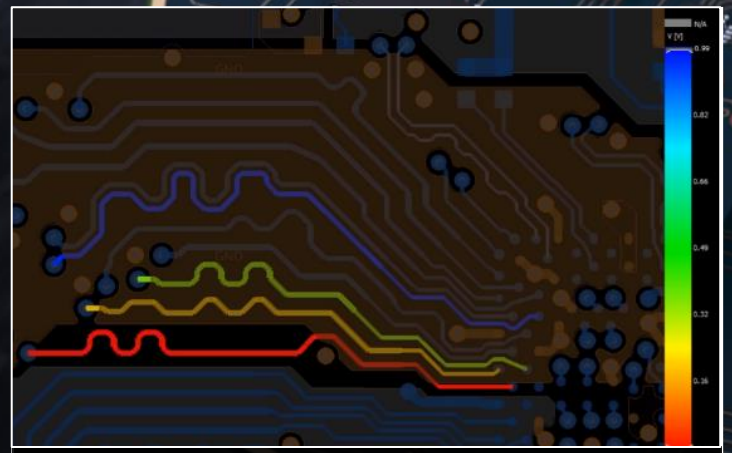
COUPLING



RETURN PATH

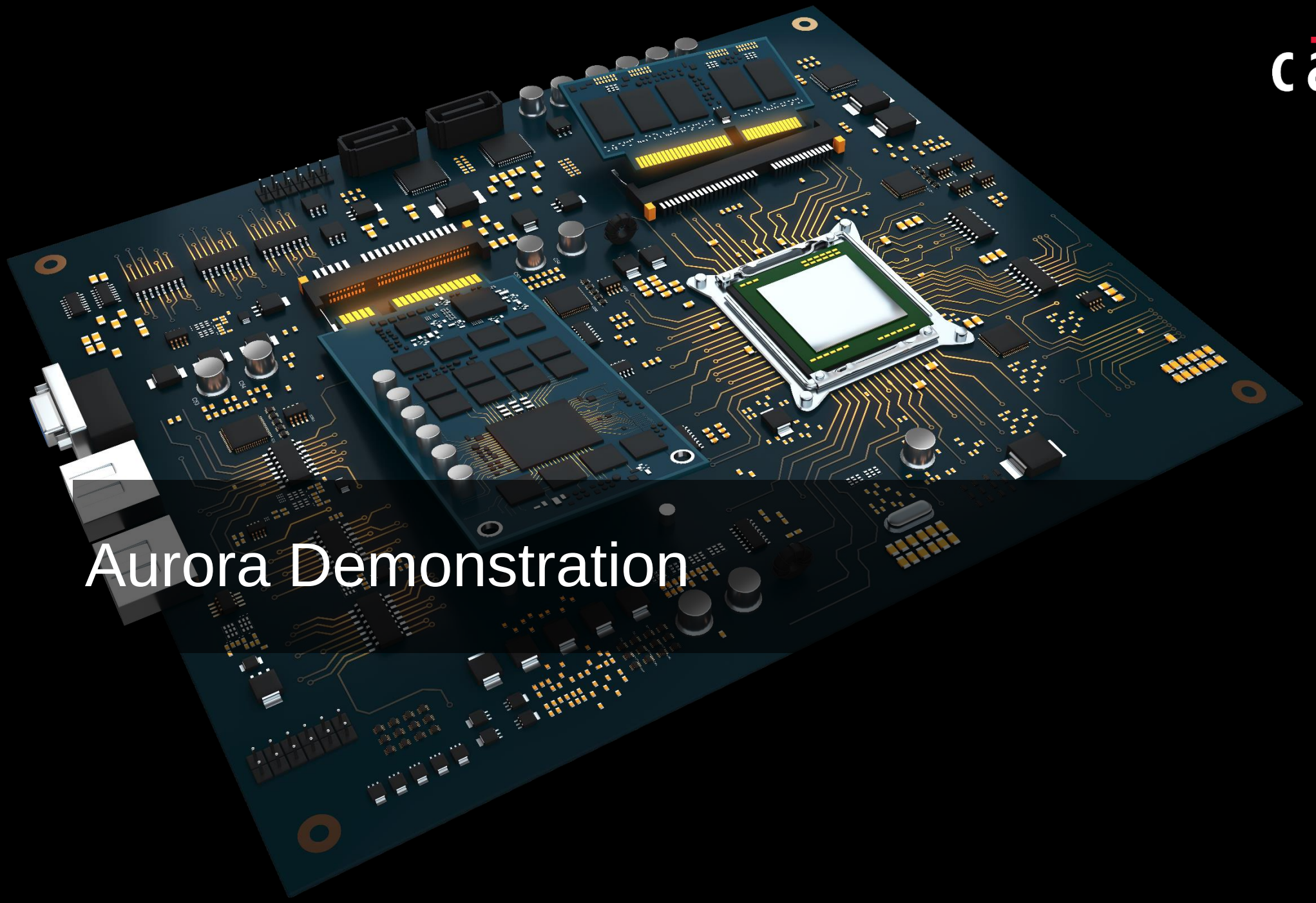


IR DROP



REFLECTION

CROSSTALK



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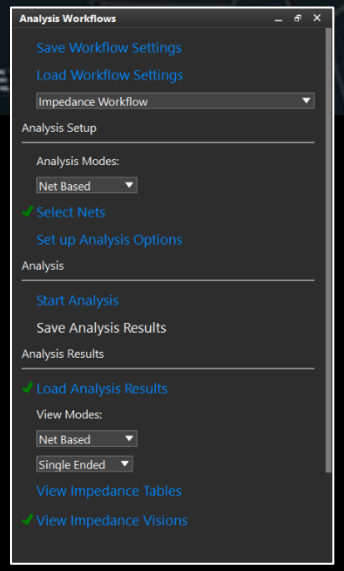
Aurora Demonstration

Impedance Workflow

1. Select the nets (or run the whole PCB) and run the analysis
2. Use the table to find the nets with the worst impedance discontinuities
3. Find problems, fix problems, and verify the solution directly on the Allegro design canvas

1



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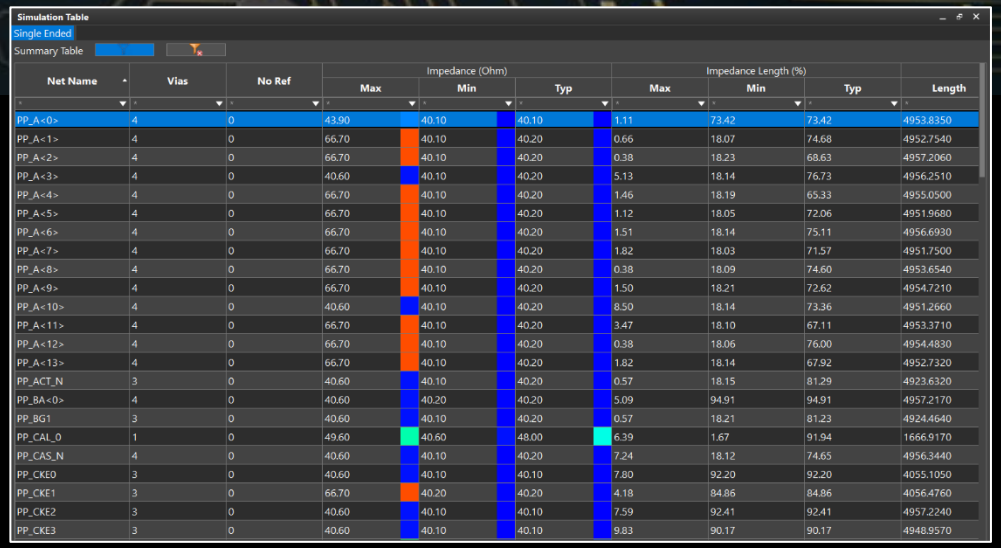
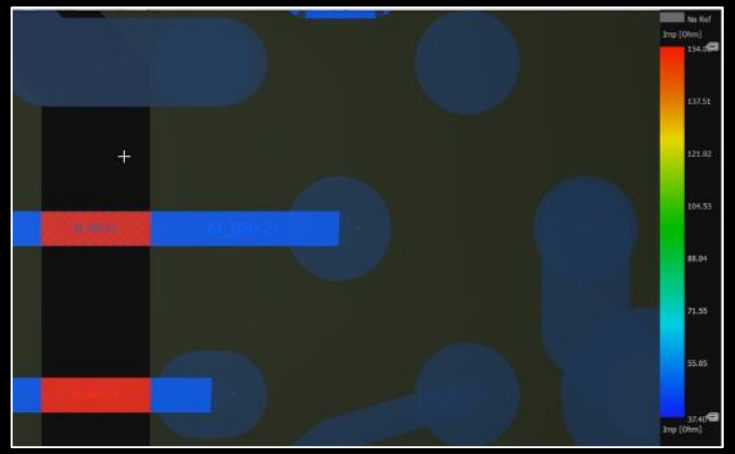
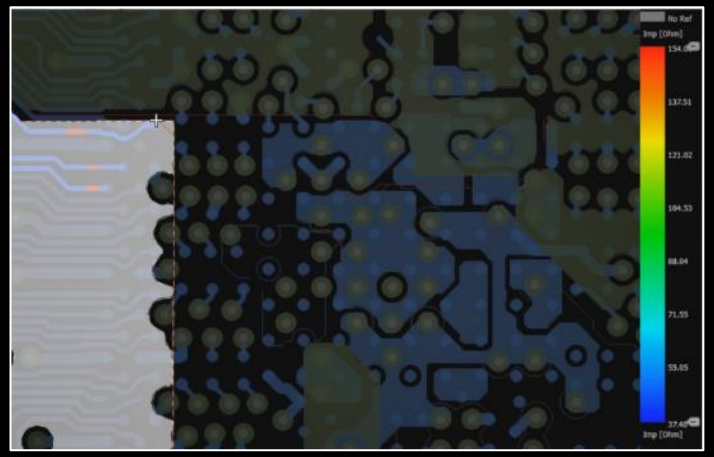


Net Name	Vias	No Ref	Impedance (Ohm) Max	Impedance (Ohm) Min	Impedance (Ohm) Typ	Impedance Length (%) Max	Impedance Length (%) Min	Impedance Length (%) Typ	Length
PP_A<0>	4	0	43.90	40.10	40.10	1.11	73.42	73.42	4953.8350
PP_A<1>	4	0	66.70	40.10	40.20	0.66	18.07	74.68	4952.7540
PP_A<2>	4	0	66.70	40.10	40.20	0.38	18.23	68.63	4957.2060
PP_A<3>	4	0	40.60	40.10	40.20	5.13	18.14	76.73	4956.2510
PP_A<4>	4	0	66.70	40.10	40.20	1.46	18.19	65.33	4955.0500
PP_A<5>	4	0	66.70	40.10	40.20	1.12	18.05	72.06	4951.9680
PP_A<6>	4	0	66.70	40.10	40.20	1.51	18.14	75.11	4956.6930
PP_A<7>	4	0	66.70	40.10	40.20	1.82	18.03	71.57	4951.7500
PP_A<8>	4	0	66.70	40.10	40.20	0.38	18.09	74.60	4953.6540
PP_A<9>	4	0	66.70	40.10	40.20	1.50	18.21	72.62	4954.7210
PP_A<10>	4	0	40.60	40.10	40.20	8.50	18.14	73.36	4951.2660
PP_A<11>	4	0	66.70	40.10	40.20	3.47	18.10	67.11	4953.3710
PP_A<12>	4	0	66.70	40.10	40.20	0.38	18.06	76.00	4954.4830
PP_A<13>	4	0	66.70	40.10	40.20	1.82	18.14	67.92	4952.7320
PP_ACT_N	3	0	40.60	40.10	40.20	0.57	18.15	81.29	4923.6320
PP_BA<0>	4	0	40.60	40.20	40.20	5.09	94.91	94.91	4957.2170
PP_BG1	3	0	40.60	40.10	40.20	0.57	18.21	81.23	4924.4640
PP_CAL_0	1	0	49.60	40.60	48.00	6.39	1.67	91.94	1666.9170
PP_CAS_N	4	0	40.60	40.10	40.20	7.24	18.12	74.65	4956.3440
PP_CKE0	3	0	40.60	40.10	40.10	7.80	92.20	92.20	4055.1050
PP_CKE1	3	0	66.70	40.20	40.20	4.18	84.86	84.86	4056.4760
PP_CKE2	3	0	40.60	40.10	40.10	7.59	92.41	92.41	4957.2240
PP_CKE3	3	0	40.60	40.10	40.10	9.83	90.17	90.17	4948.9570

3a



3b



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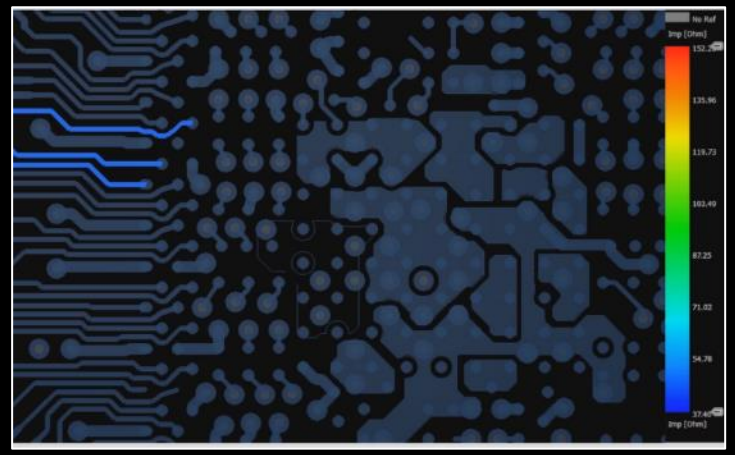
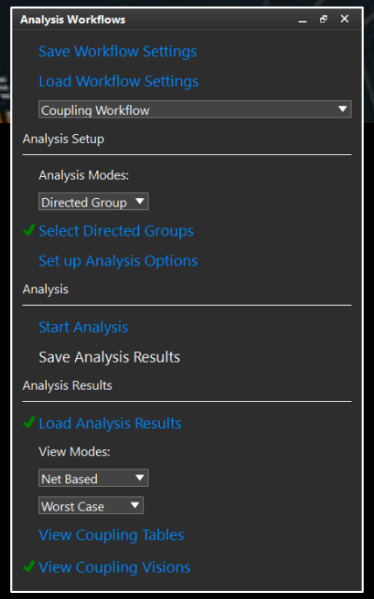


https://resources.pcb.cadence.com/feature-videos/impedance-analysis-feature-video

Coupling Workflow

1. Select the nets (or run the whole PCB) and run the analysis
2. Use the table to find the nets with the highest coupling coefficient
3. Find problems, fix problems, and verify the solution directly on the Allegro design canvas

1



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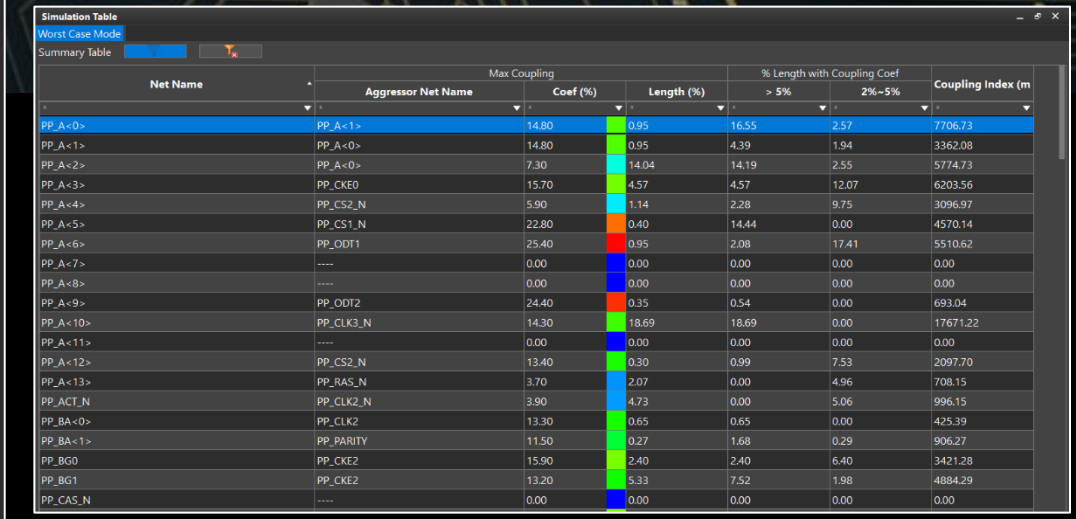
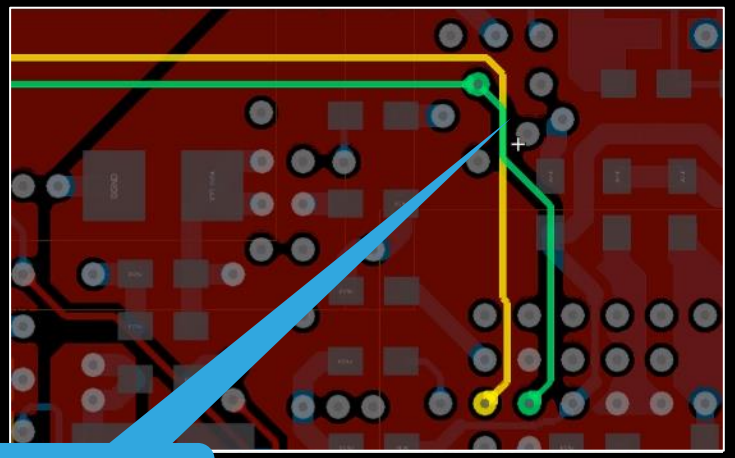


Net Name	Max Coupling: Aggressor Net Name	Coef (%)	Length (%)	% Length with Coupling Coef: > 5%	2%~5%	Coupling Index (m
PP_A<0>	PP_A<1>	14.80	0.95	16.55	2.57	7706.73
PP_A<1>	PP_A<0>	14.80	0.95	4.39	1.94	3362.08
PP_A<2>	PP_A<0>	7.30	14.04	14.19	2.55	5774.73
PP_A<3>	PP_CKE0	15.70	4.57	4.57	12.07	6203.56
PP_A<4>	PP_CS2_N	5.90	1.14	2.28	9.75	3096.97
PP_A<5>	PP_CS1_N	22.80	0.40	14.44	0.00	4570.14
PP_A<6>	PP_ODT1	25.40	0.95	2.08	17.41	5510.62
PP_A<7>	----	0.00	0.00	0.00	0.00	0.00
PP_A<8>	----	0.00	0.00	0.00	0.00	0.00
PP_A<9>	PP_ODT2	24.40	0.35	0.54	0.00	693.04
PP_A<10>	PP_CLK3_N	14.30	18.69	18.69	0.00	17671.22
PP_A<11>	----	0.00	0.00	0.00	0.00	0.00
PP_A<12>	PP_CS2_N	13.40	0.30	0.99	7.53	2097.70
PP_A<13>	PP_RAS_N	3.70	2.07	0.00	4.96	708.15
PP_ACT_N	PP_CLK2_N	3.90	4.73	0.00	5.06	996.15
PP_BA<0>	PP_CLK2	13.30	0.65	0.65	0.00	425.39
PP_BA<1>	PP_PARITY	11.50	0.27	1.68	0.29	906.27
PP_BG0	PP_CKE2	15.90	2.40	2.40	6.40	3421.28
PP_BG1	PP_CKE2	13.20	5.33	7.52	1.98	4884.29
PP_CAS_N	----	0.00	0.00	0.00	0.00	0.00

3a



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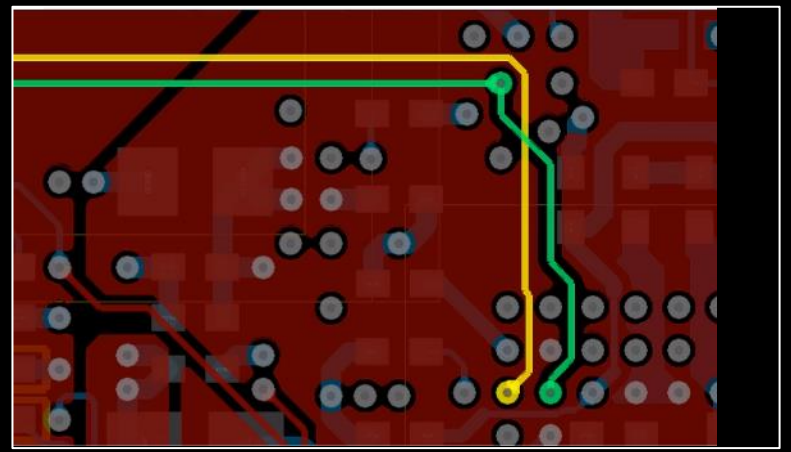

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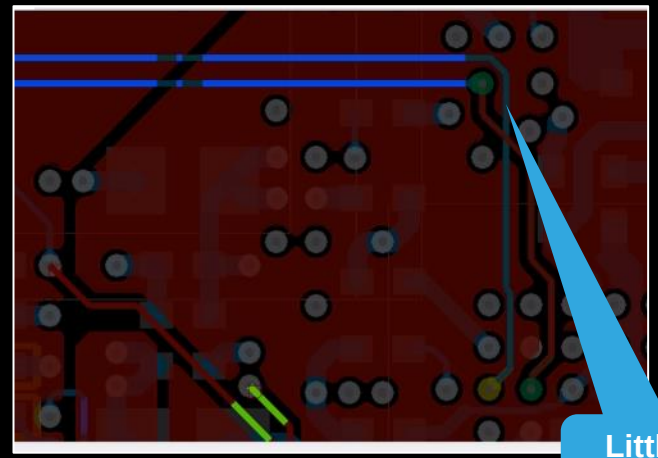


Strong coupling

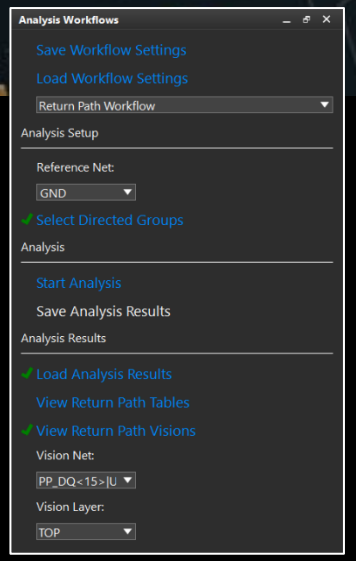
Little to no coupling

https://resources.pcb.cadence.com/feature-videos/coupling-analysis-feature-video

Return Path Workflow

1. Select devices and nets of interest and run the return path simulation
2. Look for worst return path quality (loop inductance) factor (1.0 is ideal)
3. Find problems, fix problems, and verify the solution directly on the Allegro design canvas

1

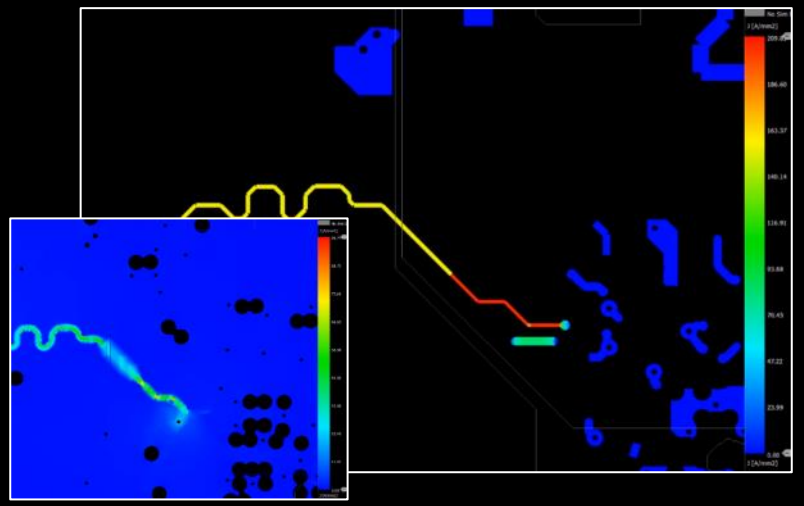


2

Simulation Table

Net/Xnet Name	Return Path		Start Signal Pin	Start Return Pin	End Signal Pin	End Return Pin
	Quality Factor	Vision				
PP_CKE0	2.070	Restart Simulation	U2.AA8	U2.Y11	DDR4_DIMM1.59	DDR4_DIMM1.56
PP_RESET0_N	1.799	Start Simulation	U2.AB8	U2.Y11	DDR4_DIMM1.57	DDR4_DIMM1.56
PP_DQ<15>	1.758	Restart Simulation	U2.V19	U2.U20	DDR4_DIMM1.174	DDR4_DIMM1.173
PP_DQ9_D	1.719	Start Simulation	U2.W16	U2.U20	DDR4_DIMM1.169	DDR4_DIMM1.170
PP_DQ<7>	1.689	Start Simulation	U2.AA19	U2.Y21	DDR4_DIMM1.152	DDR4_DIMM1.151
PP_DQ<11>	1.668	Start Simulation	U2.V16	U2.P17	DDR4_DIMM1.176	DDR4_DIMM1.177
PP_A<13>	1.612	Start Simulation	U2.T8	U2.P9	DDR4_DIMM1.229	DDR4_DIMM1.231
PP_DQ20_D	1.595	Start Simulation	U2.AB4	U2.AB1	DDR4_DIMM1.105	DDR4_DIMM1.106
PP_A<3>	1.591	Start Simulation	U2.T13	U2.U12	DDR4_DIMM1.70	DDR4_DIMM1.56
PP_DQ<1>	1.574	Start Simulation	U2.W17	U2.U20	DDR4_DIMM1.147	DDR4_DIMM1.146
PP_A<11>	1.569	Start Simulation	U2.T14	U2.P15	DDR4_DIMM1.207	DDR4_DIMM1.199
PP_CKE1	1.564	Start Simulation	U2.V8	U2.Y11	DDR4_DIMM1.200	DDR4_DIMM1.199
PP_DQ0_D	1.557	Start Simulation	U2.W18	U2.U20	DDR4_DIMM1.4	DDR4_DIMM1.3
PP_DQ<10>	1.551	Start Simulation	U2.V17	U2.U20	DDR4_DIMM1.33	DDR4_DIMM1.32
PP_DQ<14>	1.537	Start Simulation	U2.W19	U2.Y21	DDR4_DIMM1.31	DDR4_DIMM1.30

3a



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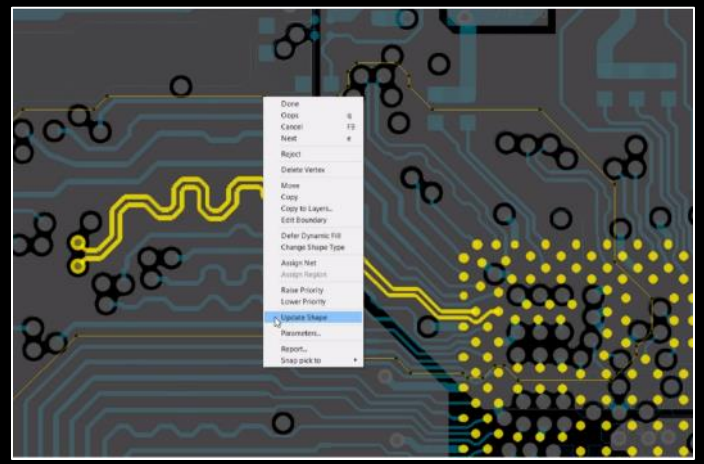

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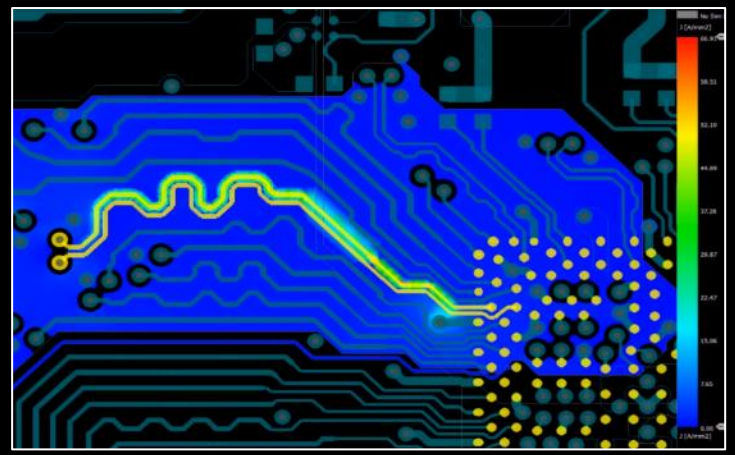
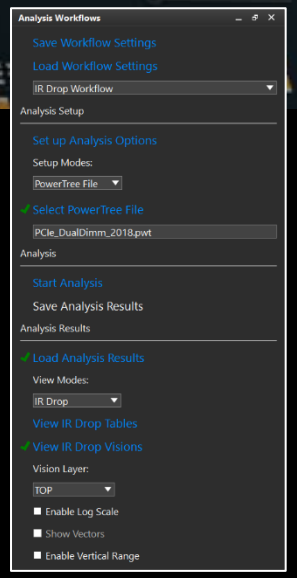


https://resources.pcb.cadence.com/feature-videos/return-path-analysis-feature-video

IR Drop Workflow

1. Load PowerTree and Analyze
2. Use the table to find the power nets with the worst voltage drop
3. Find problems, fix problems, and verify the solution directly on the Allegro design canvas

1

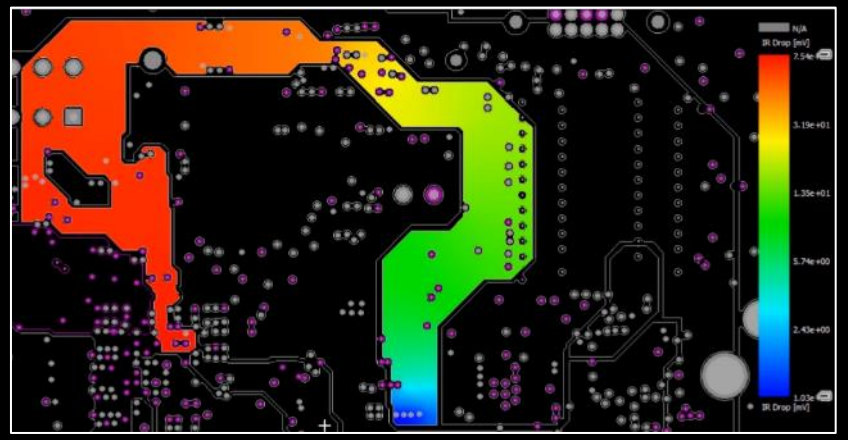


2

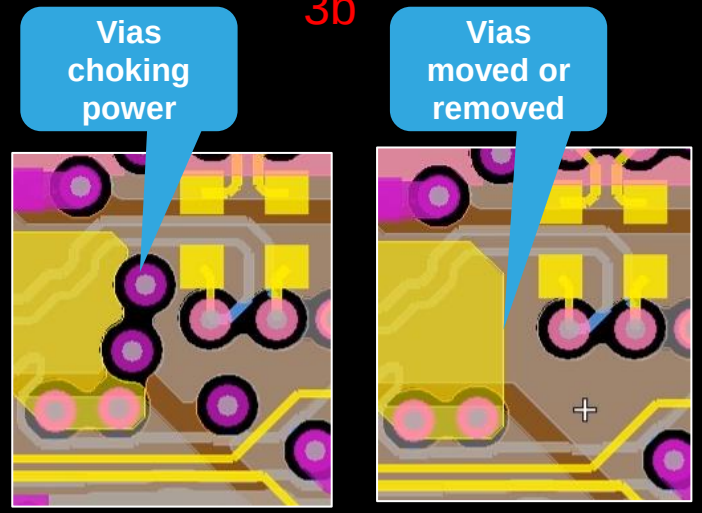
Summary Table

Sink Name	Nominal Voltage (V)	Actual Voltage (V)	IR Drop (mV)	P/F Status	Margin (mV)	Model	Nominal Current (A)	Tolerance	
								Upper (+%)	Lower (-%)
SINK_U25_P3V3_STBY_GND	3.3	3.01015	289.851	FAIL	-124.851	Unequal Current	0.1	5	5
SINK_U26_P5V_STBY_GND	5	4.85283	147.171	PASS	102.829	Unequal Current	0.2	5	5
SINK_U28_P3V3_STBY_GND	3.3	3.00916	290.838	FAIL	-125.838	Unequal Current	0.1	5	5
SINK_U28_P5V_STBY_GND	5	4.92478	75.224	PASS	174.776	Unequal Current	0.2	5	5
SINK_U30_P1V5_PCH_GND	1.5	1.48235	17.652	PASS	57.348	Unequal Current	1.5	5	5
SINK_U30_P3V3_STBY_GND	3.3	3.00252	297.481	FAIL	-132.481	Unequal Current	0.9	5	5
SINK_U32_P3V3_STBY_GND	3.3	3.0104	289.604	FAIL	-124.604	Unequal Current	0.1	5	5
SINK_U34_P3V3_STBY_GND	3.3	3.01021	289.792	FAIL	-124.792	Unequal Current	0.1	5	5
SINK_U35_P3V3_STBY_GND	3.3	3.0103	289.695	FAIL	-124.695	Unequal Current	0.1	5	5
SINK_U37_P12V_STBY_CONN_GND	12	11.9372	62.85	PASS	537.15	Unequal Current	0.1	5	5
SINK_U38_P3V3_STBY_GND	3.3	3.01094	289.06	FAIL	-124.06	Unequal Current	0.1	5	5
SINK_U40_P3V3_STBY_GND	3.3	3.01089	289.11	FAIL	-124.11	Unequal Current	1	5	5
SINK_U41_P3V3_STBY_GND	3.3	3.00316	296.838	FAIL	-131.838	Unequal Current	0.1	5	5

3a



3b



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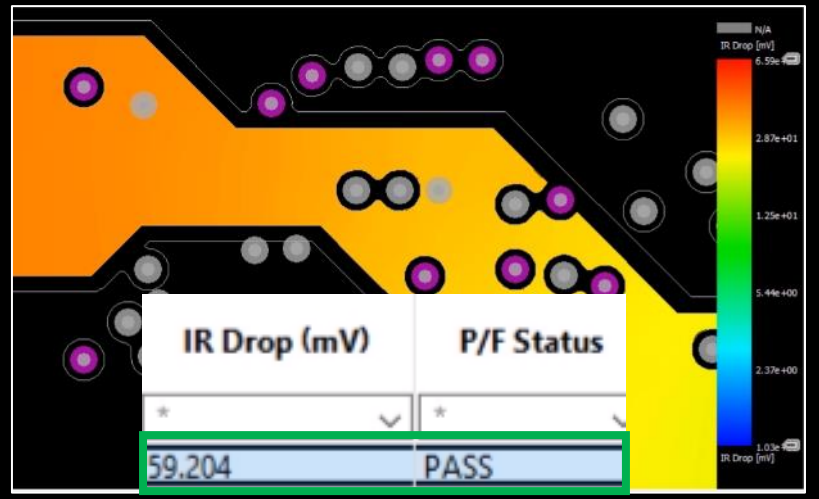
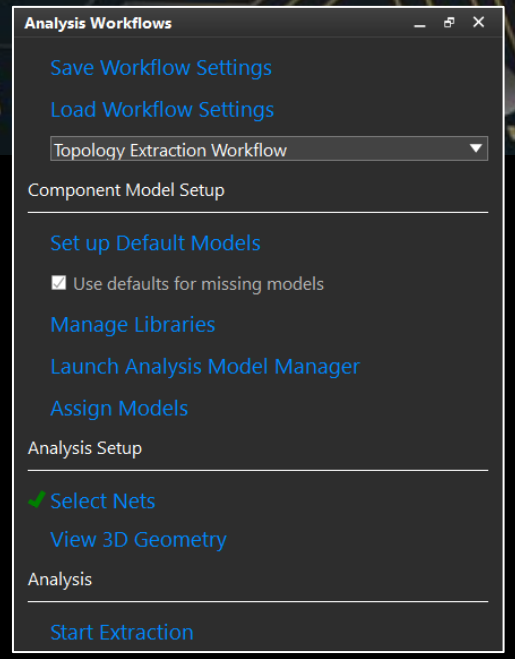
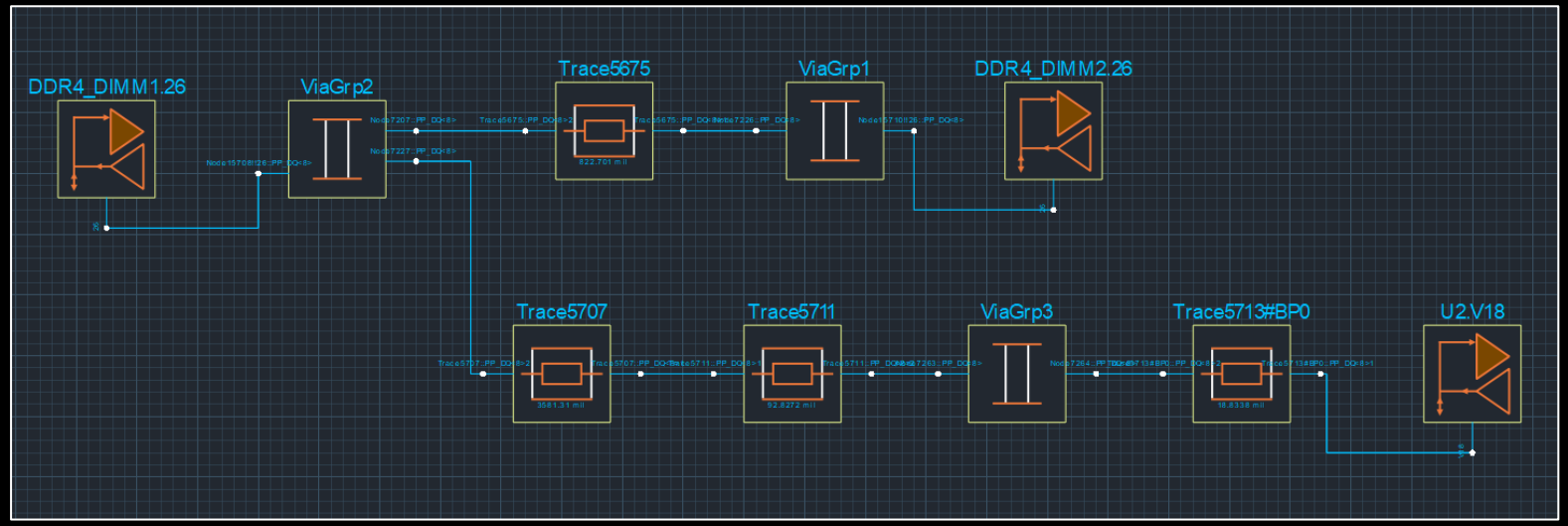


https://resources.pcb.cadence.com/feature-videos/ir-drop-analysis-feature-video

Topology Extraction

- Integrated workflow in Aurora
- Extract single-ended and differential signals into Topology Explorer
- Explore what-if scenarios and develop constraints

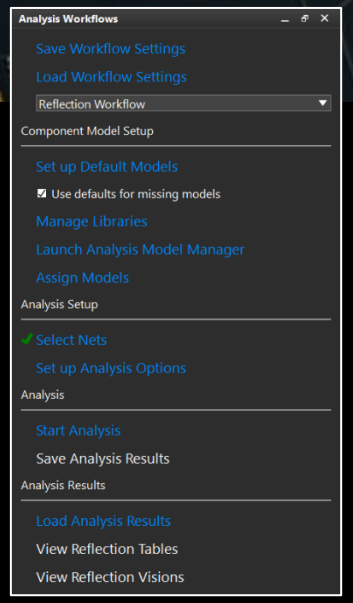




Reflection Workflow

1. Select nets of interest and analyze. IBIS models must be assigned to nets from the AMM library or use defaults
2. Use the table to find the signals with the worst signal quality (e.g. excessive ring back)
3. Find problems, fix problems, and verify the solution directly on the Allegro design canvas

1



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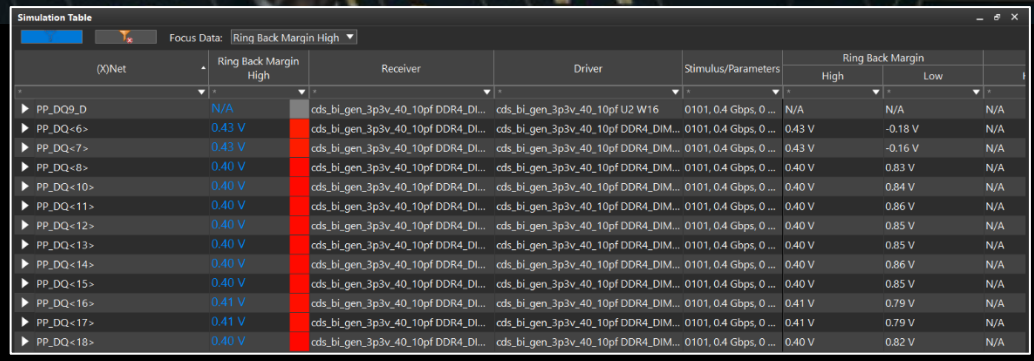

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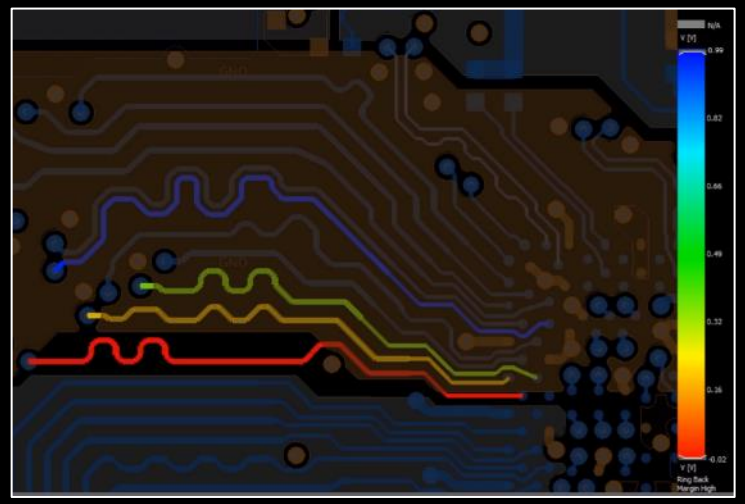
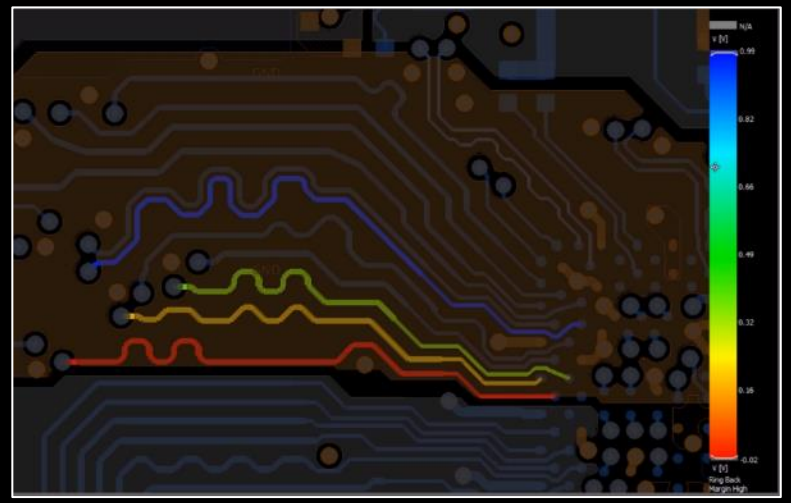


3b



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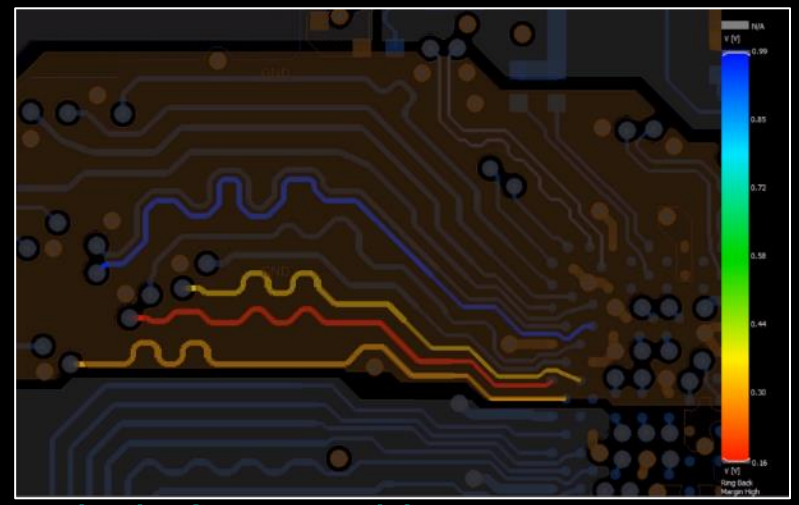
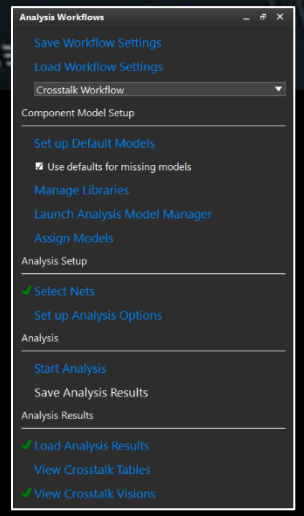


https://resources.pcb.cadence.com/feature-videos/reflection-analysis-feature-video

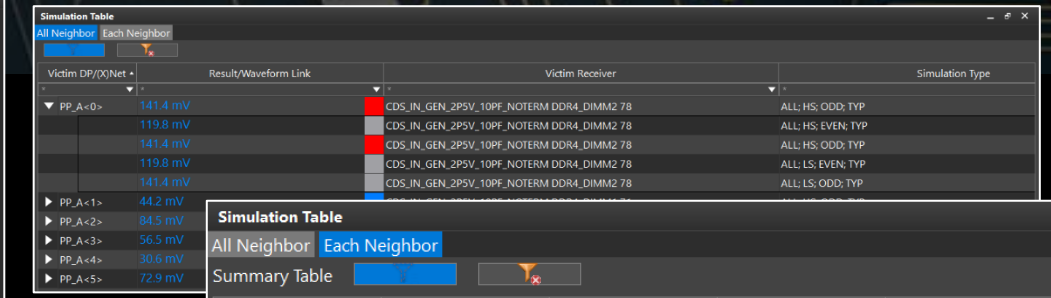
Crosstalk Workflow

1. Select nets of interest and analyze. IBIS models must be assigned to nets from the AMM library or use defaults
2. Use the table to find the signals with the worst crosstalk and view aggressors
3. Find problems, fix problems, and verify the solution directly on the Allegro design canvas

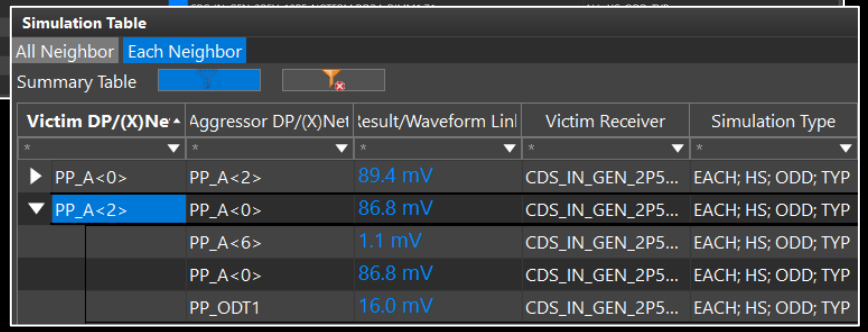
1



2a



2b



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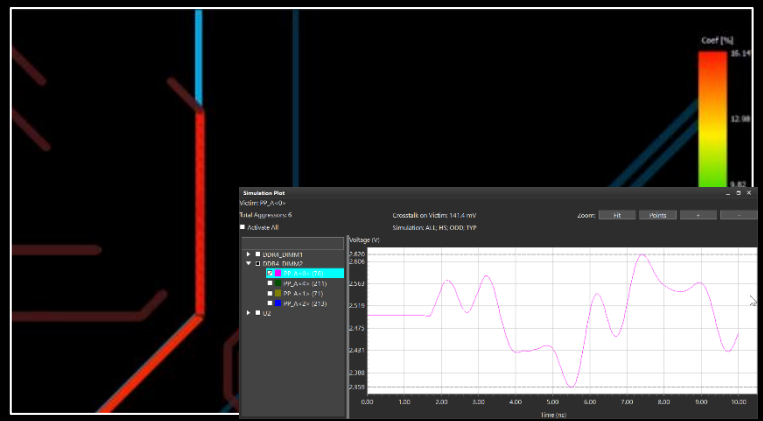

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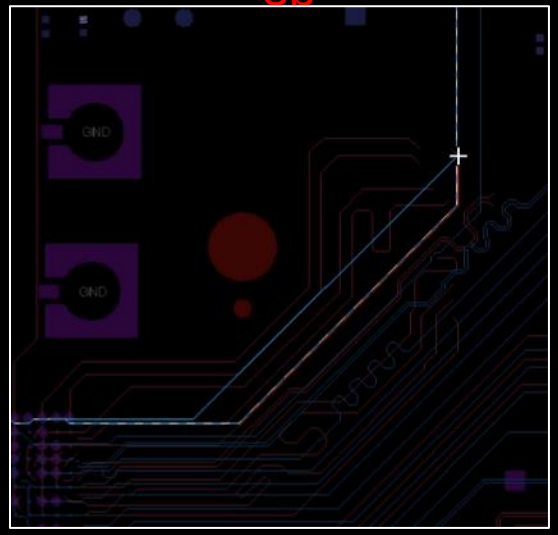

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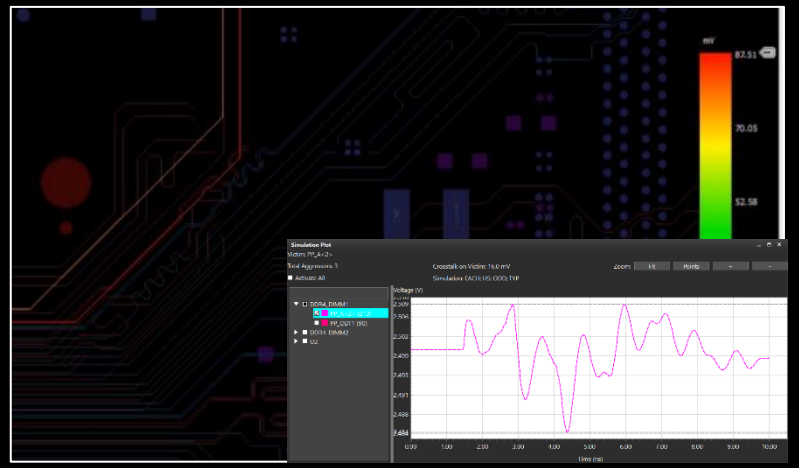
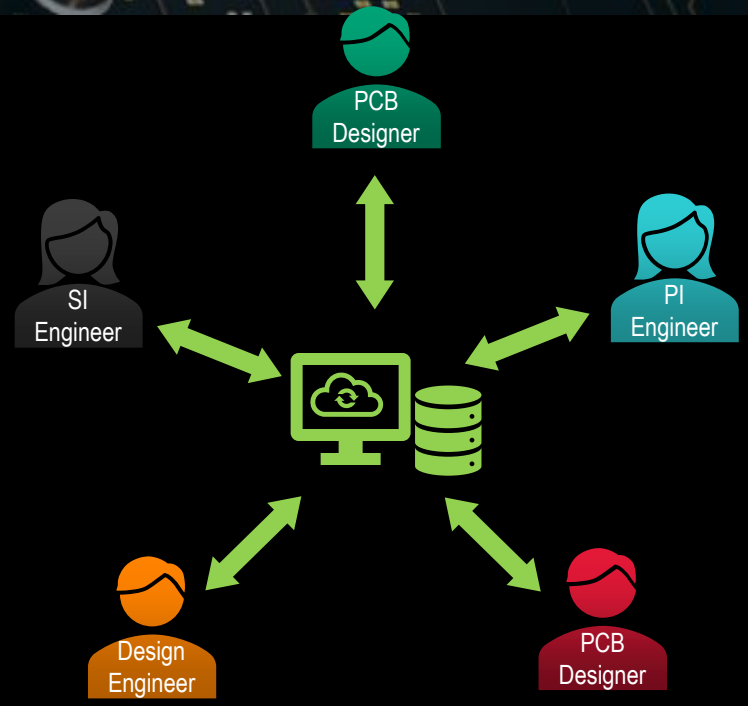


https://resources.pcb.cadence.com/feature-videos/crosstalk-analysis-feature-video

Full Collaboration Use Model: Concurrent Design and Analysis

- Concurrent design and SI / PI Analysis to improve team efficiency
  - Previously, in-cycle analysis has typically occurred on a static ‘saved off’ design version…very difficult to merge in changes
  - Now, engineers can lock a finished section and analyze
  - Engineers can perform what-if changes in the local analyzed area without impacting rest of design
  - Allows real-time analysis on the current design…embed communication so it’s always accurate and timely

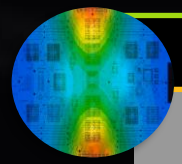


Real-time collaboration between physical design and electrical analysis (Team Design)

Layout Workbench

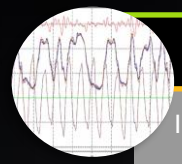
UNIQUE TO SIGRITY

Unified Electrical Analysis Platform



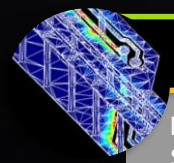
Power Integrity

IR Drop | Resonance
Loop inductance | DeCap Opt



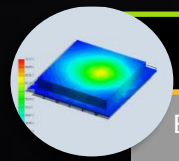
Signal Integrity

Impedance | Coupling | Crosstalk
Noise | TDR/TDT | Return Path



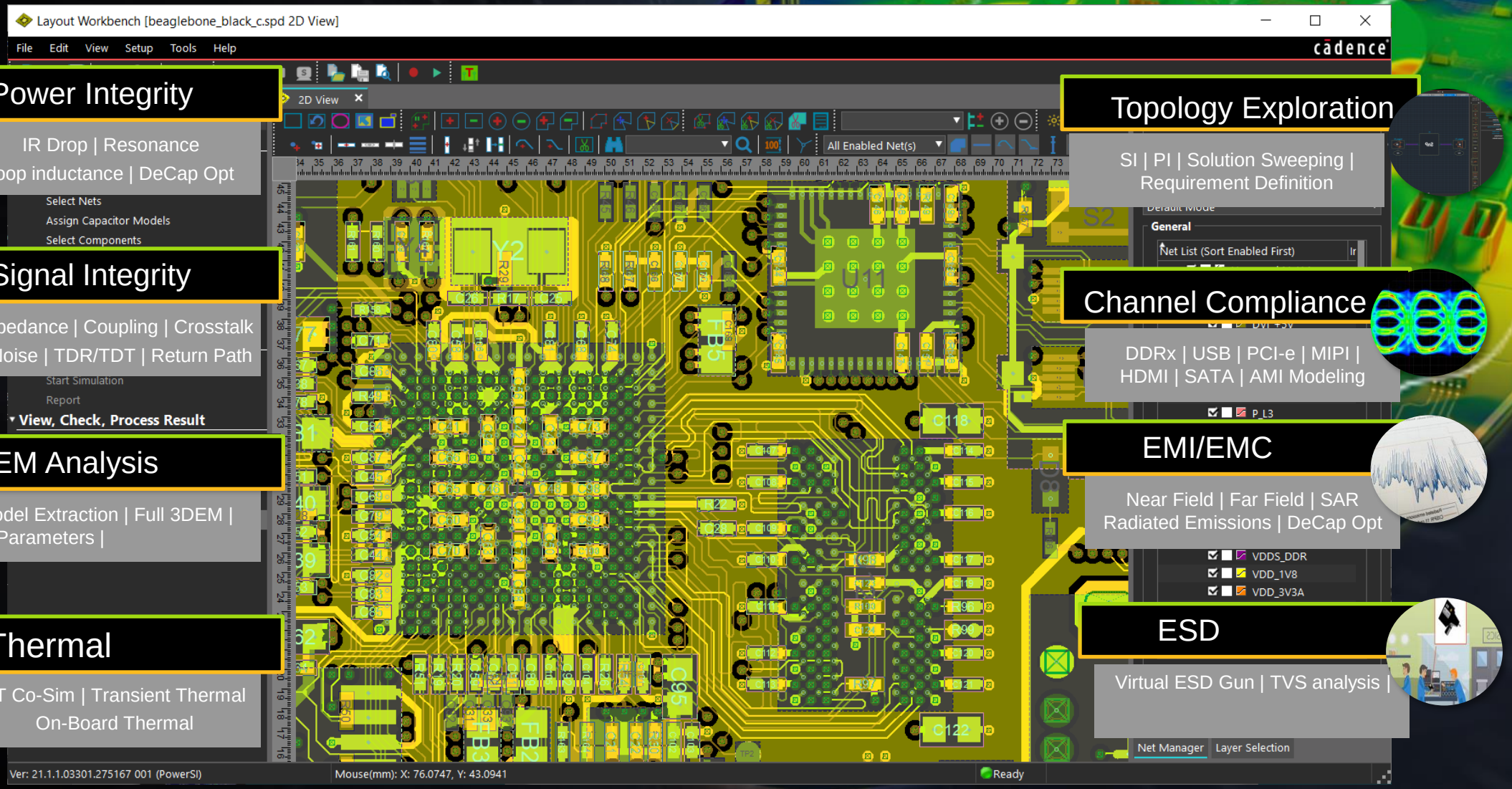
EM Analysis

Model Extraction | Full 3DEM |
S-Parameters |



Thermal

E-T Co-Sim | Transient Thermal
On-Board Thermal



Topology Exploration

SI | PI | Solution Sweeping |
Requirement Definition

Channel Compliance

DDRx | USB | PCI-e | MIPI |
HDMI | SATA | AMI Modeling

EMI/EMC

Near Field | Far Field | SAR
Radiated Emissions | DeCap Opt

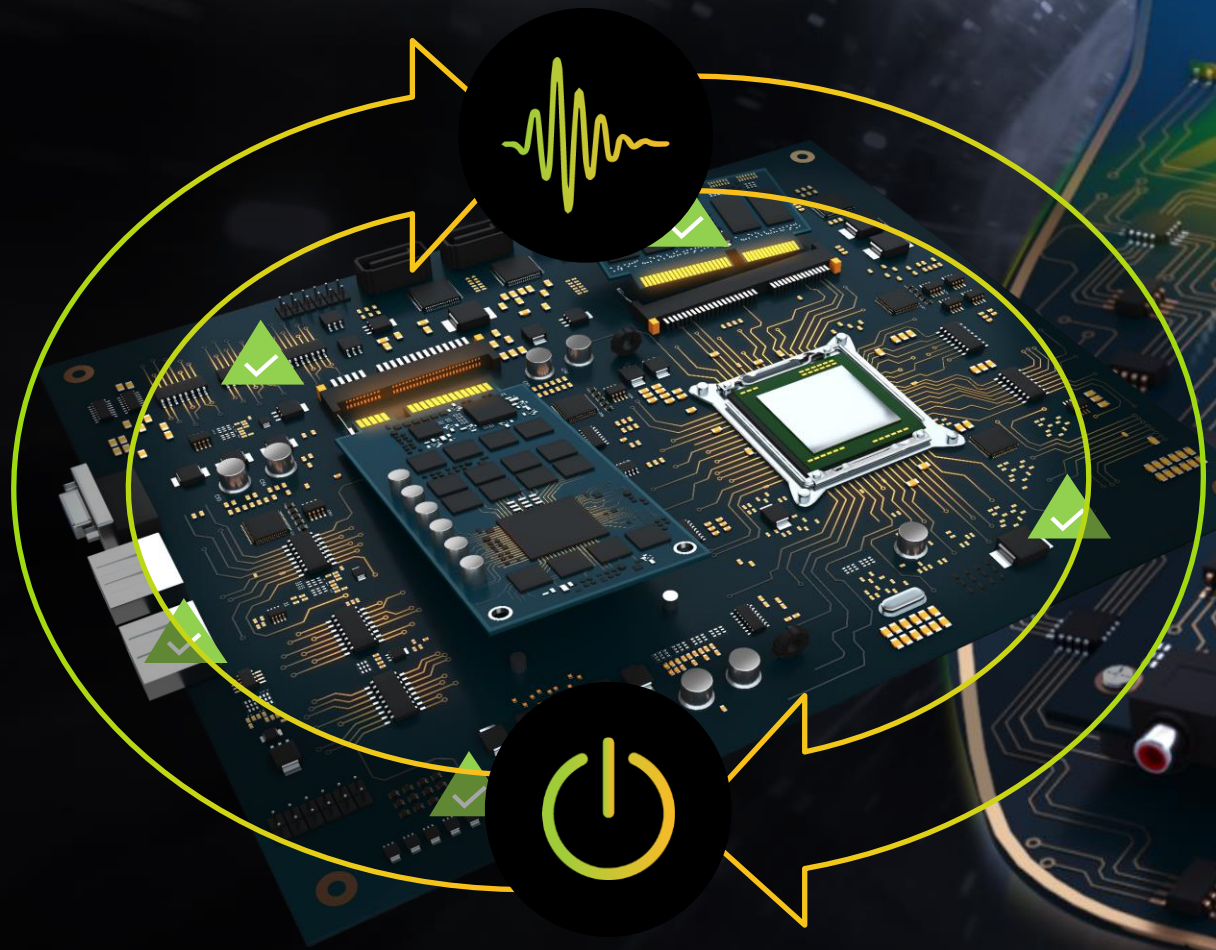
ESD

Virtual ESD Gun | TVS analysis |

EMA Design Automation®

Why Sigrity

Complete Electrical Analysis Solution



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- Optimize for Cost, Perf, Size

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