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2.5D Interposer Design Flow Using Dual-side Component Process in Cadence SiP Layout

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Purpose

This application note uses an example to outline a recommended flow process for setting up 2.5D organic interposers in Cadence® SiP Layout that uses the new dual-side component support capabilities. This is article the first of two application notes in the interposer series. The second will describe process for interposer design and routing.

Audience

This document is intended for any design implementation user of SiP Layout.

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Overview

Cadence® SiP Layout offers a rich technology portfolio for the design of IC packages, simple dies, stacked dies, complex two-sided dies, and, now, 2.5D interposers.

This article outlines a recommended flow for setting up the design database, and lists the steps to correctly design a basic 2.5D interposer component.

Only the 2.5D interposer component flow process is discussed, all other requirements for interface mapping (logic, memory, and so on), constraints, basic routing rules, and so forth are outside the scope of this document.

Setting up Design

Begin designing by setting up the design parameters to support a simple 2.5D interposer. Since a large part of the 2.5D interposer *digita*l design space typically deals with both memory and logic, the settings support both regular die (`die text in`) and die abstracts, which are imported directly from Cadence® Innovus™ Implementation System and the Cadence® Virtuoso® platform.

1. Set up cross-section information
2. Design interposer
3. Set grid
4. Add pins
5. Verify interposer

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Setting up Cross-Section Information

The first step in the design process is to set up cross-section information. The interposer is placed and managed at the SiP Layout die-stack level.

1. Choose *Setup* — *Cross-section*.

   You must add the die stack layers. A 10 layer interposer is defined for this example. The die stack defines the following three parameters:

   - Die location layer (*DIE_PLACE*).
   - Top of interposer for micro bumps (*M1_IPOSER_UBUMP*).
   - Bottom of interposer for c4 bumps and connections to package substrate (*M10_IPOSER_C4*).

   The stack is shown in the following figure.

Cross Section Editor

Export Import Edit View Filters

Primary

Objects		Types >>		Thickness >>	Physical >>	
#	Name	Layer	Layer Function	Value um	Layer ID	Material
*	*	*	*	*	*	*
		Surface				
1	DIE_PLACE	Die Stack			D1	
2	M1_IPOSER_UBUMP	Die Stack			D2	
		Dielectric				
3	M2	Die Stack			D3	
		Dielectric				
4	M3	Die Stack			D4	
		Dielectric				
5	M4	Die Stack			D5	
		Dielectric				
6	M5_BU_COREN	Dielectric			D6	
7	CORE	Dielectric			D7	
8	M6_BU_CORES	Die Stack			D8	
		Dielectric				
9	M7	Die Stack			D9	
		Dielectric				
10	M8	Die Stack			D10	
		Dielectric				
11	M9	Die Stack			D11	
		Dielectric				
12	M10_IPOSER_C4	Die Stack			D12	
		Dielectric	Dielectric	25		Fr-4
13	M1_SUB	Conductor	Conductor	14	1	Copper

Info Lock Embedded layers setup Unused pads suppression Refresh materials

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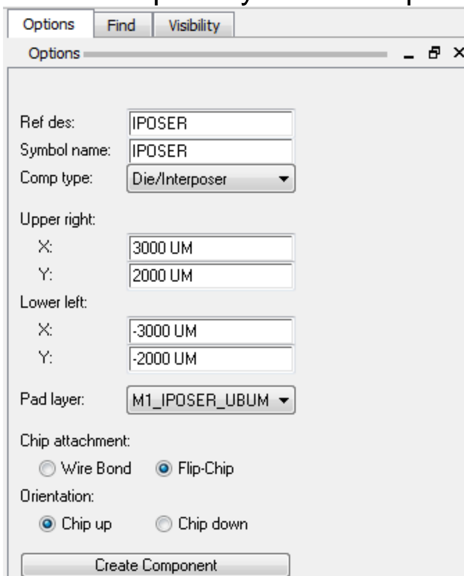
Designing the Interposer

To generate the interposer component, use the Symbol Edit application mode.

1. Choose *Setup — Application Mode — Symbol Edit*.
2. In the Find pane, select *Comps*.
3. Right-click on the canvas and choose *Add Component*.
4. In the Options pane, add parameters for the interposer.

   The following figure shows the parameters used in the example in this document.

   Note: The pad layer is the top of the interposer.

5. Click *Create Component*.

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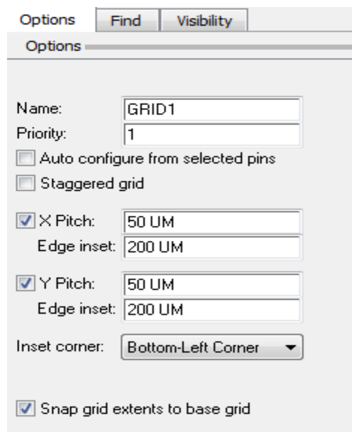
Setting Grid

A basic grid is set in the example.

1. Select the interposer in the design.
2. Right-click and choose *Add Grid*.
3. Setup grid as required. The grid settings for this example is shown in the following figure.



4. Draw a box around the area of the interposer symbol for your grid setup.

Adding Pins to the Interposer

To enhance the pin array generation performance and DRC checks for interposers using large pin arrays, set the *NODRC_SYM_SAME_PIN* property. This property stops the online DRC engine from checking pins defined in the symbol.

1. Set Find filter to *Symbols*.
2. Choose *Edit — Properties*.
3. Select your Symbol.
4. In the Edit Property form, select *NODRC_SYM_SAME_PIN*.

Now add micro bumps to the top and c4 bumps to the bottom of the interposer.

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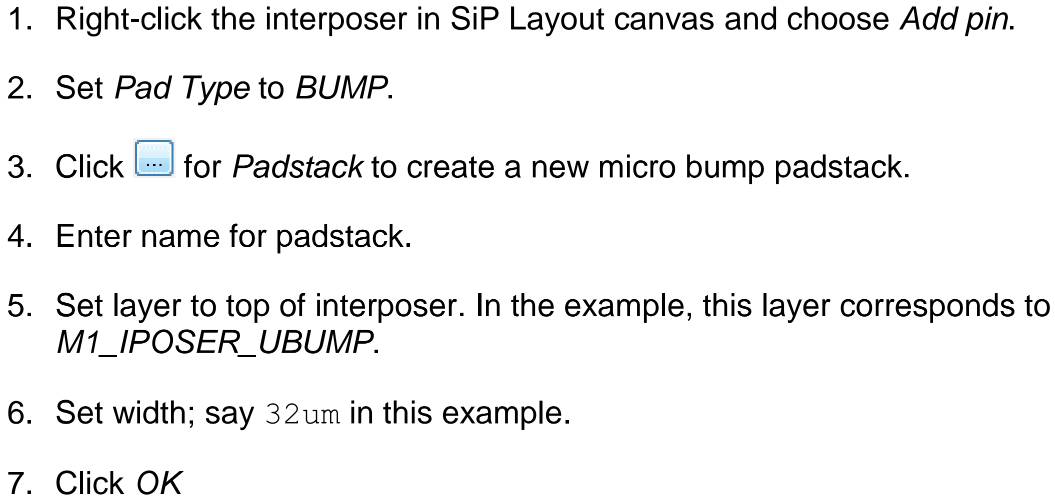
To add micro bump pins to the top of the interposer, do the following steps:.

1. Right-click the interposer in SiP Layout canvas and choose *Add pin*.
2. Set *Pad Type* to *BUMP*.
3. Click  for *Padstack* to create a new micro bump padstack.
4. Enter name for padstack.
5. Set layer to top of interposer. In the example, this layer corresponds to *M1_IPOSER_UBUMP*.
6. Set width; say `32um` in this example.
7. Click *OK*

   The pin is now attached to the cursor.

   This example defines array for both top and bottom of the interposer.
8. In the Options pane, select *Pattern definition*.
9. Add a new group name or use the default.
10. From Pattern style, select *Array*.
11. Add *X offset* and *Y offset*. In the example, both are set to 200um.

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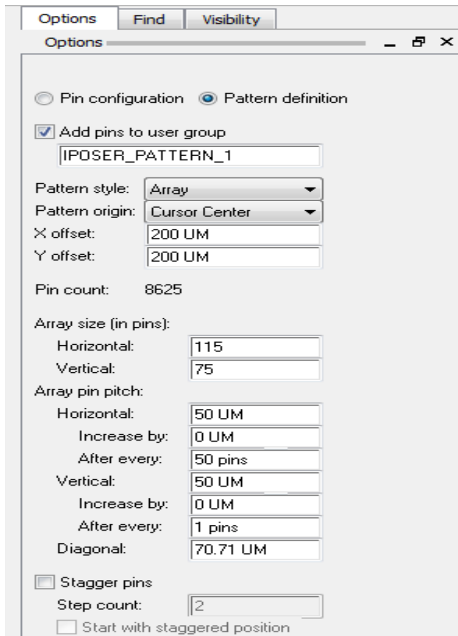
12. Specify Horizontal and Vertical values for array size.

    In this example, Horizontal is set to `115um` and Vertical is set to `75um`. Array pin pitch is set to Horizontal `50um` and Vertical `50um`.

    The array is attached to the cursor. This is an easy way to ensure the array meets the final interposer top micro bump generation.

    The following figure shows the final form prior to placing the micro bump array;



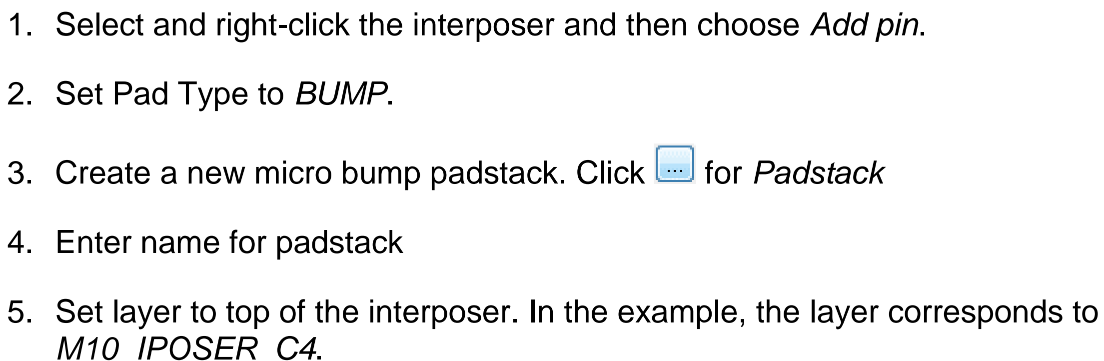
13. Place the array.

14. Right-click and choose *Done*.

To add c4 bumps to the bottom of the interposer, do the following steps:

1. Select and right-click the interposer and then choose *Add pin*.

2. Set Pad Type to *BUMP*.

3. Create a new micro bump padstack. Click  for *Padstack*

4. Enter name for padstack

5. Set layer to top of the interposer. In the example, the layer corresponds to *M10_IPOSER_C4*.

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6. Set width. In the example, it is `80um`.
7. Click *OK*.

   The pin is now attached to the cursor.

   Use an array to define the array for both top and bottom of interposer.
8. In Options pane, switch to *Pattern definition*.
9. Add a new group name or use the default.
10. Select *Array* as the Pattern style.
11. Add offset for X, Y. In this example, both are set to `100um`.
12. Enter Horizontal and Vertical Array size.

    The array is attached to the cursor. This is an easy way to ensure the array meets the final interposer top micro bump generation.
13. Place the array.
14. Right-click and choose *Done*.

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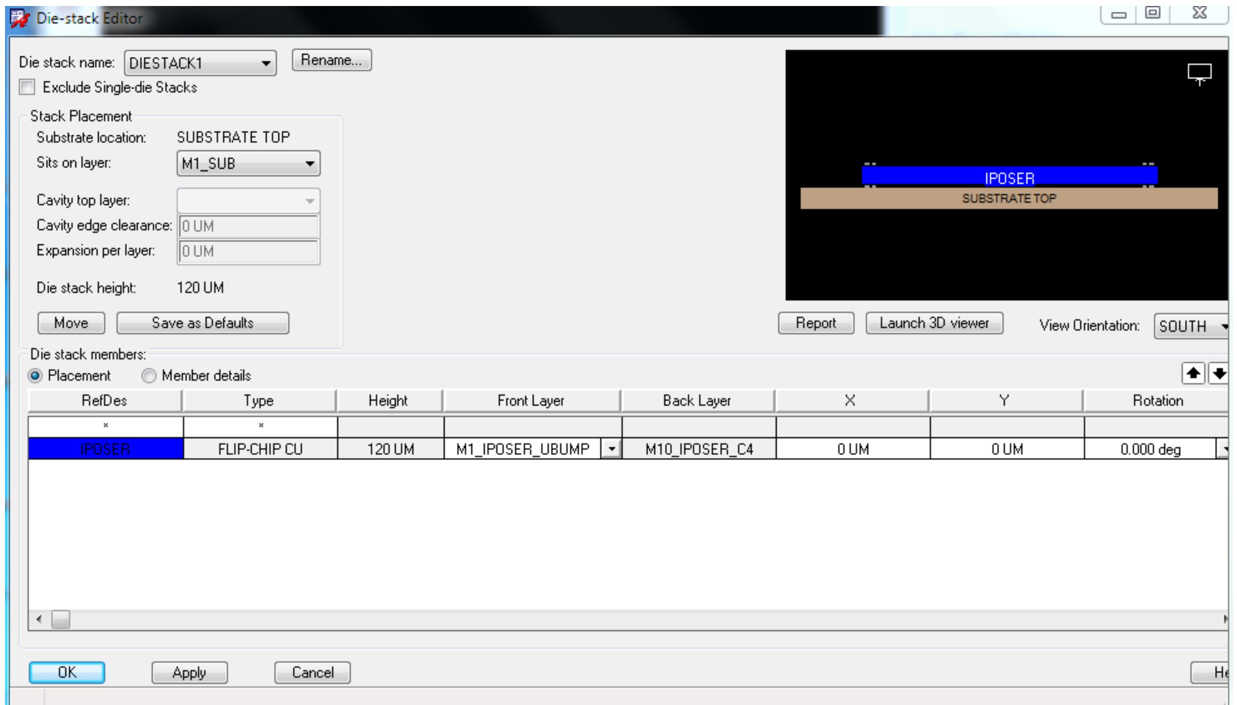
Verifying the Interposer

Verify the interposer by looking at the associated parameters using the die stack editor and 3D viewer.

1. Choose *Edit — Diestack*.

2. Verify the die stack member information and also the view.

   For the interposer created in this example, the die stack member details are shown in the following figure.



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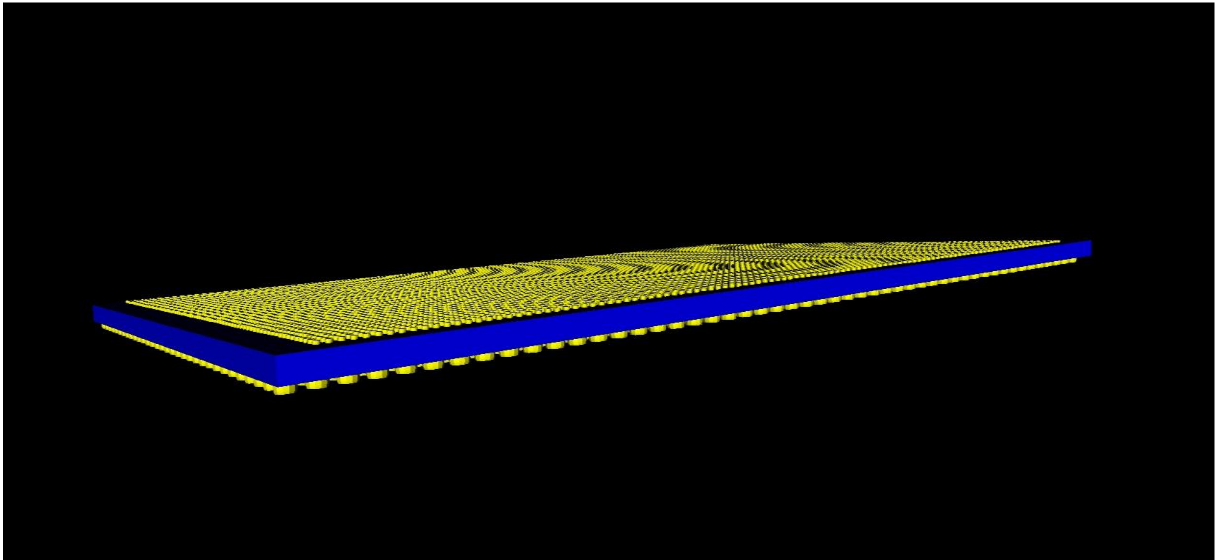
3. In Diestack editor, click *Launch 3D viewer* to open the interposer in Cadence 3D Design Viewer.



Support

Cadence Online Support provides access to support resources, including an extensive knowledge base, access to software updates for Cadence products, and the ability to interact with Cadence Customer Support. Visit *https://support.cadence.com.*

Feedback

Email comments, questions, and suggestions to content_feedback@cadence.com.

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